

# MC74HCT4066A

## Quad Analog Switch/ Multiplexer/Demultiplexer with LSTTL Compatible Inputs

### High-Performance Silicon-Gate CMOS

The MC74HCT4066A utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF-channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full power-supply range (from  $V_{CC}$  to GND).

The HCT4066A is identical in pinout to the metal-gate CMOS MC14016 and MC14066. Each device has four independent switches. The device has been designed so the ON resistances ( $R_{ON}$ ) are more linear over input voltage than  $R_{ON}$  of metal-gate CMOS analog switches.

The ON/OFF control inputs are compatible with standard CMOS and LSTTL outputs. For analog switches with voltage-level translators, see the HC4316A.

#### Features

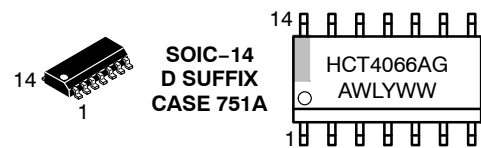
- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Wide Power-Supply Voltage Range ( $V_{CC} - GND$ ) = 4.5 to 5.5 V
- Analog Input Voltage Range ( $V_{CC} - GND$ ) = 0 to 5.5 V
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14016 or MC14066
- Low Noise
- Chip Complexity: 44 FETs or 11 Equivalent Gates
- These are Pb-Free Devices



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#### MARKING DIAGRAMS



A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week  
G or ▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# MC74HCT4066A

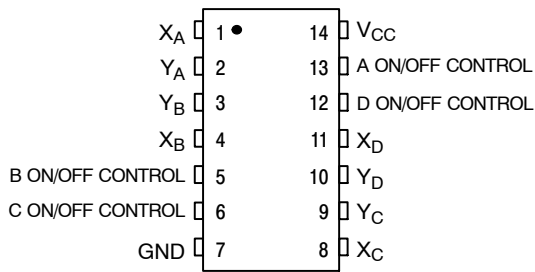
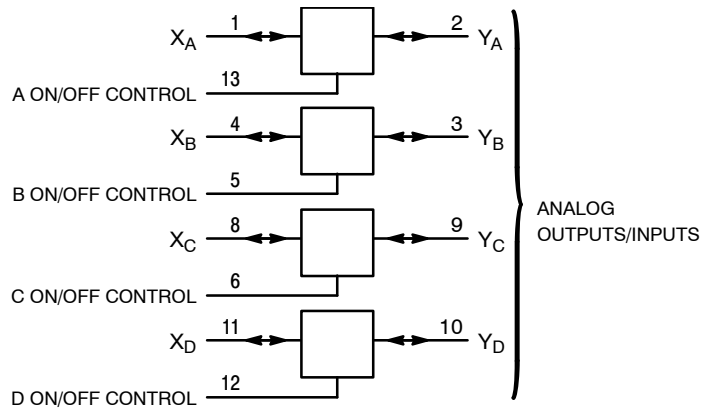


Figure 1. Pin Assignment

## FUNCTION TABLE

| On/Off Control Input | State of Analog Switch |
|----------------------|------------------------|
| L                    | Off                    |
| H                    | On                     |



ANALOG INPUTS/OUTPUTS = X<sub>A</sub>, X<sub>B</sub>, X<sub>C</sub>, X<sub>D</sub>  
 PIN 14 = V<sub>CC</sub>  
 PIN 7 = GND

Figure 2. Logic Diagram

## ORDERING INFORMATION

| Device            | Package           | Shipping <sup>†</sup> |
|-------------------|-------------------|-----------------------|
| MC74HCT4066ADG    | SOIC-14 (Pb-Free) | 55 Units / Rail       |
| MC74HCT4066ADR2G  | SOIC-14 (Pb-Free) | 2500 / Tape & Reel    |
| MC74HCT4066ADTR2G | TSSOP-14*         | 2500 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

# MC74HCT4066A

## MAXIMUM RATINGS

| Symbol    | Parameter  | Value                  | Unit |
|-----------|--|------------------------|------|
| $V_{CC}$  | Positive DC Supply Voltage (Referenced to GND)                     | -0.5 to +14.0          | V    |
| $V_{IS}$  | Analog Input Voltage (Referenced to GND)                           | -0.5 to $V_{CC} + 0.5$ | V    |
| $V_{in}$  | Digital Input Voltage (Referenced to GND)                          | -0.5 to $V_{CC} + 0.5$ | V    |
| I         | DC Current Into or Out of Any Pin                                  | $\pm 25$               | mA   |
| $P_D$     | Power Dissipation in Still Air,<br>SOIC Package†<br>TSSOP Package† | 500<br>450             | mW   |
| $T_{stg}$ | Storage Temperature  | -65 to +150            | °C   |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating – SOIC Package: - 7 mW/°C from 65°C to 125°C  
TSSOP Package: - 6.1 mW/°C from 65°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

## RECOMMENDED OPERATING CONDITIONS

| Symbol     | Parameter  | Min                           | Max      | Unit |
|------------|--|-------------------------------|----------|------|
| $V_{CC}$   | Positive DC Supply Voltage (Referenced to GND)                 | 4.5                           | 5.5      | V    |
| $V_{IS}$   | Analog Input Voltage (Referenced to GND)                       | GND                           | $V_{CC}$ | V    |
| $V_{in}$   | Digital Input Voltage (Referenced to GND)                      | GND                           | $V_{CC}$ | V    |
| $V_{IO}^*$ | Static or Dynamic Voltage Across Switch                        | -                             | 1.2      | V    |
| $T_A$      | Operating Temperature, All Package Types                       | -55                           | +125     | °C   |
| $t_r, t_f$ | Input Rise and Fall Time, ON/OFF Control Inputs<br>(Figure 10) | $V_{CC} = 4.5 \text{ V}$<br>0 | 500      | ns   |

\*For voltage drops across the switch greater than 1.2 V (switch on), excessive  $V_{CC}$  current may be drawn; i.e., the current out of the switch may contain both  $V_{CC}$  and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

## DC ELECTRICAL CHARACTERISTIC Digital Section (Voltages Referenced to GND)

| Symbol          | Parameter  | Test Conditions   | $V_{CC}$<br>V | Guaranteed Limit |           |           | Unit    |
|-----------------|--|---|---------------|------------------|-----------|-----------|---------|
|                 |  |   |               | - 55 to<br>25°C  | ≤ 85°C    | ≤ 125°C   |         |
| $V_{IH}$        | Minimum High-Level Voltage<br>ON/OFF Control Inputs    | $R_{on} = \text{Per Spec}$  | 4.5 to 5.5    | 2.0              | 2.0       | 2.0       | V       |
| $V_{IL}$        | Maximum Low-Level Voltage<br>ON/OFF Control Inputs     | $R_{on} = \text{Per Spec}$  | 4.5 to 5.5    | 0.8              | 0.8       | 0.8       | V       |
| $I_{in}$        | Maximum Input Leakage Current<br>ON/OFF Control Inputs | $V_{in} = V_{CC} \text{ or } GND$   | 5.5           | $\pm 0.1$        | $\pm 1.0$ | $\pm 1.0$ | $\mu A$ |
| $I_{CC}$        | Maximum Quiescent Supply Current<br>(per Package)      | $V_{in} = V_{CC} \text{ or } GND$<br>$V_{IO} = 0 \text{ V}$                     | 5.5           | 2                | 20        | 40        | $\mu A$ |
| $\Delta I_{CC}$ | Additional Quiescent Supply Current<br>(per Input)     | $V_{in} = V_{CC} - 2.1 \text{ V}$<br>Other control inputs at $V_{CC}$<br>or GND | 4.5 to 5.5    | 360              | 450       | 490       | $\mu A$ |

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## DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to GND)

| Symbol           | Parameter  | Test Conditions  | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|------------------|--|--|----------------------|------------------|--------|---------|------|
|                  |  |  |                      | - 55 to<br>25°C  | ≤ 85°C | ≤ 125°C |      |
| R <sub>on</sub>  | Maximum "ON" Resistance  | V <sub>in</sub> = V <sub>IH</sub><br>V <sub>IS</sub> = V <sub>CC</sub> to GND<br>I <sub>S</sub> ≤ 2.0 mA (Figures 3, 4)                | 4.5                  | 120              | 160    | 200     | Ω    |
|                  |  | V <sub>in</sub> = V <sub>IH</sub><br>V <sub>IS</sub> = V <sub>CC</sub> or GND<br>(Endpoints)<br>I <sub>S</sub> ≤ 2.0 mA (Figures 3, 4) | 4.5                  | 70               | 85     | 120     |      |
| ΔR <sub>on</sub> | Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package | V <sub>in</sub> = V <sub>IH</sub><br>V <sub>IS</sub> = 1/2 (V <sub>CC</sub> - GND)<br>I <sub>S</sub> ≤ 2.0 mA                          | 4.5                  | 20               | 25     | 30      | Ω    |
| I <sub>off</sub> | Maximum Off-Channel Leakage Current, Any One Channel                               | V <sub>in</sub> = V <sub>IL</sub><br>V <sub>IO</sub> = V <sub>CC</sub> or GND<br>Switch Off (Figure 5)                                 | 5.5                  | 0.1              | 0.5    | 1.0     | μA   |
| I <sub>on</sub>  | Maximum On-Channel Leakage Current, Any One Channel                                | V <sub>in</sub> = V <sub>IH</sub><br>V <sub>IS</sub> = V <sub>CC</sub> or GND<br>(Figure 6)  | 5.5                  | 0.1              | 0.5    | 1.0     | μA   |

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, ON/OFF Control Inputs: t<sub>r</sub> = t<sub>f</sub> = 6 ns)

| Symbol                                 | Parameter   | V <sub>CC</sub><br>V      | Guaranteed Limit |        |         | Unit |    |
|--|---|---------------------------|------------------|--------|---------|------|----|
|  |   |                           | - 55 to<br>25°C  | ≤ 85°C | ≤ 125°C |      |    |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Analog Input to Analog Output<br>(Figures 10 and 11)   | 4.5                       | 10               | 13     | 15      | ns   |    |
| t <sub>PLZ</sub> ,<br>t <sub>PHZ</sub> | Maximum Propagation Delay, ON/OFF Control to Analog Output<br>(Figures 12 and 13) | 4.5                       | 30               | 38     | 45      | ns   |    |
| t <sub>PZL</sub> ,<br>t <sub>PZH</sub> | Maximum Propagation Delay, ON/OFF Control to Analog Output<br>(Figures 12 and 13) | 4.5                       | 25               | 32     | 37      | ns   |    |
| C                                      | Maximum Capacitance   | ON/OFF Control Input      | -                | 10     | 10      | 10   | pF |
|  |   | Control Input = GND       | -                | 35     | 35      | 35   |    |
|  |   | Analog I/O<br>Feedthrough | -                | 1.0    | 1.0     | 1.0  |    |

| C <sub>PD</sub> | Power Dissipation Capacitance (Per Switch) (Figure 15)* | Typical @ 25°C, V <sub>CC</sub> = 5.0 V |  | pF |
|-----------------|---|---|--|----|
|                 |   | 15                                      |  |    |
|                 |   |   |  |    |

\*Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

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## ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

| Symbol | Parameter   | Test Conditions   | V <sub>CC</sub><br>V | Limit*<br>25°C<br>54/74HCT | Unit             |
|--------|---|---|----------------------|----------------------------|------------------|
| BW     | Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 7) | f <sub>in</sub> = 1 MHz Sine Wave<br>Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>OS</sub><br>Increase f <sub>in</sub> Frequency Until dB Meter Reads - 3 dB<br>R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF | 4.5                  | 150                        | MHz              |
| -      | Off-Channel Feedthrough Isolation (Figure 8)                          | f <sub>in</sub> ≡ Sine Wave<br>Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>IS</sub><br>f <sub>in</sub> = 10 kHz, R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF  | 4.5                  | -50                        | dB               |
|        |   | f <sub>in</sub> = 1.0 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF  | 4.5                  | -40                        |                  |
| -      | Feedthrough Noise, Control to Switch (Figure 9)                       | V <sub>in</sub> ≤ 1 MHz Square Wave (t <sub>r</sub> = t <sub>f</sub> = 6 ns)<br>Adjust R <sub>L</sub> at Setup so that I <sub>S</sub> = 0 A<br>R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF                             | 4.5                  | 60                         | mV <sub>PP</sub> |
|        |   | R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 10 pF  | 4.5                  | 30                         |                  |
| -      | Crosstalk Between Any Two Switches (Figure 14)                        | f <sub>in</sub> ≡ Sine Wave<br>Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>IS</sub><br>f <sub>in</sub> = 10 kHz, R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF  | 4.5                  | -70                        | dB               |
|        |   | f <sub>in</sub> = 1.0 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF  | 4.5                  | -80                        |                  |
| THD    | Total Harmonic Distortion (Figure 16)                                 | f <sub>in</sub> = 1 kHz, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 50 pF<br>THD = THD <sub>Measured</sub> - THD <sub>Source</sub><br>V <sub>IS</sub> = 4.0 V <sub>PP</sub> sine wave                                       | 4.5                  | 0.10                       | %                |

\*Guaranteed limits not tested. Determined by design and verified by qualification.

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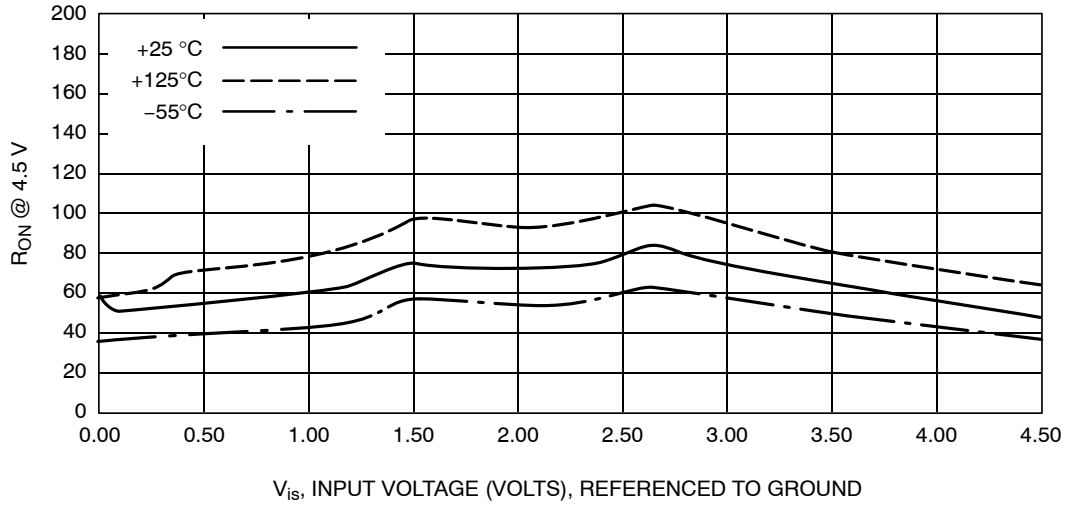


Figure 3. Typical On Resistance,  $V_{CC} = 4.5\text{ V}$

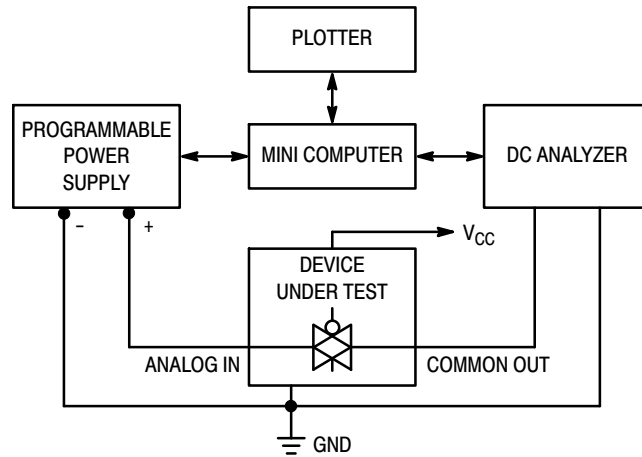


Figure 4. On Resistance Test Set-Up

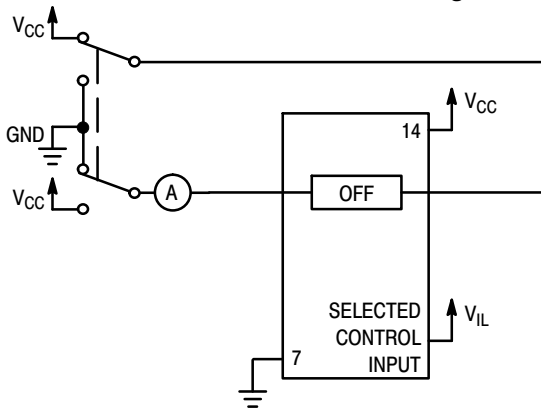


Figure 5. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

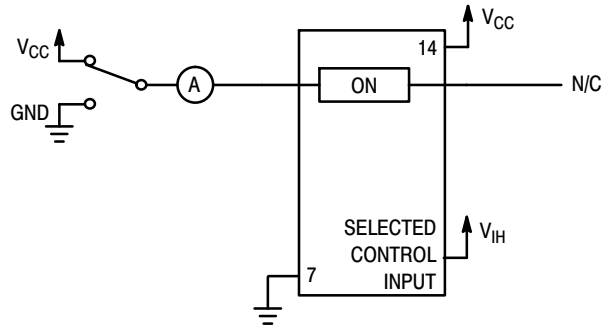
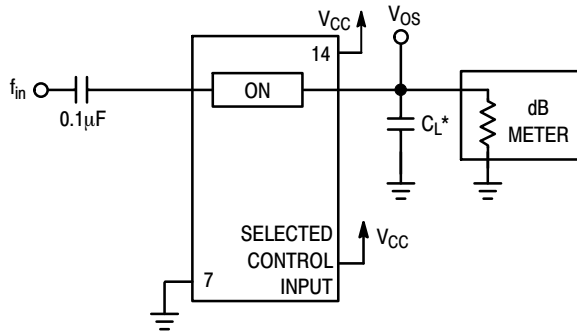


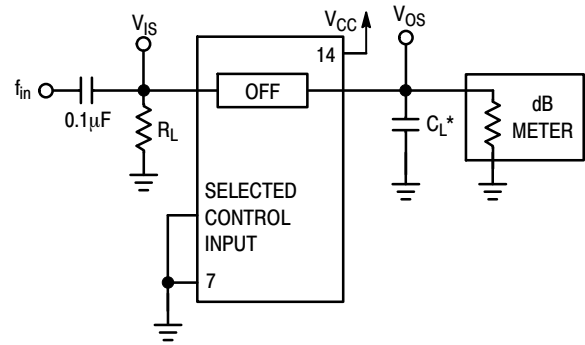
Figure 6. Maximum On Channel Leakage Current, Test Set-Up

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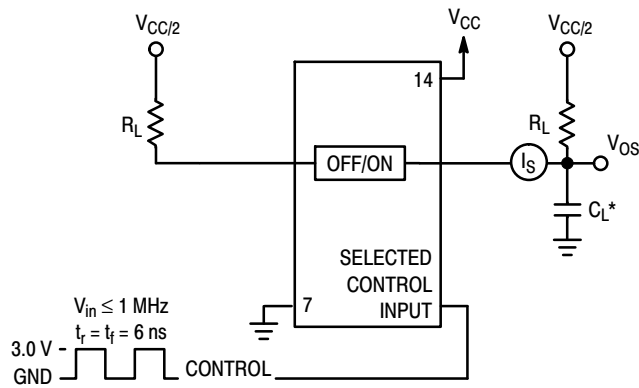
\*Includes all probe and jig capacitance.

**Figure 7. Maximum On-Channel Bandwidth Test Set-Up**



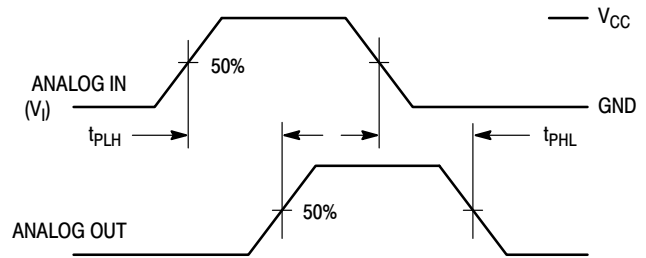
\*Includes all probe and jig capacitance.

**Figure 8. Off-Channel Feedthrough Isolation, Test Set-Up**



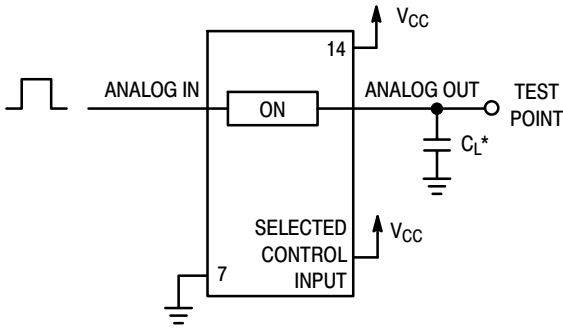
\*Includes all probe and jig capacitance.

**Figure 9. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set-Up**



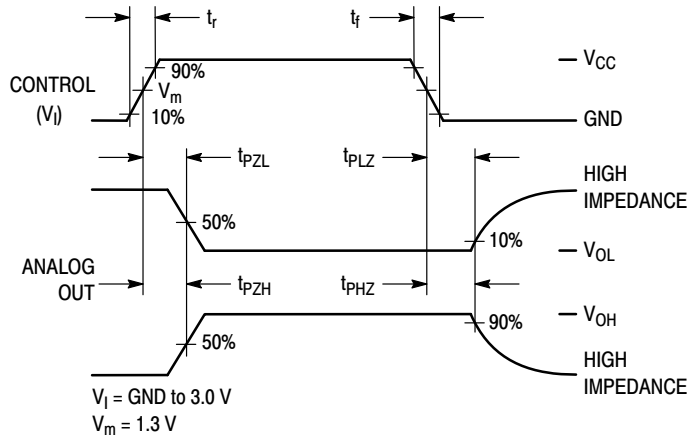
**Figure 10. Propagation Delays, Analog In to Analog Out**

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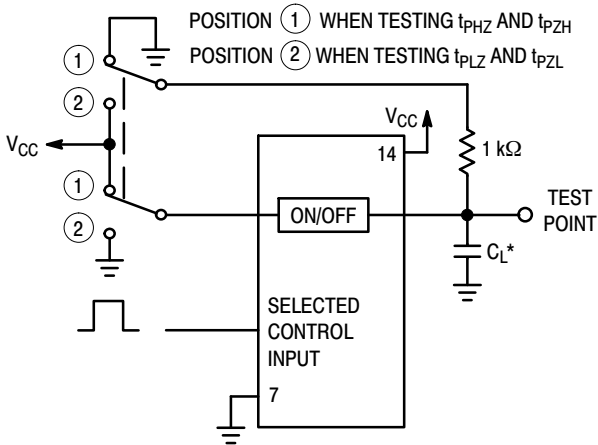


\*Includes all probe and jig capacitance.

**Figure 11. Propagation Delay Test Set-Up**

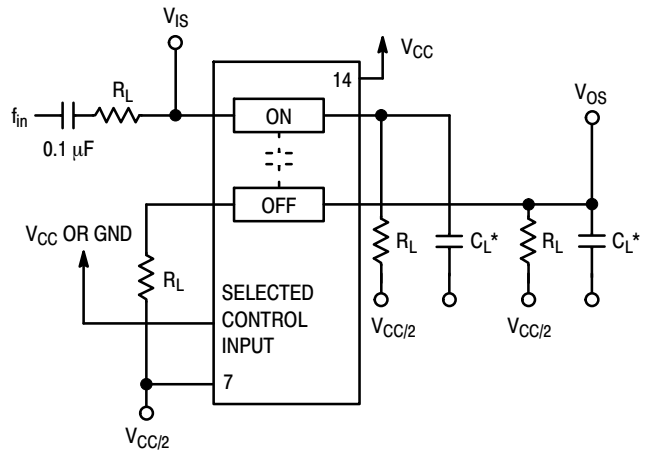


**Figure 12. Propagation Delay, ON/OFF Control to Analog Out**



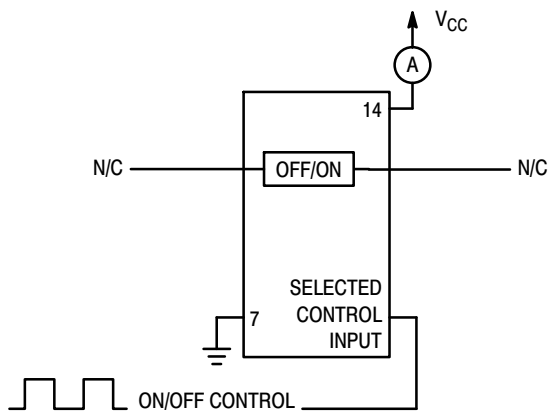
\*Includes all probe and jig capacitance.

**Figure 13. Propagation Delay Test Set-Up**

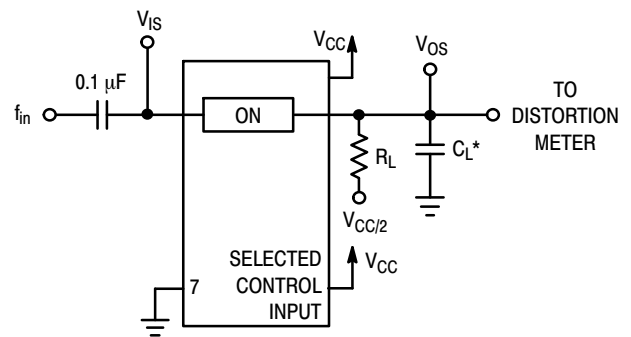


\*Includes all probe and jig capacitance.

**Figure 14. Crosstalk Between Any Two Switches, Test Set-Up**



**Figure 15. Power Dissipation Capacitance Test Set-Up**



\*Includes all probe and jig capacitance.

**Figure 16. Total Harmonic Distortion, Test Set-Up**



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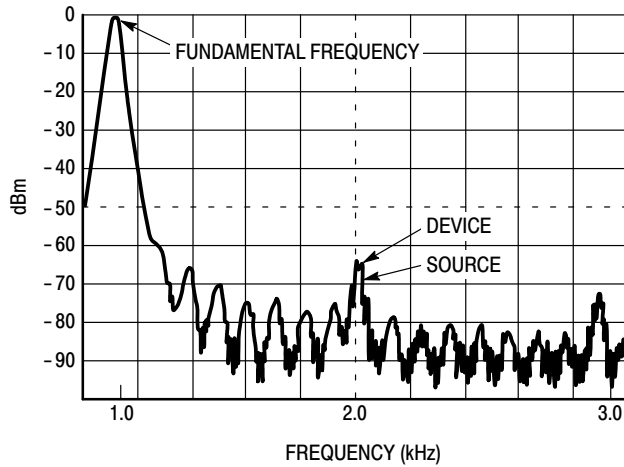


Figure 17. Plot, Harmonic Distortion

## APPLICATION INFORMATION

Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to  $V_{CC}$  or GND through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked-up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages  $V_{CC}$  and GND. The positive peak analog voltage should not exceed  $V_{CC}$ . Similarly, the negative peak analog voltage should not go below GND. In the example below, the difference between  $V_{CC}$  and GND is twelve volts. Therefore, using the configuration in Figure 16, a maximum

analog signal of twelve volts peak-to-peak can be controlled.

When voltage transients above  $V_{CC}$  and/or below GND are anticipated on the analog channels, external diodes ( $D_x$ ) are recommended as shown in Figure 17. These diodes should be small signal, fast turn-on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the  $D_x$  diodes with MOSORB® (MOSORB is an acronym for high current surge protectors). MOSORBs are fast turn-on devices ideally suited for precise DC protection with no inherent wear out mechanism.

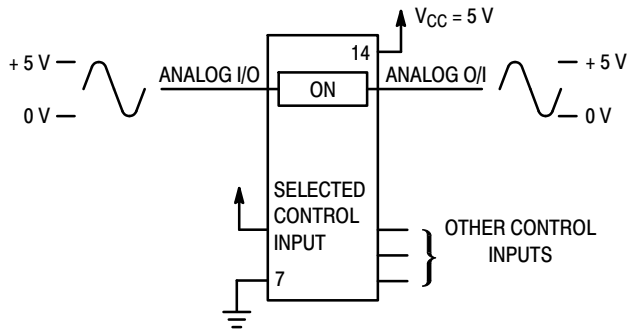


Figure 18. 5 V Application

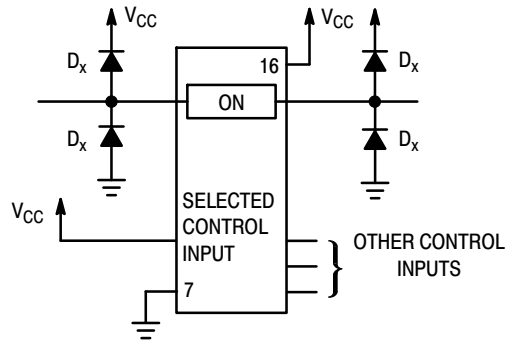
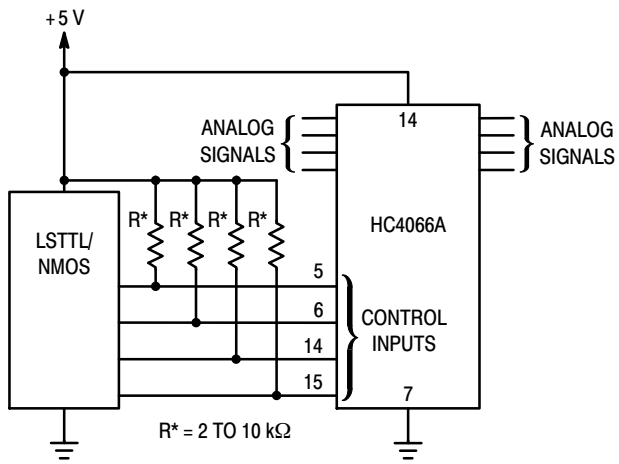
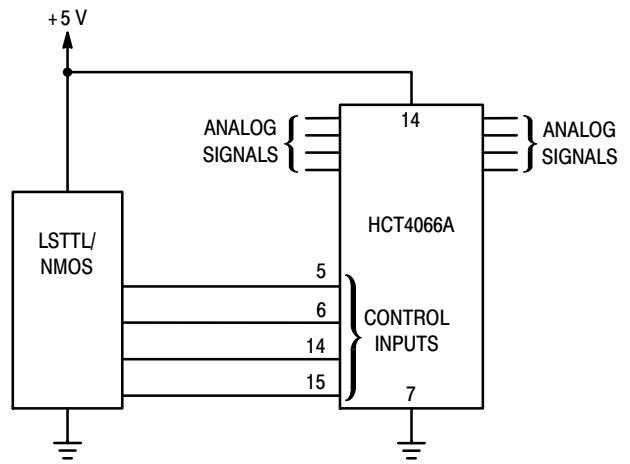


Figure 19. Transient Suppressor Application

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a. Using Pull-Up Resistors with HC Device



b. Using HCT Buffer

Figure 20. LSTTL/NMOS to HCTMOS Interface

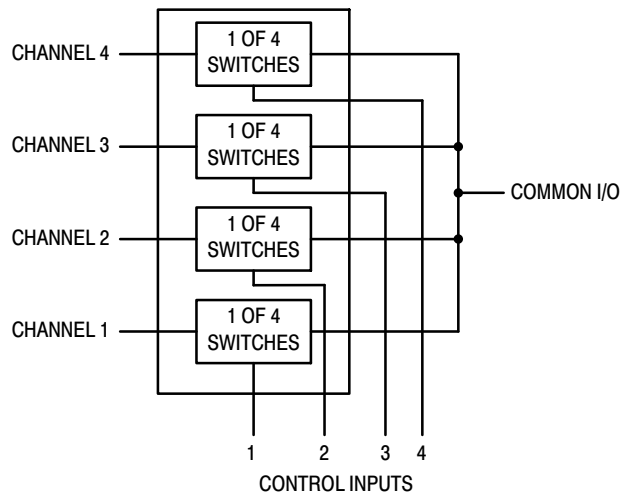


Figure 21. 4-Input Multiplexer

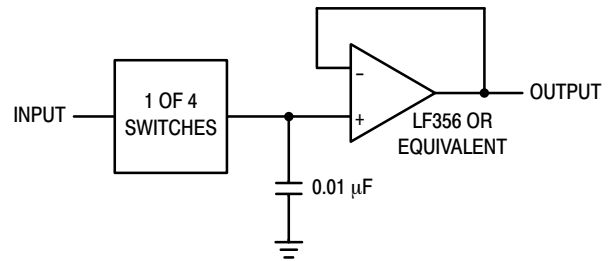
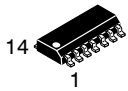


Figure 22. Sample/Hold Amplifier

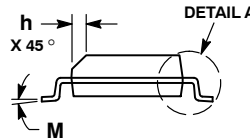
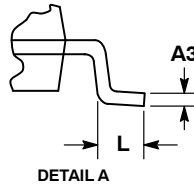
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 1.35        | 1.75 | 0.054     | 0.068 |
| A1  | 0.10        | 0.25 | 0.004     | 0.010 |
| A3  | 0.19        | 0.25 | 0.008     | 0.010 |
| b   | 0.35        | 0.49 | 0.014     | 0.019 |
| D   | 8.55        | 8.75 | 0.337     | 0.344 |
| E   | 3.80        | 4.00 | 0.150     | 0.157 |
| e   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 5.80        | 6.20 | 0.228     | 0.244 |
| h   | 0.25        | 0.50 | 0.010     | 0.019 |
| L   | 0.40        | 1.25 | 0.016     | 0.049 |
| M   | 0°          | 7°   | 0°        | 7°    |

SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

|                  |             |  |
|------------------|-------------|--|
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**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 2:  
 CANCELLED

STYLE 3:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON CATHODE

STYLE 4:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 5:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 6:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 7:  
 PIN 1. ANODE/CATHODE  
 2. COMMON ANODE  
 3. COMMON CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. COMMON CATHODE  
 12. COMMON ANODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

STYLE 8:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

|                         |                    |   |
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