

Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs

High-Performance Silicon-Gate CMOS

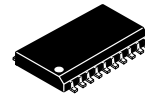
MC74HCT241A

The MC74HCT241A is identical in pinout to the LS241. This device may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs. The HCT241A is an octal noninverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has non-inverted outputs and two output enables. Enable A is active-low and Enable B is active-high.

The HCT241A is similar in function to the HCT244. See also HCT240.

Features

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 118 FETs or 29.5 Equivalent Gates
- Pb-Free Packages are Available*

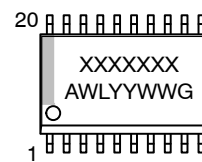


SOIC-20
 DW SUFFIX
 CASE 751D

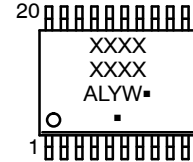


TSSOP-20
 DT SUFFIX
 CASE 948E

MARKING DIAGRAMS



SOIC-20



TSSOP-20

- XXXXXXXX = Specific Device Code
- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74HCT241A

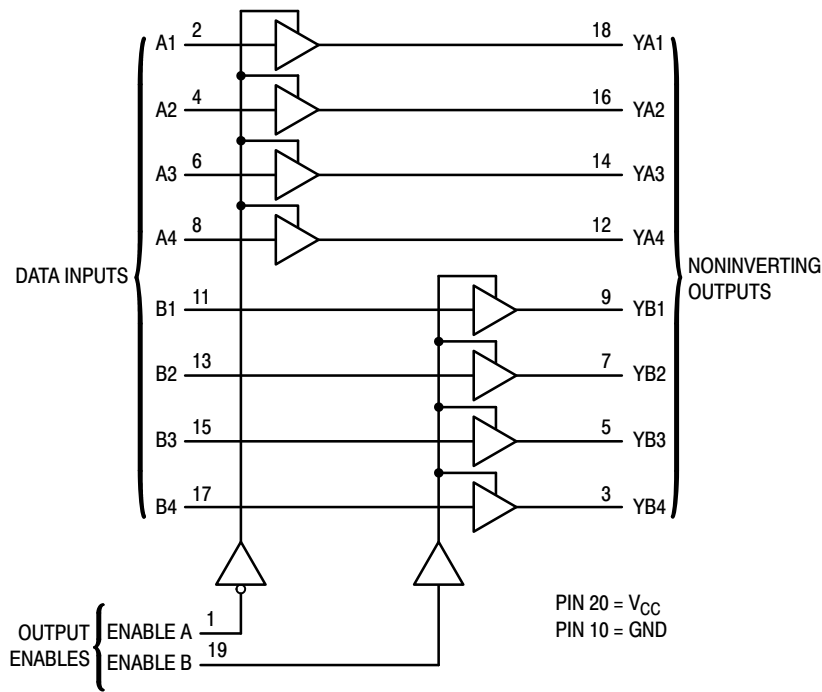


Figure 1. Logic Diagram

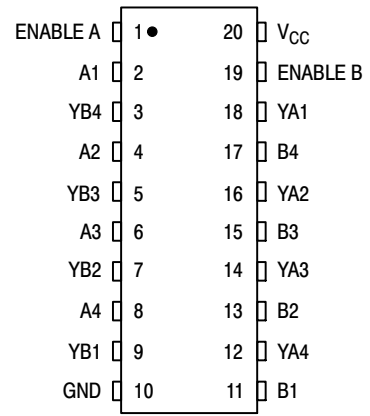


Figure 2. Pin Assignment

FUNCTION TABLE

| Inputs | | Output |
|----------|---|--------|
| Enable A | A | YA |
| L | L | L |
| L | H | H |
| H | X | Z |

| Inputs | | Output |
|----------|---|--------|
| Enable B | B | YB |
| H | L | L |
| H | H | H |
| L | X | Z |

Z = high impedance

X = don't care

MC74HCT241A

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit | |
|------------------|--|--|-----------------------------|------|
| V _{CC} | DC Supply Voltage | -0.5 to +6.5 | V | |
| V _{IN} | DC Input Voltage | -0.5 to V _{CC} +0.5 | V | |
| V _{OUT} | DC Output Voltage | -0.5 to V _{CC} +0.5 | V | |
| I _{IN} | DC Input Diode Current, per Pin | ±20 | mA | |
| I _{OUT} | DC Input Diode Current, Per Pin | ±35 | mA | |
| I _{CC} | DC Supply Current, V _{CC} and GND Pins | ±75 | mA | |
| I _{IK} | Input Clamp Current (V _{IN} < 0 or V _{IN} > V _{CC}) | ±20 | mA | |
| I _{OK} | Output Clamp Current (V _{OUT} < 0 or V _{OUT} > V _{CC}) | ±20 | mA | |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C | |
| T _L | Lead Temperature, 1 mm from Case for 10 secs | 260 | °C | |
| T _J | Junction Temperature Under Bias | +150 | °C | |
| θ _{JA} | Thermal Resistance (Note 1) | SOIC-20W WQFN20 QFN20 TSSOP-20 | 96 99 111 150 | °C/W |
| P _D | Power Dissipation in Still Air at 25°C | SOIC-20W WQFN20 QFN20 TSSOP-20 | 1302 1256 1127 833 | mW |
| MSL | Moisture Sensitivity | SOIC-20W All Other Packages | Level 3 Level 1 | - |
| F _R | Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in | - |
| V _{ESD} | ESD Withstand Voltage (Note 2) | Human Body Model Charged Device Model | > 2000 > 1000 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------------------------------|--|-----|-----------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | 4.5 | 5.5 | V |
| V _{in} , V _{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V _{CC} | V |
| T _A | Operating Temperature, All Package Types | -55 | +125 | °C |
| t _r , t _f | Input Rise and Fall Time | 0 | 500 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

MC74HCT241A

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|--|---|----------------------|------------------|------------|------------|------|
| | | | | -55 to 25°C | ≤ 85°C | ≤ 125°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA | 4.5 5.5 | 2 2 | 2 2 | 2 2 | V |
| V _{IL} | Maximum Low-Level Input Voltage | V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA | 4.5 5.5 | 0.8 0.8 | 0.8 0.8 | 0.8 0.8 | V |
| V _{OH} | Minimum High-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA | 4.5 5.5 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | V |
| | | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6 mA | 4.5 | 3.98 | 3.84 | 3.7 | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA | 4.5 5.5 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | V |
| | | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6 mA | 4.5 | 0.26 | 0.33 | 0.4 | |
| I _{in} | Maximum Input Leakage Current | V _{in} = V _{CC} or GND | 5.5 | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| I _{OZ} | Maximum Three-State Leakage Current | Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND | 5.5 | ± 0.5 | ± 5.0 | ± 10 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{in} = V _{CC} or GND I _{out} = 0 μA | 5.5 | 4 | 40 | 160 | μA |

| ΔI _{CC} | Additional Quiescent Supply Current | V _{in} = 2.4 V, Any One Input V _{in} = V _{CC} or GND, Other Inputs I _{out} = 0 μA | 5.5 | ≥ -55°C | 25°C to 125°C | mA |
|------------------|-------------------------------------|---|-----|---------|---------------|----|
| | | | | 2.9 | 2.4 | |
| | | | | | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Total Supply Current = I_{CC} + ΣΔI_{CC}.

AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Guaranteed Limit | | | Unit |
|--|---|------------------|--------|---------|------|
| | | -55 to 25°C | ≤ 85°C | ≤ 125°C | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3) | 23 | 29 | 35 | ns |
| t _{PLZ} , t _{PHZ} | Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4) | 30 | 38 | 45 | ns |
| t _{PZL} , t _{PZH} | Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4) | 26 | 33 | 39 | ns |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output (Figures 1 and 3) | 12 | 15 | 18 | ns |
| C _{in} | Maximum Input Capacitance | 10 | 10 | 10 | pF |
| C _{out} | Maximum Three-State Output Capacitance (Output in High-Impedance State) | 15 | 15 | 15 | pF |

| C _{PD} | Power Dissipation Capacitance (Per Enabled Output)* | Typical @ 25°C, V _{CC} = 5.0 V | | | pF |
|-----------------|---|---|--|--|----|
| | | 55 | | | |
| | | | | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}.

MC74HCT241A

SWITCHING WAVEFORMS

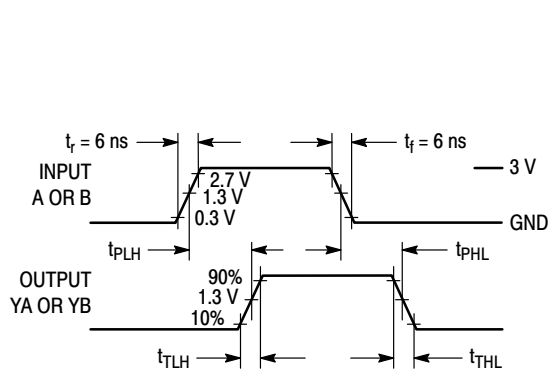


Figure 3.

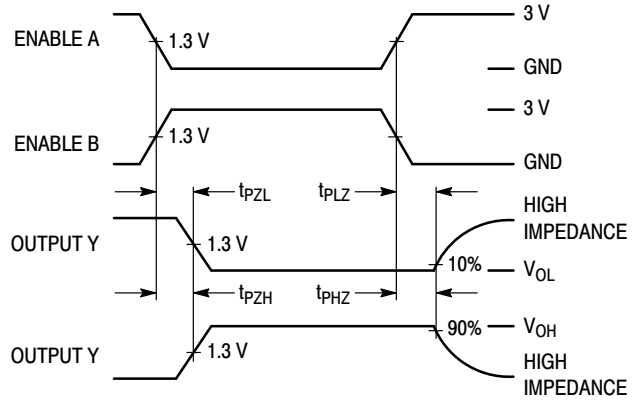
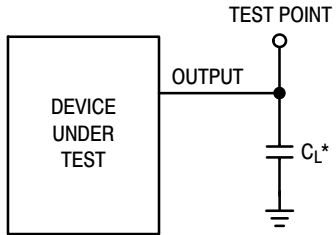
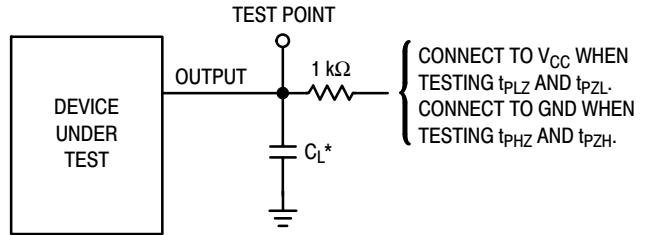


Figure 4.



*Includes all probe and jig capacitance

Figure 5. Test Circuit



*Includes all probe and jig capacitance

Figure 6. Test Circuit

MC74HCT241A

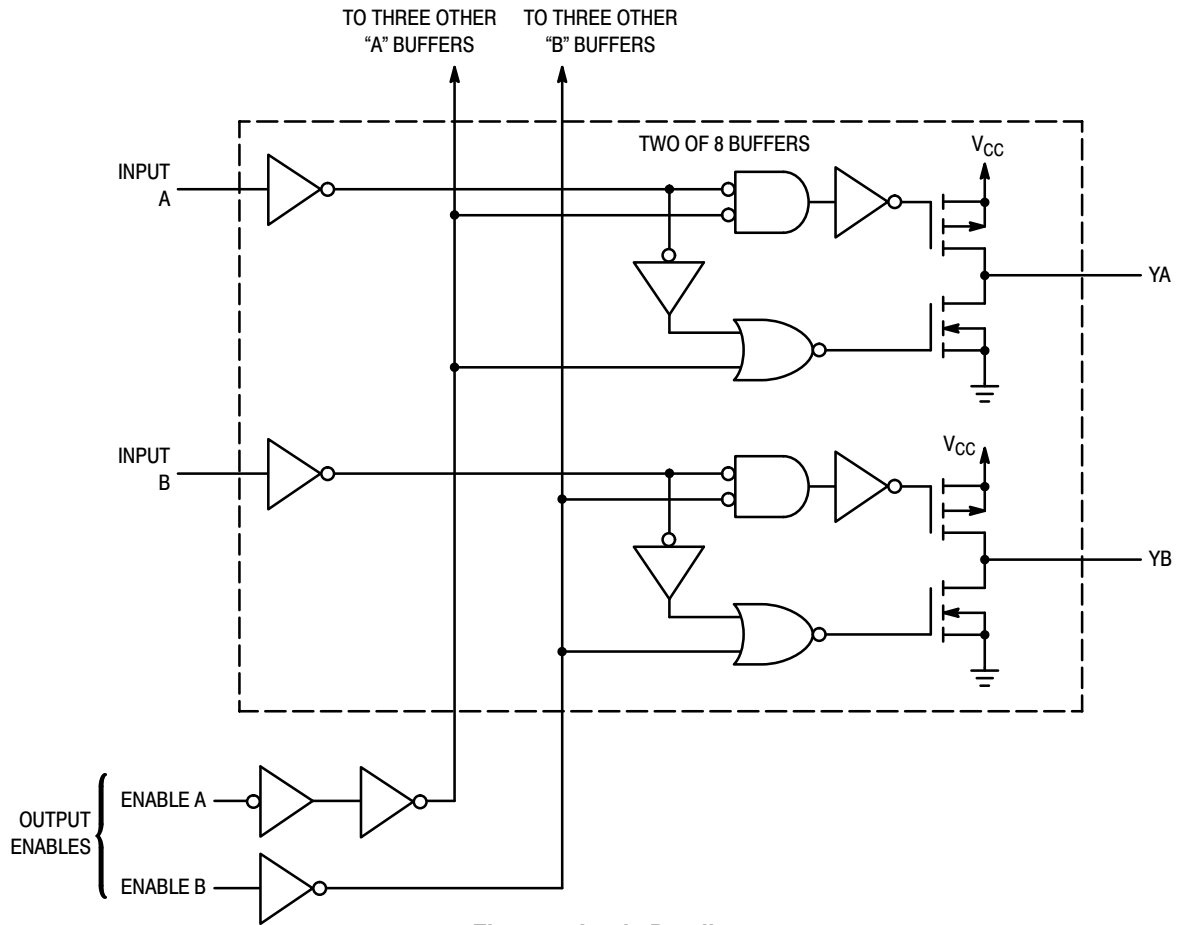


Figure 7. Logic Detail

ORDERING INFORMATION

| Device | Marking | Package | Shipping [†] |
|------------------|-------------|--------------|-----------------------|
| MC74HCT241ADWR2G | HCT241A | SOIC-20 Wide | 1000 / Tape & Reel |
| MC74HCT241ADTG | HCT 241A | TSSOP-20 | 75 Units / Rail |
| MC74HCT241ADTR2G | HCT 241A | TSSOP-20 | 2500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



TSSOP-20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

SCALE 2:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |



SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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