Hex 3-State Noninverting Buffer with Common Enables

High−Performance Silicon−Gate CMOS

MC74HC365A, MC74HCT365A

The MC74HC365A/MC74HCT365A is identical in pinout to the LS365. The MC74HC365A inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. The MC74HCT365A inputs are compatible with LSTTL outputs.

This device is a high−speed hex buffer with 3−state outputs and two common active−low Output Enables. When either of the enables is high, the buffer outputs are placed into high−impedance states. The HC365A, HCT365A has noninverting outputs.

Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V (HC), 4.5 to 5.5 V (HCT)
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 90 FETs or 22.5 Equivalent Gates
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant
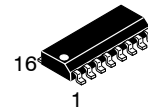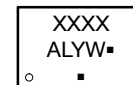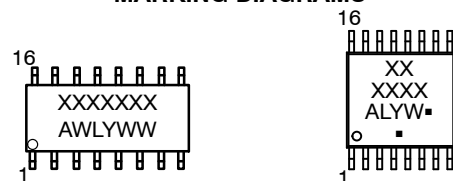
SOIC−16
D SUFFIX
CASE 751B
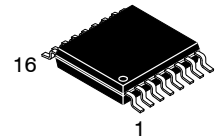
TSSOP−16
DT SUFFIX
CASE 948F

QFN16
MN SUFFIX
CASE 485AW

MARKING DIAGRAMS

XXXXXXX
AWLYWW

XX
XXXX
ALYW■

XXXX
ALYW■

A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ■	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

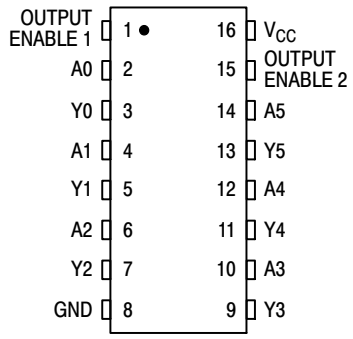See detailed ordering and shipping information on page 8 of this data sheet.

March, 2024 – Rev. 4

Publication Order Number:
MC74HC365A/D

MC74HC365A, MC74HCT365A

Figure 1. Pin Assignment

FUNCTION TABLE

Inputs			Output
Enable 1	Enable 2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

X = don't care
Z = high impedance

PIN 16 = V$_{CC}$
PIN 8 = GND
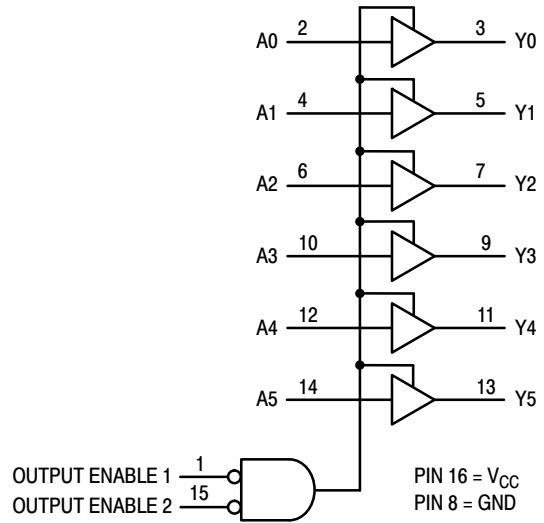
Figure 2. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to V_{CC} + 0.5	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} + 0.5	V
I_{IN}	DC Input Current, per Pin		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±50	mA
I_{IK}	Input Clamp Current (V_{IN} < 0 or V_{IN} > V_{CC})		±20	mA
I_{OK}	Output Clamp Current (V_{OUT} < 0 or V_{OUT} > V_{CC})		±20	mA
T_{STG}	Storage Temperature		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		±150	°C
θ_{JA}	Thermal Resistance (Note 1)	SOIC−16 QFN16 TSSOP−16	126 118 159	°C/W
P_D	Power Dissipation in Still Air at 25°C	SOIC−16 QFN16 TSSOP−16	995 1062 787	mW
MSL	Moisture Sensitivity		Level 1	–
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	–
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Measured with minimum pad spacing on an FR4 board, using 76 mm−by−114 mm, 2−ounce copper trace no air flow per JESD51−7.
2. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
MC74HC					
V_{CC}	DC Supply Voltage		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input, Output Voltage (Note 3)		0	V_{CC}	V
T_A	Operating Free−Air Temperature		−55	+125	°C
t_r, t_f	Input Rise or Fall Time	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns
MC74HCT					
V_{CC}	DC Supply Voltage		4.5	5.5	V
V_{IN}, V_{OUT}	DC Input, Output Voltage (Note 3)		0	V_{CC}	V
T_A	Operating Free−Air Temperature		−55	+125	°C
t_r, t_f	Input Rise or Fall Time		0	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

MC74HC365A, MC74HCT365A

DC ELECTRICAL CHARACTERISTICS (MC74HC365A)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				−55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High−Level Input Voltage	$V_{out} = V_{CC} − 0.1$ V $|I_{out}| \leq 20$ μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low−Level Input Voltage	$V_{out} = 0.1$ V $|I_{out}| \leq 20$ μA	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
V_{OH}	Minimum High−Level Output Voltage	$V_{in} = V_{IH}$ $|I_{out}| \leq 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ $|I_{out}| \leq 3.6$ mA $|I_{out}| \leq 6.0$ mA $|I_{out}| \leq 7.8$ mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low−Level Output Voltage	$V_{in} = V_{IL}$ $|I_{out}| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IL}$ $|I_{out}| \leq 3.6$ mA $|I_{out}| \leq 6.0$ mA $|I_{out}| \leq 7.8$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three−State Leakage Current	Output in High−Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μA	6.0	4	40	160	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (MC74HC365A)

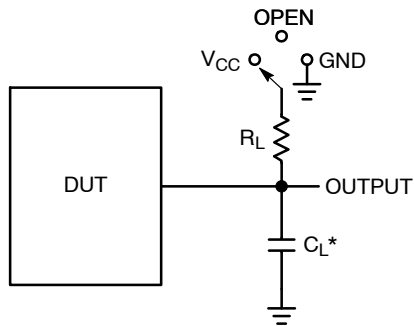| Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			−55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 3 and 4)	2.0 3.0 4.5 6.0	120 60 24 20	150 75 30 26	180 90 36 31	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 4)	2.0 3.0 4.5 6.0	220 110 44 37	275 140 55 47	330 170 66 56	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 4)	2.0 3.0 4.5 6.0	220 110 44 37	275 140 55 47	330 170 66 56	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 4)	2.0 3.0 4.5 6.0	60 22 12 10	75 28 15 13	90 34 18 15	ns
C_{in}	Maximum Input Capacitance	–	10	10	10	pF
C_{out}	Maximum Three−State Output Capacitance (Output in High−Impedance State)	–	15	15	15	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Buffer)*	60	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
*Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

MC74HC365A, MC74HCT365A

DC ELECTRICAL CHARACTERISTICS (MC74HCT365A)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				−55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High−Level Input Voltage	$V_{out} = V_{CC} - 0.1$ V $\|I_{out}\| \leq 20$ μA	4.5 to 5.5	2.0	2.0	2.0	V
V_{IL}	Maximum Low−Level Input Voltage	$V_{out} = 0.1$ V $\|I_{out}\| \leq 20$ μA	4.5 to 5.5	0.8	0.8	0.8	V
V_{OH}	Minimum High−Level Output Voltage	$V_{in} = V_{IH}$ $\|I_{out}\| \leq 20$ μA	4.5	4.4	4.4	4.4	V
		$V_{in} = V_{IH}$ $\|I_{out}\| \leq 6.0$ mA	4.5	3.98	3.84	3.70	
V_{OL}	Maximum Low−Level Output Voltage	$V_{in} = V_{IL}$ $\|I_{out}\| \leq 20$ μA	4.5	0.1	0.1	0.1	V
		$V_{in} = V_{IL}$ $\|I_{out}\| \leq 6.0$ mA	4.5	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	4.5	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three−State Leakage Current	Output in High−Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	4.5	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μA	4.5	4	40	160	μA

				≥ −55°C	25 to 125°C		
ΔI_{CC}	Additional Quiescent Supply Current	$V_{in} = 2.4$ V, Any One Input $V_{in} = V_{CC}$ or GND, Other Inputs $I_{out} = 0$ μA	5.5	2.9	2.4		mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (MC74HCT365A)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			−55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 3 and 4)	4.5	24	30	36	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 4)	4.5	44	55	66	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 4)	4.5	44	55	66	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 4)	4.5	12	15	18	ns
C_{in}	Maximum Input Capacitance	–	10	10	10	pF
C_{out}	Maximum Three−State Output Capacitance (Output in High−Impedance State)	–	15	15	15	pF

		Typical @ 25°C, $V_{CC} = 5.0$ V			
C_{PD}	Power Dissipation Capacitance (Per Buffer)*	60			pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
*Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
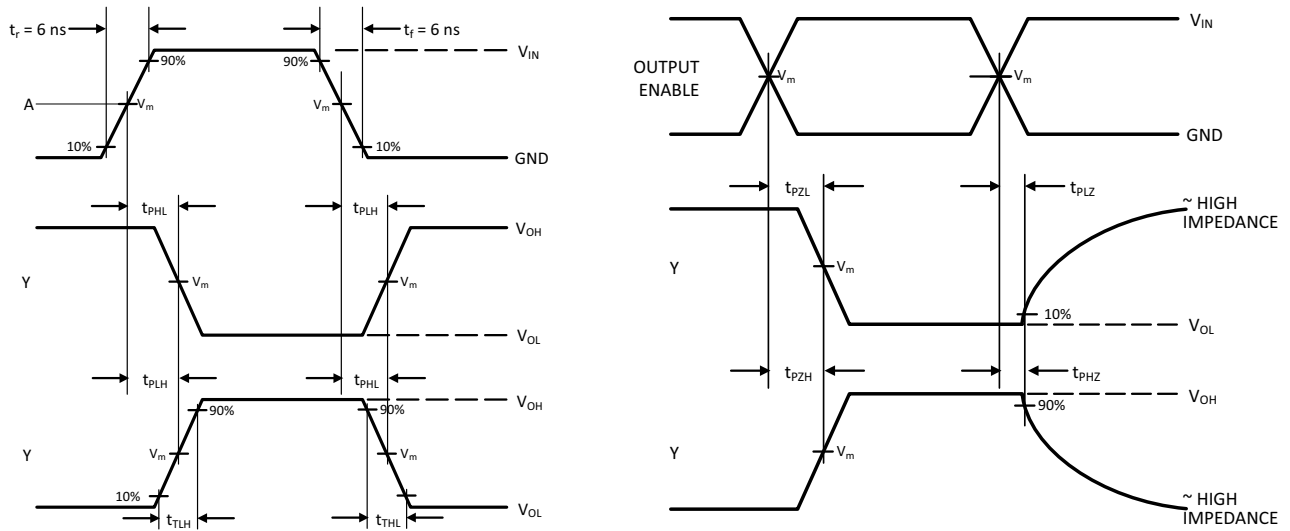
SWITCHING WAVEFORMS

*C_L Includes probe and jig capacitance

Test	Switch Position	C_L	R_L
t_{PLH} / t_{PHL}	Open	50 pF	1 kΩ
t_{PLZ} / t_{PZL}	V_{CC}		
t_{PHZ} / t_{PZH}	GND		

Figure 3. Test Circuit

Device	V_{IN}, V	V_m, V
MC74HC365A	V_{CC}	50% x V_{CC}
MC74HCT365A	3 V	1.3 V

Figure 4. Switching Waveforms
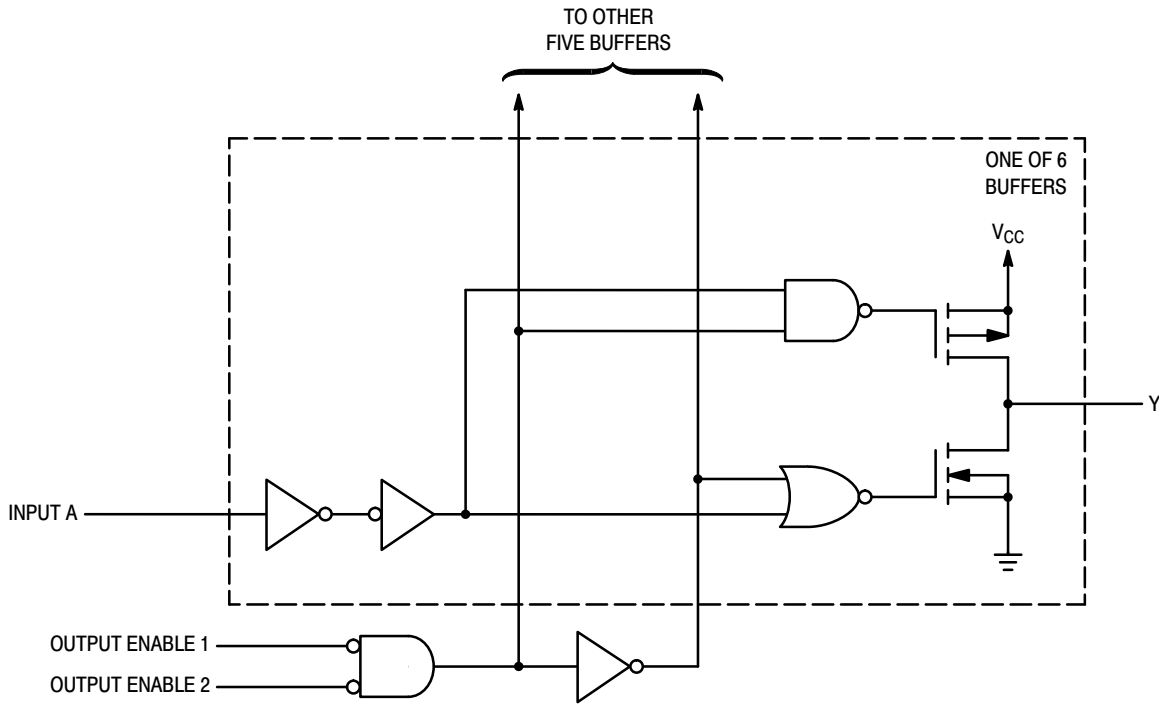
MC74HC365A, MC74HCT365A

TEST CIRCUITS

TO OTHER
FIVE BUFFERS

ONE OF 6
BUFFERS

V_{CC}

INPUT A

Y

OUTPUT ENABLE 1

OUTPUT ENABLE 2

Figure 5. Logic Detail

ORDERING INFORMATION

Device	Marking	Package	Shipping†
MC74HC365ADR2G	HC365AG	SOIC−16	2500 / Tape & Reel
MC74HC365ADTR2G	HC 365A	TSSOP−16	2500 / Tape & Reel
MC74HC365ADTR2G−Q*	HC 365A	TSSOP−16	2500 / Tape & Reel
MC74HCT365ADR2G	HCT365AG	SOIC−16	2500 / Tape & Reel
MC74HCT365ADTR2G	HCT 365A	TSSOP−16	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

MC74HC365A, MC74HCT365A

PACKAGE DIMENSIONS

SCALE 2:1

QFN16, 2.5x3.5, 0.5P
CASE 485AW
ISSUE O

DATE 11 DEC 2008

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
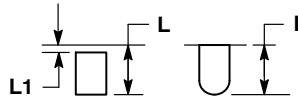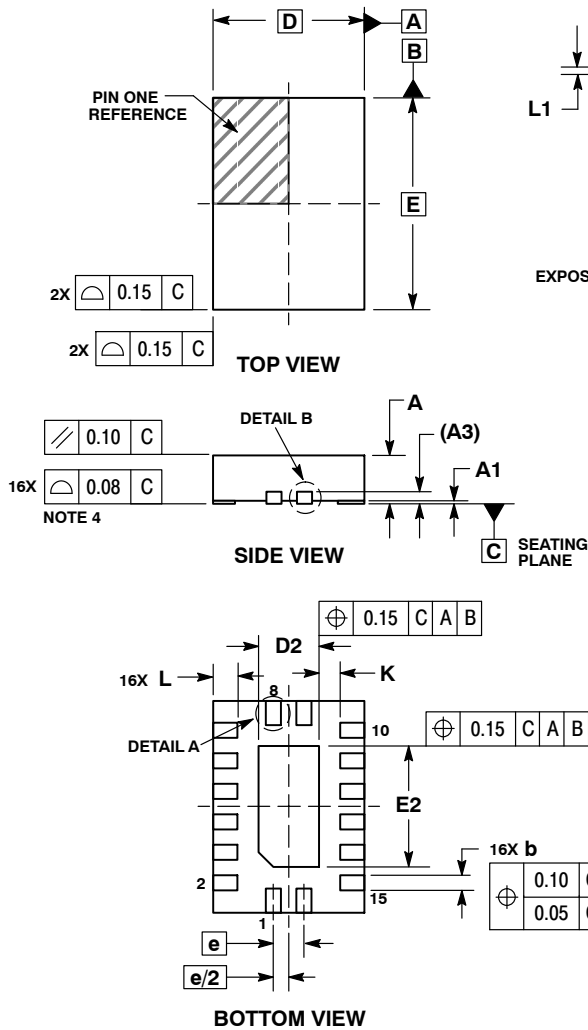
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS
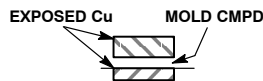
DETAIL B
ALTERNATE CONSTRUCTIONS

EXPOSED Cu   MOLD CMPD

TOP VIEW

PIN ONE REFERENCE

2X ⌒ 0.15 C

2X ⌒ 0.15 C

SIDE VIEW

DETAIL B

16X ⌒ 0.08 C
NOTE 4

∥ 0.10 C

C SEATING PLANE

BOTTOM VIEW

⊕ 0.15 C A B

16X L

DETAIL A

⊕ 0.15 C A B

16X b

| 0.10 | C | A | B |
| 0.05 | C | | |

NOTE 3

| DIM | MILLIMETERS | |
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.50 BSC	
D2	0.85	1.15
E	3.50 BSC	
E2	1.85	2.15
e	0.50 BSC	
K	0.20	---
L	0.35	0.45
L1	---	0.15

GENERIC MARKING DIAGRAM*
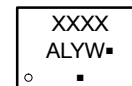
XXXX
ALYW▪

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*
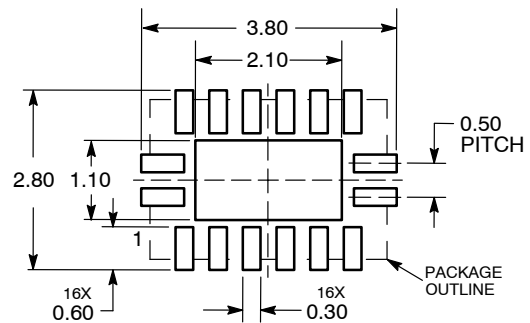
3.80
2.10
2.80   1.10
0.50 PITCH
1
16X 0.60
16X 0.30
PACKAGE OUTLINE

DIMENSIONS: MILLIMETERS

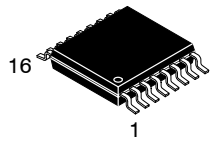*For additional information on our Pb–Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
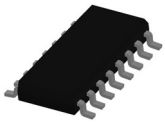
SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
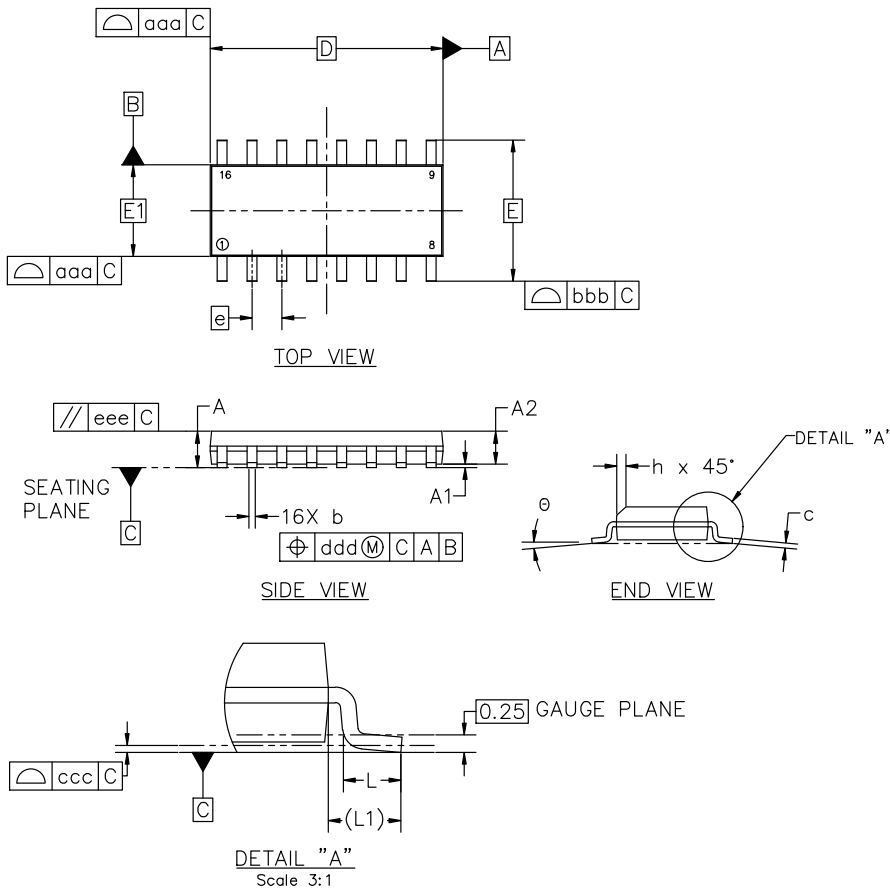
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	---	7°

TOLERANCE OF FORM AND POSITION	
aaa	0.10
bbb	0.20
ccc	0.10
ddd	0.25
eee	0.10

TOP VIEW

SIDE VIEW

END VIEW

DETAIL "A"

SEATING PLANE

h × 45°

DETAIL "A"
Scale 3:1

0.25 GAUGE PLANE
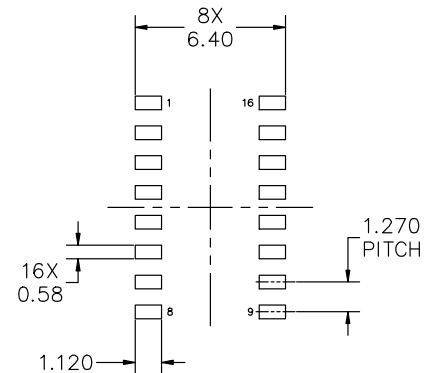
RECOMMENDED MOUNTING FOOTPRINT

8X 6.40

16X 0.58

1.270 PITCH

1.120

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOIC−16 9.90X3.90X1.50 1.27P		PAGE 1 OF 2

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

**GENERIC
MARKING DIAGRAM***


```
16  XXXXXXXXXXXXG
    XXXXXXXXXXXXX
1       AWLYWW
```
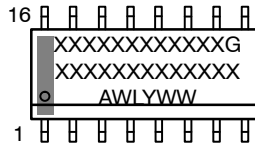
XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:	STYLE 2:	STYLE 3:	STYLE 4:
PIN 1. COLLECTOR	PIN 1. CATHODE	PIN 1. COLLECTOR, DYE #1	PIN 1. COLLECTOR, DYE #1
2. BASE	2. ANODE	2. BASE, #1	2. COLLECTOR, #1
3. EMITTER	3. NO CONNECTION	3. EMITTER, #1	3. COLLECTOR, #2
4. NO CONNECTION	4. CATHODE	4. COLLECTOR, #1	4. COLLECTOR, #2
5. EMITTER	5. CATHODE	5. COLLECTOR, #2	5. COLLECTOR, #3
6. BASE	6. NO CONNECTION	6. BASE, #2	6. COLLECTOR, #3
7. COLLECTOR	7. ANODE	7. EMITTER, #2	7. COLLECTOR, #4
8. COLLECTOR	8. CATHODE	8. COLLECTOR, #2	8. COLLECTOR, #4
9. BASE	9. CATHODE	9. COLLECTOR, #3	9. BASE, #4
10. EMITTER	10. ANODE	10. BASE, #3	10. EMITTER, #4
11. NO CONNECTION	11. NO CONNECTION	11. EMITTER, #3	11. BASE, #3
12. EMITTER	12. CATHODE	12. COLLECTOR, #3	12. EMITTER, #3
13. BASE	13. CATHODE	13. COLLECTOR, #4	13. BASE, #2
14. COLLECTOR	14. NO CONNECTION	14. BASE, #4	14. EMITTER, #2
15. EMITTER	15. ANODE	15. EMITTER, #4	15. BASE, #1
16. COLLECTOR	16. CATHODE	16. COLLECTOR, #4	16. EMITTER, #1

STYLE 5:	STYLE 6:	STYLE 7:
PIN 1. DRAIN, DYE #1	PIN 1. CATHODE	PIN 1. SOURCE N-CH
2. DRAIN, #1	2. CATHODE	2. COMMON DRAIN (OUTPUT)
3. DRAIN, #2	3. CATHODE	3. COMMON DRAIN (OUTPUT)
4. DRAIN, #2	4. CATHODE	4. GATE P-CH
5. DRAIN, #3	5. CATHODE	5. COMMON DRAIN (OUTPUT)
6. DRAIN, #3	6. CATHODE	6. COMMON DRAIN (OUTPUT)
7. DRAIN, #4	7. CATHODE	7. COMMON DRAIN (OUTPUT)
8. DRAIN, #4	8. CATHODE	8. SOURCE P-CH
9. GATE, #4	9. ANODE	9. SOURCE P-CH
10. SOURCE, #4	10. ANODE	10. COMMON DRAIN (OUTPUT)
11. GATE, #3	11. ANODE	11. COMMON DRAIN (OUTPUT)
12. SOURCE, #3	12. ANODE	12. COMMON DRAIN (OUTPUT)
13. GATE, #2	13. ANODE	13. GATE N-CH
14. SOURCE, #2	14. ANODE	14. COMMON DRAIN (OUTPUT)
15. GATE, #1	15. ANODE	15. COMMON DRAIN (OUTPUT)
16. SOURCE, #1	16. ANODE	16. SOURCE N-CH

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DESCRIPTION:	SOIC−16 9.90X3.90X1.50 1.27P		PAGE 2 OF 2

TSSOP−16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006

16

1

SCALE 2:1

16X **K** REF

⊕ 0.10 (0.004) Ⓜ T U Ⓢ V Ⓢ

⬠ 0.15 (0.006) T U Ⓢ

2X **L/2**

L

16   9

PIN 1
IDENT.

1   8

B
−U−

⬠ 0.15 (0.006) T U Ⓢ

A
−V−

K
K1

J1

SECTION N−N

J

N

0.25 (0.010)

M

N

F

DETAIL E

C

⬠ 0.10 (0.004)

−T− SEATING
PLANE

D   **G**   **H**

DETAIL E

−W−
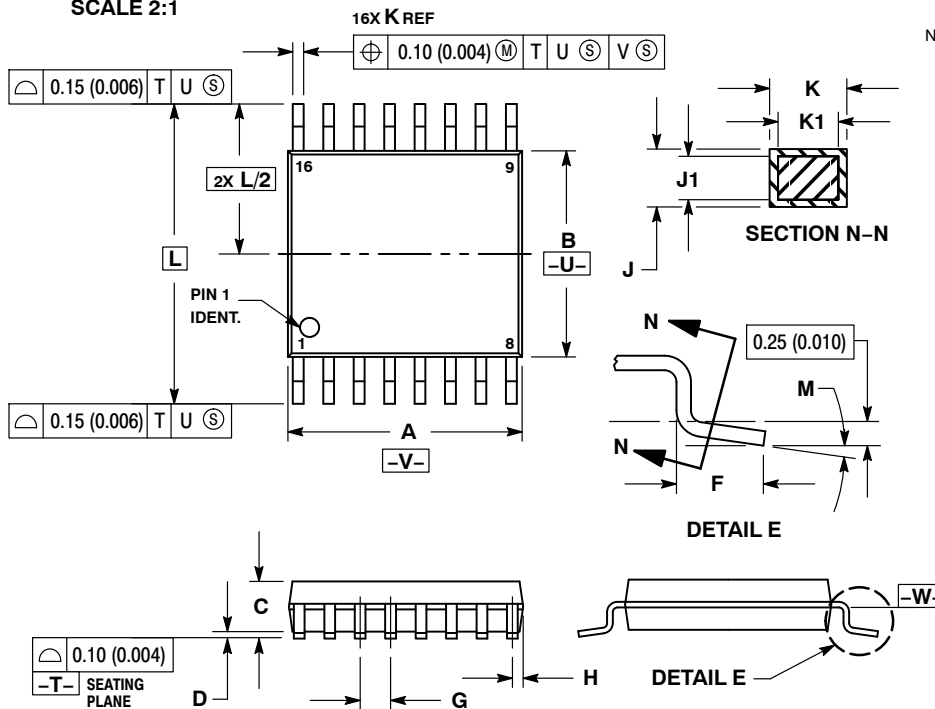
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| DIM | MILLIMETERS | | INCHES | |
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

**RECOMMENDED
SOLDERING FOOTPRINT***
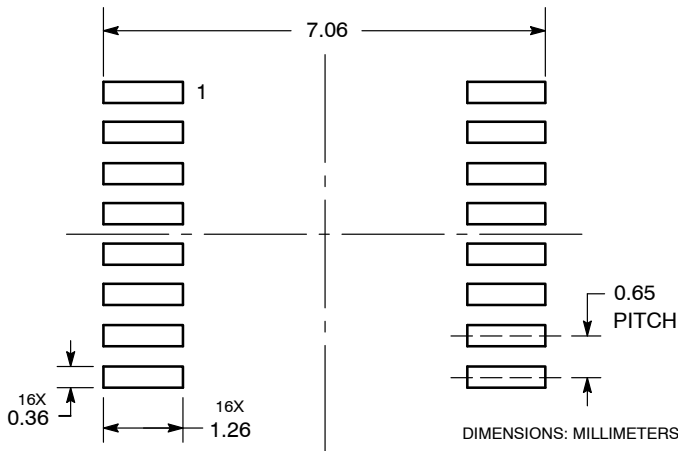
7.06

1

0.65
PITCH

16X
0.36

16X
1.26

DIMENSIONS: MILLIMETERS

**GENERIC
MARKING DIAGRAM***

16

XXXX
XXXX
ALYW

1
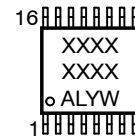
XXXX   = Specific Device Code
A   = Assembly Location
L   = Wafer Lot
Y   = Year
W   = Work Week
G or ▪   = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	TSSOP−16		PAGE 1 OF 1

ADDITIONAL INFORMATION

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