

8-Input Data Selector/ Multiplexer with 3-State Outputs

High-Performance Silicon-Gate CMOS

MC74HC251A

The MC74HC251 is identical in pinout to the LS251. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device selects one of the eight binary Data Inputs, as determined by the Address Inputs. The Output Enable pin must be a low level for the selected data to appear at the outputs. If Output Enable is high, both the Y and the \overline{Y} outputs are in the high-impedance state. This 3-state feature allows the HC251 to be used in bus-oriented systems.

The HC251 is similar in function to the HC251 which does not have 3-state outputs.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- –Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



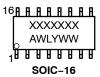


TSSOP-16 DT SUFFIX CASE 948F



QFN16 MN SUFFIX CASE 485AW

MARKING DIAGRAMS







XXXXXXX = Specific Device Code

A = Assembly Location

WL, L = Wafer Lot Y = Year WW, W = Work Week G or = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT

| D3 [| 1 ● | 16 |] V _C |
|---------------|-----|----|------------------|
| D2 [| 2 | 15 |] D4 |
| D1 [| 3 | 14 |] D5 |
| D0 [| 4 | 13 |] D6 |
| Υ[| 5 | 12 | D7 |
| ₹ [| 6 | 11 |] A0 |
| OUTPUT ENABLE | 7 | 10 |] A1 |
| GND [| 8 | 9 |] A2 |
| | | | |

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

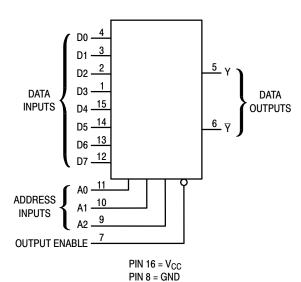


Figure 1. Logic Diagram

FUNCTION TABLE

| Inputs | | | Outputs | | |
|--------|------------|----|-------------------|---|---|
| A2 | A 1 | Α0 | Output Enabled | Υ | ¥ |
| X | X | X | H | Z D0 D1 D2 D3 D4 D5 D6 D7 | Z D0 D1 D2 D3 D4 D5 D6 D7 |

Z = high impedance

D0, D1, ..., D7 = the level of the respective D input.

MAXIMUM RATINGS

| Symbol | Parameter | | Value | Unit |
|------------------|--|--|------------------------------|------|
| V _{CC} | DC Supply Voltage | | -0.5 to +6.5 | V |
| V _{IN} | DC Input Voltage | | -0.5 to V _{CC} +0.5 | V |
| V _{OUT} | DC Output Voltage | | -0.5 to V _{CC} +0.5 | V |
| I _{IN} | DC Input Diode Current, per Pin | | ±20 | mA |
| I _{OUT} | DC Input Diode Current, Per Pin | | ±25 | mA |
| I _{CC} | DC Supply Current, V _{CC} and GND Pins | | ±50 | mA |
| I _{IK} | Input Clamp Current (V _{IN} < 0 or V _{IN} > V _{CC}) | | ±20 | mA |
| I _{OK} | Output Clamp Current (V _{OUT} < 0 or V _{OUT} > V _{CC}) | | ±20 | mA |
| T _{STG} | Storage Temperature Range | | −65 to +150 | °C |
| TL | Lead Temperature, 1 mm from Case for 10 secs | | 260 | °C |
| TJ | Junction Temperature Under Bias | | +150 | °C |
| θJA | Thermal Resistance (Note 1) | SOIC-16 QFN16 TSSOP-16 | 126 118 159 | °C/W |
| P _D | Power Dissipation in Still Air at 25°C | SOIC-16 QFN16 TSSOP-16 | 995 1062 787 | mW |
| MSL | Moisture Sensitivity | | Level 1 | = |
| F _R | Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in | - |
| V _{ESD} | ESD Withstand Voltage (Note 2) | Human Body Model Charged Device Model | 2000 N/A | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.

2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A.

⁽Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------------------------------|--|-----------------|--------------------|------|
| V _{CC} | DC Supply Voltage | 2.0 | 6.0 | V |
| V _{in} , V _{out} | DC Input Voltage, Output Voltage (Note 3) | 0 | V _{CC} | ٧ |
| T _A | Operating Temperature, All Package Types | - 55 | +125 | °C |
| t _r , t _f | Input Rise and Fall Time $ V_{CC} = 2.0 \ V_{CC} = 4.5 \ V_{CC} = 6.0 \ V_{CC} = 6.0 \ V_{CC} = 1.0 \ V_{CC} =$ | 0 0 0 | 1000 500 400 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

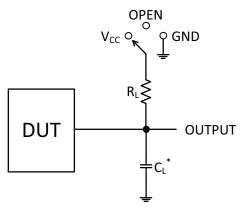
| | | | | Gu | aranteed Li | mit | |
|-----------------|---|--|----------------------|--------------------|--------------------|--------------------|------|
| Symbol | Parameter | Test Conditions | V _{CC} V | – 55 to 25°C | ≤ 85 °C | ≤ 125°C | Unit |
| V _{IH} | Minimum High-Level Input Voltage | V_{out} = 0.1 V or V_{CC} - 0.1 V $ I_{out} \le 20 \mu A$ | 2.0 4.5 6.0 | 1.5 3.15 4.2 | 1.5 3.15 4.2 | 1.5 3.15 4.2 | V |
| V _{IL} | Maximum Low-Level Input Voltage | V_{out} = 0.1 V or V_{CC} - 0.1 V $ I_{out} \le 20 \mu A$ | 2.0 4.5 6.0 | 0.3 0.9 1.2 | 0.3 0.9 1.2 | 0.3 0.9 1.2 | V |
| V _{OH} | Minimum High-Level Output Voltage | $V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 20 \mu\text{A}$ | 2.0 4.5 6.0 | 1.9 4.4 5.9 | 1.9 4.4 5.9 | 1.9 4.4 5.9 | V |
| | | $V_{in} = V_{IH} \text{ or } V_{IL} \qquad \begin{vmatrix} I_{out} \end{vmatrix} \le 4.0 \text{ mA} \\ I_{out} \le 5.2 \text{ mA} \end{vmatrix}$ | 4.5 6.0 | 3.98 5.48 | 3.84 5.34 | 3.70 5.20 | |
| V _{OL} | Maximum Low-Level Output Voltage | $V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 20 \mu\text{A}$ | 2.0 4.5 6.0 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V |
| | | $V_{in} = V_{IH} \text{ or } V_{IL} $ $ I_{out} \le 4.0 \text{ mA}$ $ I_{out} \le 5.2 \text{ mA}$ | 4.5 6.0 | 0.26 0.26 | 0.33 0.33 | 0.40 0.40 | |
| I _{in} | Maximum Input Leakage Current | V _{in} = V _{CC} or GND | 6.0 | ± 0.1 | ± 1.0 | ± 1.0 | μΑ |
| l _{OZ} | Maximum Three-State Leakage Current | Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$ | 6.0 | ± 0.5 | ± 5.0 | ± 10 | μΑ |
| Icc | Maximum Quiescent Supply Current (per Package) | $V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$ | 6.0 | 8 | 80 | 160 | μΑ |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

| | | | Gu | aranteed Li | mit | |
|--|---|-------------------|-----------------|-----------------|-----------------|------|
| Symbol | Parameter | V _{CC} | – 55 to 25°C | ≤ 85 °C | ≤ 125°C | Unit |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input D to Output Y or ₹ (Figures 2, 3, 4) | 2.0 4.5 6.0 | 185 37 31 | 230 46 39 | 280 56 48 | ns |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input A to Output Y or ₹ (Figures 2, 5) | 2.0 4.5 6.0 | 205 41 35 | 255 51 43 | 310 62 53 | ns |
| t _{PLZ} , t _{PHZ} | Maximum Propagation Delay, Output Enable to Output Y (Figures 5, 7) | 2.0 4.5 6.0 | 195 39 33 | 245 49 42 | 295 59 50 | ns |
| t _{PZL} , t _{PZH} | Maximum Propagation Delay, Output Enable to Output Y (Figures 2, 6) | 2.0 4.5 6.0 | 145 29 25 | 180 36 31 | 220 44 38 | ns |
| t _{PLZ} , t _{PHZ} | Maximum Propagation Delay, Output Enable to Output ₹ (Figures 2, 6) | 2.0 4.5 6.0 | 220 44 37 | 275 55 47 | 330 66 56 | ns |
| t _{PZL} , t _{PZH} | Maximum Propagation Delay, Output Enable to Output ₹ (Figures 2, 6) | 2.0 4.5 6.0 | 150 30 26 | 190 38 33 | 225 45 38 | ns |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output (Figures 2, 3, 4) | 2.0 4.5 6.0 | 75 15 13 | 95 19 16 | 110 22 19 | ns |
| C _{in} | Maximum Input Capacitance | - | 10 | 10 | 10 | pF |
| C _{out} | Maximum Three-State Output Capacitance (Output in High-Impedance State) | - | 15 | 15 | 15 | pF |

| | | Typical @ 25°C, V _{CC} = 5.0 V | |
|----------|---|---|----|
| C_{PD} | Power Dissipation Capacitance (Per Package) | 36 | pF |



| Test | Switch Position | CL | R _L |
|-------------------------------------|-----------------|-------|----------------|
| t _{PLH} / t _{PHL} | Open | 50 pF | 1 kΩ |
| t _{PLZ} / t _{PZL} | V _{CC} | | |
| t _{PHZ} / t _{PZH} | GND | | |

*C_L Includes probe and jig capacitance

Figure 2. Test Circuit

SWITCHING WAVEFORMS

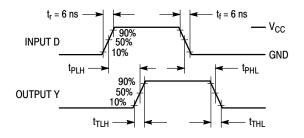


Figure 3.

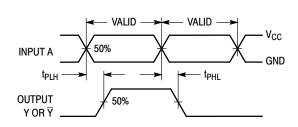


Figure 5.

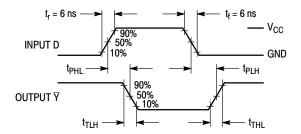


Figure 4.

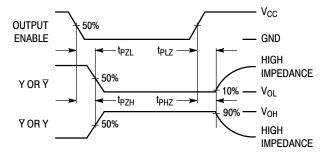


Figure 6.

PIN DESCRIPTIONS

ADDRESS INPUTS A0, A1, A2 (Pins 1, 2, 3)

Address inputs. These inputs, when the chip is selected, determine which of the eight outputs is active—low.

CONTROL INPUTS CS1, CS2, CS3 (Pins 6, 4, 5)

Chip select inputs. For CS1 at a high level and CS2, CS3 at a low level, the chip is selected and the outputs follow the

Address inputs. For any other combination of CS1, CS2, and CS3, the outputs are at a logic low.

OUTPUTS

Y0 - Y7 (Pins 15, 14, 13, 12, 11, 10, 9, 7)

Active-high Decoded outputs. These outputs assume a high level when addressed and the chip is selected. These outputs remain low when not addressed or the chip is not selected.

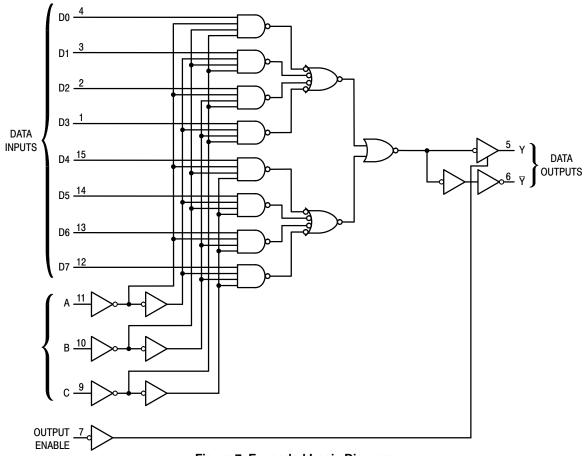


Figure 7. Expanded Logic Diagram

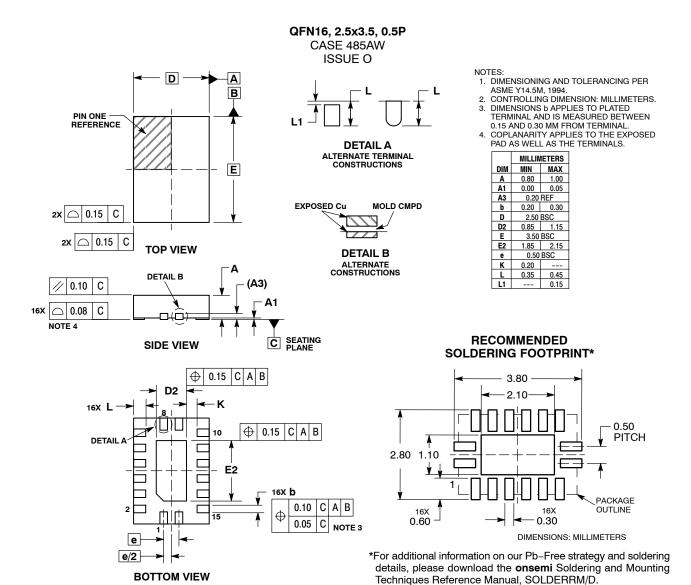
ORDERING INFORMATION

| CHDEHING IN CHIMAIICH | | | |
|-----------------------|------------|----------|--------------------------|
| Device | Marking | Package | Shipping [†] |
| MC74HC251ADG | HC251AG | SOIC-16 | 48 Units / Rail |
| MC74HC251ADR2G | HC251AG | SOIC-16 | 2500 Units / Tape & Reel |
| MC74HC251ADR2G-Q* | HC251AG | SOIC-16 | 2500 Units / Tape & Reel |
| MC74HC251ADTG | HC 251A | TSSOP-16 | 96 Units / Rail |
| MC74HC251ADTR2G | HC 251A | TSSOP-16 | 2500 Units / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{*-}Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

PACKAGE DIMENSIONS





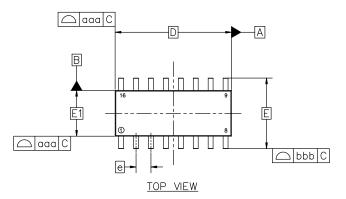


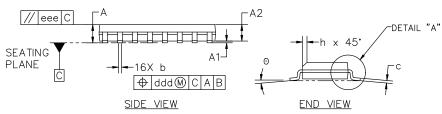
SOIC-16 9.90x3.90x1.50 1.27P CASE 751B ISSUE L

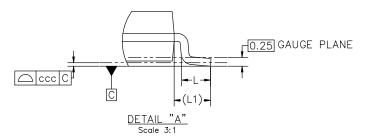
DATE 29 MAY 2024

NOTES:

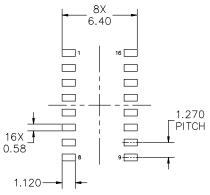
- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
- 2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
- 3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
- 4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
- DIMENSION 6 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE 6 DIMENSION AT MAXIMUM MATERIAL CONDITION.







| MILLIMETERS | | | | | |
|-------------|----------|----------|----------|--|--|
| DIM | MIN | NOM | MAX | | |
| А | 1.35 | 1.55 | 1.75 | | |
| A1 | 0.00 | 0.05 | 0.10 | | |
| A2 | 1.35 | 1.50 | 1.65 | | |
| b | 0.35 | 0.42 | 0.49 | | |
| С | 0.19 | 0.22 | 0.25 | | |
| D | 9.90 BSC | | | | |
| E | 6.00 BSC | | | | |
| E1 | 3.90 BSC | | | | |
| е | | 1.27 BSC | | | |
| h | 0.25 | | 0.50 | | |
| L | 0.40 | 0.83 | 1.25 | | |
| L1 | | 1.05 REF | | | |
| Θ | 0. | | 7° | | |
| TOLERAN | CE OF FC | RM AND | POSITION | | |
| aaa | | 0.10 | | | |
| bbb | | 0.20 | | | |
| ccc | | 0.10 | | | |
| ddd | | 0.25 | | | |
| eee | | 0.10 | | | |



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR
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AND MOUNTING TECHNIQUES REFERENCE
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| DESCRIPTION: | SOIC-16 9.90X3.90X1.50 1 | .27P | PAGE 1 OF 2 |

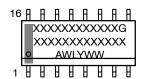
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SOIC-16 9.90x3.90x1.50 1.27P CASE 751B ISSUE L

DATE 29 MAY 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code

A = Assembly Location

WL = Wafer Lot
 Y = Year
 WW = Work Week
 G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

| 077/15/ | | 077/15.0 | | 071/15 0 | | T | |
|---|--|--|---|--|---|-------------------|------------------|
| STYLE 1: PIN 1. | COLLECTOR | STYLE 2: | CATHODE | STYLE 3: PIN 1. | | TYLE 4: PIN 1. | COLLECTOR DVF #1 |
| PIN 1. 2. | | PIN 1. 2. | | PIN 1. 2. | COLLECTOR, DYE #1 BASE, #1 | 2. | |
| 2. 3. | EMITTER | 2. 3. | NO CONNECTION | | | | |
| | | | | 3. | | 3. | |
| 4. | NO CONNECTION | 4. | | 4. | | 4. | |
| 5. | EMITTER | 5. | | 5. | | 5. | |
| 6. | BASE | 6. | | 6. | | 6. | |
| 7. | | 7. | | | EMITTER, #2 | | COLLECTOR, #4 |
| 8. | | 8. | | 8. | | | COLLECTOR, #4 |
| 9. | | 9. | | | COLLECTOR, #3 | | BASE, #4 |
| 10. | | | ANODE | | BASE, #3 | | EMITTER, #4 |
| | NO CONNECTION | 11. | | | EMITTER, #3 | | BASE, #3 |
| | EMITTER | | CATHODE | | COLLECTOR, #3 | | EMITTER, #3 |
| | BASE | | CATHODE | | COLLECTOR, #4 | | BASE, #2 |
| | COLLECTOR | 14. | | | BASE, #4 | | EMITTER, #2 |
| 15. | | | ANODE | | EMITTER, #4 | | BASE, #1 |
| 16. | COLLECTOR | 16. | CATHODE | 16. | COLLECTOR, #4 | 16. | EMITTER, #1 |
| | | | | | | | |
| | | | | | | | |
| STYLE 5: | | STYLE 6: | | STYLE 7: | | | |
| STYLE 5: PIN 1. | DRAIN, DYE #1 | STYLE 6: PIN 1. | CATHODE | STYLE 7: PIN 1. | SOURCE N-CH | | |
| | DRAIN, DYE #1 DRAIN, #1 | | | PIN 1. | SOURCE N-CH COMMON DRAIN (OUTPUT) | | |
| PIN 1. | , | PIN 1. | CATHODE | PIN 1. | COMMON DRAIN (OUTPUT) | | |
| PIN 1. 2. | DRAIN, #1 | PIN 1. 2. | CATHODE CATHODE | PIN 1. 2. | COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) | | |
| PIN 1. 2. 3. | DRAIN, #1 DRAIN, #2 | PIN 1. 2. 3. | CATHODE CATHODE | PIN 1. 2. 3. | COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) | | |
| PIN 1. 2. 3. 4. | DRAIN, #1 DRAIN, #2 DRAIN, #2 | PIN 1. 2. 3. 4. | CATHODE CATHODE CATHODE CATHODE | PIN 1. 2. 3. 4. | COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) | | |
| PIN 1. 2. 3. 4. 5. | DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 | PIN 1. 2. 3. 4. 5. | CATHODE CATHODE CATHODE CATHODE | PIN 1. 2. 3. 4. 5. | COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) | | |
| PIN 1. 2. 3. 4. 5. | DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 | PIN 1. 2. 3. 4. 5. | CATHODE CATHODE CATHODE CATHODE CATHODE | PIN 1. 2. 3. 4. 5. | COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) | | |
| PIN 1. 2. 3. 4. 5. 6. 7. | DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 | PIN 1. 2. 3. 4. 5. 6. | CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE | PIN 1. 2. 3. 4. 5. 6. | COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH | | |
| PIN 1. 2. 3. 4. 5. 6. 7. | DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 | PIN 1. 2. 3. 4. 5. 6. 7. | CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE | PIN 1. 2. 3. 4. 5. 6. 7. | COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH | | |
| PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. | DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 SOURCE, #4 | PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. | CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE ANODE | PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. | COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) | | |
| PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. | DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 GATE, #4 SOURCE, #4 GATE, #3 | PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. | CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE ANODE | PIN 1. 2. 3. 4. 5. 6. 7. 8. | COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) | | |
| PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. | DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 SOURCE, #4 | PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. | CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE ANODE ANODE ANODE ANODE ANODE ANODE | PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. | COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) | | |
| PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. | DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 GATE, #4 SOURCE, #4 GATE, #3 SOURCE, #3 GATE, #2 | PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. | CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE ANODE ANODE ANODE ANODE ANODE ANODE | PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. | COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GOMMON DRAIN (OUTPUT) GATE N-CH | | |
| PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. | DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 DRAIN, #4 GATE, #4 SOURCE, #4 GATE, #3 SOURCE, #3 GATE, #2 SOURCE, #2 SOURCE, #2 | PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. | CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE | PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13. | COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) CATE N-CH COMMON DRAIN (OUTPUT) | | |
| PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. | DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 GATE, #4 SOURCE, #4 GATE, #3 SOURCE, #3 GATE, #2 | PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13. | CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE | PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. | COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE N-CH COMMON DRAIN (OUTPUT) | | |

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|------------------|------------------------------|---|-------------|--|
| DESCRIPTION: | SOIC-16 9.90X3.90X1.50 1.27P | | PAGE 2 OF 2 | |

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2X L/2

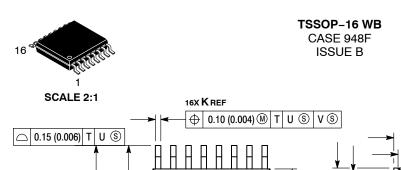
L

☐ 0.15 (0.006)

PIN 1 IDENT.

υ®





DATE 19 OCT 2006

NOTES

Κ

SECTION N-N

0.25 (0.010)

J1

В

-U-

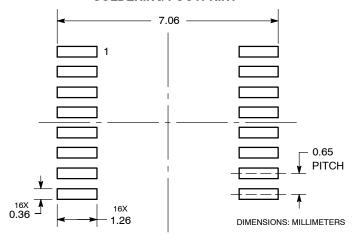
- DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT
- EXCEED 0.15 (0.006) PER SIDE.
 DIMENSION B DOES NOT INCLUDE
 INTERLEAD FLASH OR PROTRUSION.
- INTERLEAD FLASH OR PROTRUSION.
 INTERLEAD FLASH OR PROTRUSION SHALL
 NOT EXCEED 0.25 (0.010) PER SIDE.
 DIMENSION K DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABILE DAMBAR
 PROTRUSION SHALL BE 0.08 (0.003) TOTAL
 IN EXCESS OF THE K DIMENSION AT
 MAXIMUM MATERIAL CONDITION.
 TERMINIAL NILMBERS ADE SUCIUMI ECIP.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| DIM | MIN | MAX | MIN | MAX |
| Α | 4.90 | 5.10 | 0.193 | 0.200 |
| В | 4.30 | 4.50 | 0.169 | 0.177 |
| С | | 1.20 | | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| Н | 0.18 | 0.28 | 0.007 | 0.011 |
| 7 | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| М | 00 | 00 | 00 | 00 |

DETAIL E -W-☐ 0.10 (0.004) **DETAIL E** SEATING PLANE D

RECOMMENDED SOLDERING FOOTPRINT*

-V-



^{*}For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



= Specific Device Code XXXX Α = Assembly Location

= Wafer Lot L = Year W = Work Week G or • = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present. Some products may not follow the Generic Marking.

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