

Octal Transparent Latch with 3-State Outputs

MC74AC373, MC74ACT373

The MC74AC373/74ACT373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH, the bus output is in the high impedance state.

Features

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Outputs Source/Sink 24 mA
- 'ACT373 Has TTL Compatible Inputs
- These are Pb-Free Devices

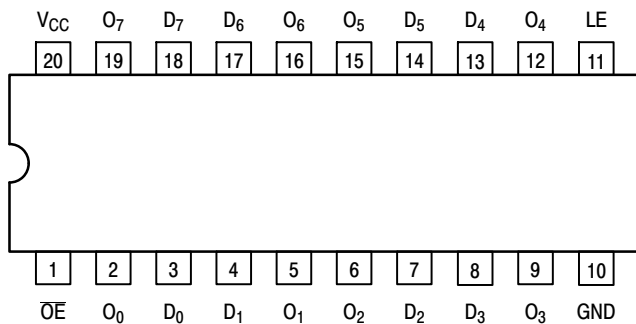


Figure 1. Pinout: 20-Lead Packages Conductors (Top View)

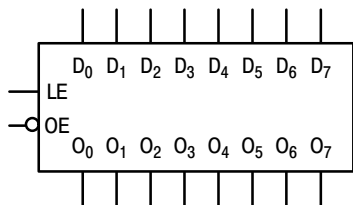
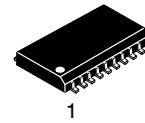


Figure 2. Logic Symbol

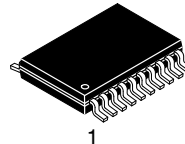
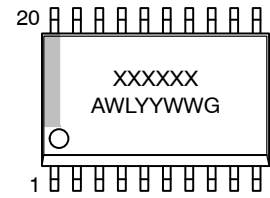
PIN ASSIGNMENT

| PIN | FUNCTION |
|--------------------------------|-----------------------|
| D ₀ -D ₇ | Data Inputs |
| LE | Latch Enable Input |
| \overline{OE} | Output Enable Input |
| O ₀ -O ₇ | 3-State Latch Outputs |

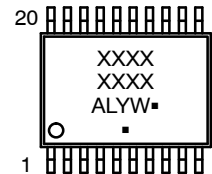
MARKING DIAGRAMS



1
SOIC-20W
DW SUFFIX
CASE 751D



1
TSSOP-20
DT SUFFIX
CASE 948E



XXXXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

MC74AC373, MC74ACT373

TRUTH TABLE

| Inputs | | | Outputs |
|-----------------|----|-------|---------|
| \overline{OE} | LE | D_n | O_n |
| H | X | X | Z |
| L | H | L | L |
| L | H | H | H |
| L | L | X | O_0 |

H = HIGH Voltage Level

L = LOW Voltage Level

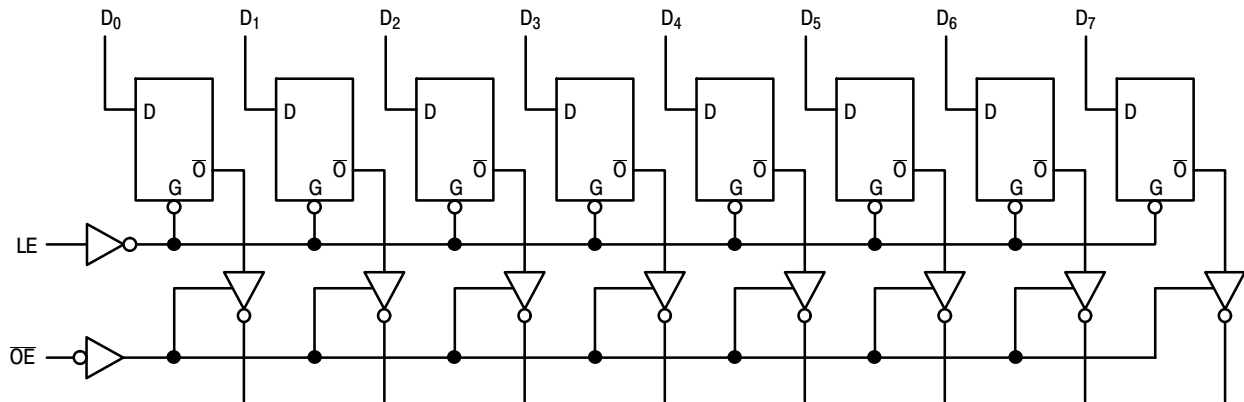
Z = High Impedance

X = Immaterial

O_0 = Previous O_0 before LOW-to-HIGH Transition of Clock

FUNCTIONAL DESCRIPTION

The MC74AC373/74ACT373 contains eight D-type latches with 3-state standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state standard outputs are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the standard outputs are in the 2-state mode. When \overline{OE} is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.



NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

MC74AC373, MC74ACT373

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|----------------------|---|--|-----------------------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +6.5 | V |
| V _{IN} | DC Input Voltage (Referenced to GND) | -0.5 to V _{CC} +0.5 | V |
| V _{OUT} | DC Output Voltage (Referenced to GND) (Note 1) | -0.5 to V _{CC} +0.5 | V |
| I _{IK} | DC Input Diode Current | ±20 | mA |
| I _{OK} | DC Output Diode Current | ±50 | mA |
| I _{OUT} | DC Output Sink/Source Current | ±50 | mA |
| I _{CC} | DC Supply Current, per Output Pin | ±50 | mA |
| I _{GND} | DC Ground Current, per Output Pin | ±100 | mA |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C |
| T _L | Lead temperature, 1 mm from Case for 10 Seconds | 260 | °C |
| T _J | Junction Temperature Under Bias | 140 | °C |
| θ _{JA} | Thermal Resistance (Note 2) | SOIC TSSOP 96 150 | °C/W |
| MSL | Moisture Sensitivity | SOIC TSSOP Level 3 Level 1 | |
| F _R | Flammability Rating | Oxygen Index: 30% – 35% | UL 94 V-0 @ 0.125 in |
| V _{ESD} | ESD Withstand Voltage | Human Body Model (Note 3) Charged Device Model (Note 4) | > 2000 > 1000 V |
| I _{Latchup} | Latchup Performance | Above V _{CC} and Below GND at 85°C (Note 5) | ±100 mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_{OUT} absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. Tested to EIA/JESD22-A114-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Typ | Max | Unit | |
|------------------------------------|---|-------------------------|-----|-----------------|------|------|
| V _{CC} | Supply Voltage | 'AC | 2.0 | 5.0 | 6.0 | V |
| | | 'ACT | 4.5 | 5.0 | 5.5 | |
| V _{IN} , V _{OUT} | DC Input Voltage, Output Voltage (Ref. to GND) | 0 | - | V _{CC} | V | |
| t _r , t _f | Input Rise and Fall Time (Note 6) 'AC Devices except Schmitt Inputs | V _{CC} @ 3.0 V | - | 150 | - | ns/V |
| | | V _{CC} @ 4.5 V | - | 40 | - | |
| | | V _{CC} @ 5.5 V | - | 25 | - | |
| t _r , t _f | Input Rise and Fall Time (Note 7) 'ACT Devices except Schmitt Inputs | V _{CC} @ 4.5 V | - | 10 | - | ns/V |
| | | V _{CC} @ 5.5 V | - | 8.0 | - | |
| T _A | Operating Ambient Temperature Range | -40 | 25 | 85 | °C | |
| I _{OH} | Output Current – High | - | - | -24 | mA | |
| I _{OL} | Output Current – Low | - | - | 24 | mA | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
7. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

MC74AC373, MC74ACT373

DC CHARACTERISTICS

| Symbol | Parameter | V _{CC} (V) | 74AC | | 74ACT | | Unit | Conditions |
|------------------|--------------------------------------|------------------------|------------------------|-------------------|------------------------------------|--|------|---|
| | | | T _A = +25°C | | T _A = -40°C to +85°C | | | |
| | | | Typ | Guaranteed Limits | | | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 | 1.5 | 2.1 | 2.1 | | V | V _{OUT} = 0.1 V or V _{CC} - 0.1 V |
| | | 4.5 | 2.25 | 3.15 | 3.15 | | | |
| | | 5.5 | 2.75 | 3.85 | 3.85 | | | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 | 1.5 | 0.9 | 0.9 | | V | V _{OUT} = 0.1 V or V _{CC} - 0.1 V |
| | | 4.5 | 2.25 | 1.35 | 1.35 | | | |
| | | 5.5 | 2.75 | 1.65 | 1.65 | | | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 | 2.99 | 2.9 | 2.9 | | V | I _{OUT} = -50 μA |
| | | 4.5 | 4.49 | 4.4 | 4.4 | | | |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | | |
| | | 3.0 | - | 2.56 | 2.46 | | V | *V _{IN} = V _{IL} or V _{IH} -12 mA I _{OH} -24 mA -24 mA |
| | | 4.5 | - | 3.86 | 3.76 | | | |
| | | 5.5 | - | 4.86 | 4.76 | | | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 | 0.002 | 0.1 | 0.1 | | V | I _{OUT} = 50 μA |
| | | 4.5 | 0.001 | 0.1 | 0.1 | | | |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | | |
| | | 3.0 | - | 0.36 | 0.44 | | V | *V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA |
| | | 4.5 | - | 0.36 | 0.44 | | | |
| | | 5.5 | - | 0.36 | 0.44 | | | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | - | ±0.1 | ±1.0 | | μA | V _I = V _{CC} , GND |
| I _{OZ} | Maximum 3-State Current | 5.5 | - | ±0.5 | ±5.0 | | μA | V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND |
| I _{OLD} | †Minimum Dynamic Output Current | 5.5 | - | - | 75 | | mA | V _{OLD} = 1.65 V Max |
| I _{OHD} | | 5.5 | - | - | -75 | | mA | V _{OHD} = 3.85 V Min |
| I _{CC} | Maximum Quiescent Supply Current | 5.5 | - | 8.0 | 80 | | μA | V _{IN} = V _{CC} or GND |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC373, MC74ACT373

AC CHARACTERISTICS (For Figures and Waveforms – See AND8277/D at www.onsemi.com)

| Symbol | Parameter | V _{CC} * (V) | 74AC | | | 74AC | | Unit | Fig. No. |
|------------------|---|--------------------------|--|------------|-------------|--|--------------|------|----------|
| | | | T _A = +25°C C _L = 50 pF | | | T _A = -40°C to +85°C C _L = 50 pF | | | |
| | | | Min | Typ | Max | Min | Max | | |
| t _{PLH} | Propagation Delay D _n to O _n | 3.3 5.0 | 1.5 1.5 | 10 7.0 | 13.5 9.5 | 1.5 1.5 | 15 10.5 | ns | 3-5 |
| t _{PHL} | Propagation Delay D _n to O _n | 3.3 5.0 | 1.5 1.5 | 9.5 7.0 | 13 9.5 | 1.5 1.5 | 14.5 10.5 | ns | 3-5 |
| t _{PLH} | Propagation Delay LE to O _n | 3.3 5.0 | 1.5 1.5 | 10 7.5 | 13.5 9.5 | 1.5 1.5 | 15 10.5 | ns | 3-6 |
| t _{PHL} | Propagation Delay LE to O _n | 3.3 5.0 | 1.5 1.5 | 9.5 7.0 | 12.5 9.5 | 1.5 1.5 | 14 10.5 | ns | 3-6 |
| t _{PZH} | Output Enable Time | 3.3 5.0 | 1.5 1.5 | 9.0 7.0 | 11.5 8.5 | 1.0 1.0 | 13 9.5 | ns | 3-7 |
| t _{PZL} | Output Enable Time | 3.3 5.0 | 1.5 1.5 | 8.5 6.5 | 11.5 8.5 | 1.0 1.0 | 13 9.5 | ns | 3-8 |
| t _{PHZ} | Output Disable Time | 3.3 5.0 | 1.5 1.5 | 10 8.0 | 12.5 11 | 1.0 1.0 | 14.5 12.5 | ns | 3-7 |
| t _{PLZ} | Output Disable Time | 3.3 5.0 | 1.5 1.5 | 8.0 6.5 | 11.5 8.5 | 1.0 1.0 | 12.5 10 | ns | 3-8 |

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

| Symbol | Parameter | V _{CC} * (V) | 74AC | | 74AC | | Unit | Fig. No. |
|----------------|---|--------------------------|--|--------------------|--|--|------|----------|
| | | | T _A = +25°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | | |
| | | | Typ | Guaranteed Minimum | | | | |
| t _s | Setup Time, HIGH or LOW D _n to LE | 3.3 5.0 | 3.5 2.0 | 5.5 4.0 | 6.0 4.5 | | ns | 3-9 |
| t _h | Hold Time, HIGH or LOW D _n to LE | 3.3 5.0 | -3.0 -1.5 | 1.0 1.0 | 1.0 1.0 | | ns | 3-9 |
| t _w | LE Pulse Width, HIGH | 3.3 5.0 | 4.0 2.0 | 5.5 4.0 | 6.0 4.5 | | ns | 3-6 |

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74AC373, MC74ACT373

DC CHARACTERISTICS

| Symbol | Parameter | V _{CC} (V) | 74ACT | | 74ACT | | Unit | Conditions |
|-------------------|--|------------------------|------------------------|-------------------|------------------------------------|--|------|---|
| | | | T _A = +25°C | | T _A = -40°C to +85°C | | | |
| | | | Typ | Guaranteed Limits | | | | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 | 1.5 | 2.0 | 2.0 | | V | V _{OUT} = 0.1 V or V _{CC} - 0.1 V |
| | | 5.5 | 1.5 | 2.0 | 2.0 | | | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 | 1.5 | 0.8 | 0.8 | | V | V _{OUT} = 0.1 V or V _{CC} - 0.1 V |
| | | 5.5 | 1.5 | 0.8 | 0.8 | | | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | | V | I _{OUT} = -50 μA |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | | |
| | | 4.5 | - | 3.86 | 3.76 | | | |
| 5.5 | - | 4.86 | 4.76 | | | | | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | | V | I _{OUT} = 50 μA |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | | |
| | | 4.5 | - | 0.36 | 0.44 | | | |
| 5.5 | - | 0.36 | 0.44 | | | | | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | - | ±0.1 | ±1.0 | | μA | V _I = V _{CC} , GND |
| ΔI _{CCT} | Additional Max. I _{CC} /Input | 5.5 | 0.6 | - | 1.5 | | mA | V _I = V _{CC} - 2.1 V |
| I _{OZ} | Maximum 3-State Current | 5.5 | - | ±0.5 | ±5.0 | | μA | V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND |
| I _{OLD} | †Minimum Dynamic Output Current | 5.5 | - | - | 75 | | mA | V _{OLD} = 1.65 V Max |
| I _{OHD} | | 5.5 | - | - | -75 | | mA | V _{OHD} = 3.85 V Min |
| I _{CC} | Maximum Quiescent Supply Current | 5.5 | - | 8.0 | 80 | | μA | V _{IN} = V _{CC} or GND |

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

MC74AC373, MC74ACT373

AC CHARACTERISTICS (For Figures and Waveforms – See AND8277/D at www.onsemi.com)

| Symbol | Parameter | V _{CC} * (V) | 74ACT | | | 74ACT | | Unit | Fig. No. |
|------------------|---|--------------------------|--|-----|-----|--|------|------|----------|
| | | | T _A = +25°C C _L = 50 pF | | | T _A = -40°C to +85°C C _L = 50 pF | | | |
| | | | Min | Typ | Max | Min | Max | | |
| t _{PLH} | Propagation Delay D _n to O _n | 5.0 | 2.5 | 8.5 | 10 | 1.5 | 11.5 | ns | 3-5 |
| t _{PHL} | Propagation Delay D _n to O _n | 5.0 | 2.0 | 8.0 | 10 | 1.5 | 11.5 | ns | 3-5 |
| t _{PLH} | Propagation Delay LE to O _n | 5.0 | 2.5 | 8.5 | 11 | 2.0 | 11.5 | ns | 3-6 |
| t _{PHL} | Propagation Delay LE to O _n | 5.0 | 2.0 | 8.0 | 10 | 1.5 | 11.5 | ns | 3-6 |
| t _{PZH} | Output Enable Time | 5.0 | 2.0 | 8.0 | 9.5 | 1.5 | 10.5 | ns | 3-7 |
| t _{PZL} | Output Enable Time | 5.0 | 2.0 | 7.5 | 9.0 | 1.5 | 10.5 | ns | 3-8 |
| t _{PHZ} | Output Disable Time | 5.0 | 2.5 | 9.0 | 11 | 2.5 | 12.5 | ns | 3-7 |
| t _{PLZ} | Output Disable Time | 5.0 | 1.5 | 7.5 | 8.5 | 1.0 | 10 | ns | 3-8 |

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS (For Figures and Waveforms – See AND8277/D at www.onsemi.com)

| Symbol | Parameter | V _{CC} * (V) | 74ACT | | 74ACT | | Unit | Fig. No. |
|----------------|---|--------------------------|--|--------------------|--|----|------|----------|
| | | | T _A = +25°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | | |
| | | | Typ | Guaranteed Minimum | | | | |
| t _s | Setup Time, HIGH or LOW D _n to LE | 5.0 | 3.0 | 7.0 | 8.0 | ns | 3-9 | |
| t _h | Hold Time, HIGH or LOW D _n to LE | 5.0 | 0 | 0 | 1.0 | ns | 3-9 | |
| t _w | LE Pulse Width, HIGH | 5.0 | 2.0 | 7.0 | 8.0 | ns | 3-6 | |

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

| Symbol | Parameter | Value Typ | Unit | Test Conditions |
|-----------------|-------------------------------|--------------|------|-------------------------|
| C _{IN} | Input Capacitance | 4.5 | pF | V _{CC} = 5.0 V |
| C _{PD} | Power Dissipation Capacitance | 40 | pF | V _{CC} = 5.0 V |

MC74AC373, MC74ACT373

ORDERING INFORMATION

| Device | Marking | Package | Shipping [†] |
|-----------------|------------|----------|-----------------------|
| MC74AC373DWG | AC373 | SOIC-20 | 38 Units / Rail |
| MC74AC373DWR2G | AC373 | SOIC-20 | 1000 / Tape & Reel |
| MC74ACT373DWG | ACT373 | SOIC-20 | 38 Units / Rail |
| MC74ACT373DWR2G | ACT373 | SOIC-20 | 1000 / Tape & Reel |
| MC74AC373DTR2G | AC 373 | TSSOP-20 | 2500 / Tape & Reel |
| MC74ACT373DTR2G | ACT 373 | TSSOP-20 | 2500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

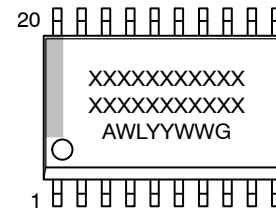
RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|------------------|-------------|--|
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| DESCRIPTION: | SOIC-20 WB | PAGE 1 OF 1 |

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

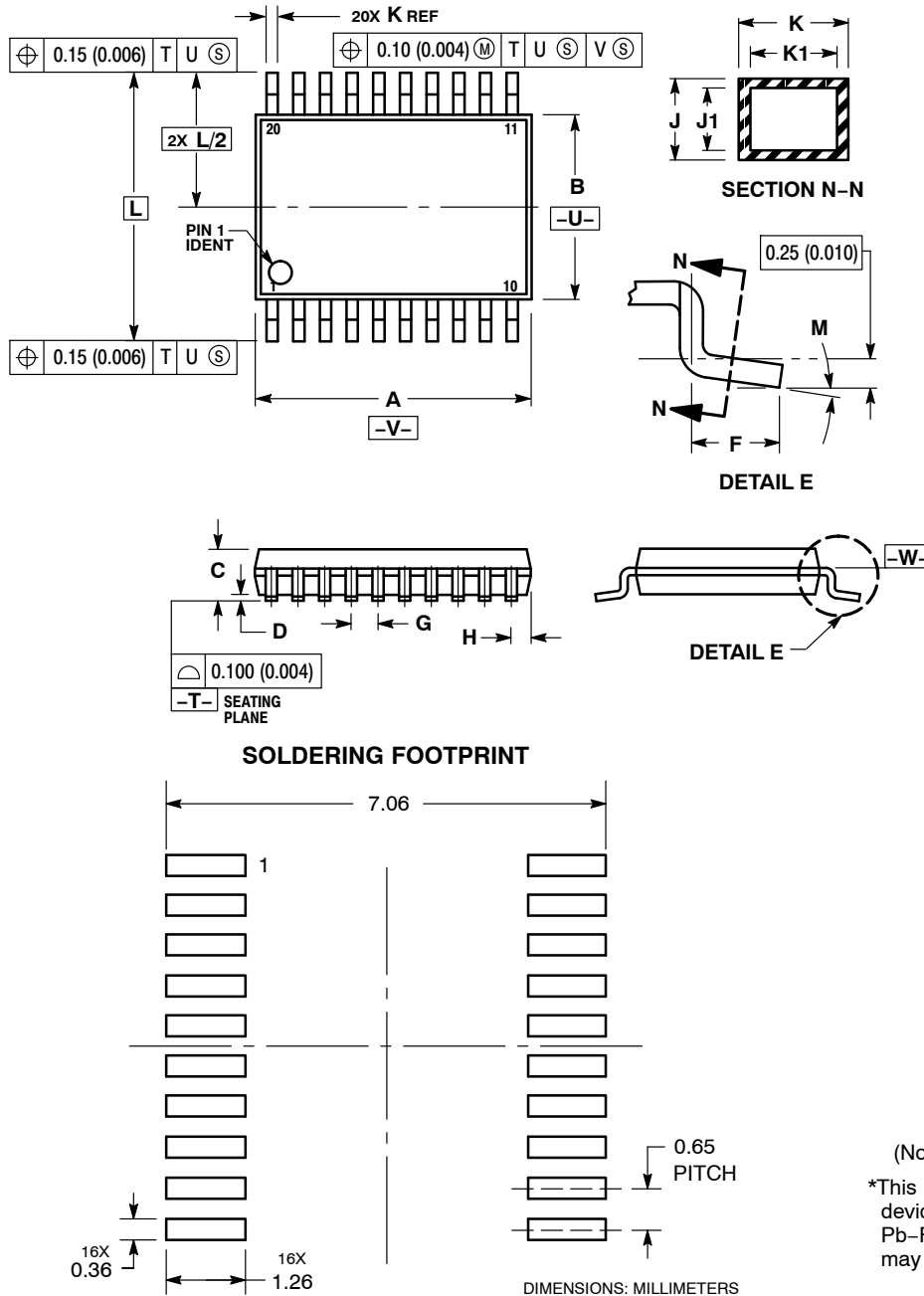
ON Semiconductor®



TSSOP-20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

SCALE 2:1

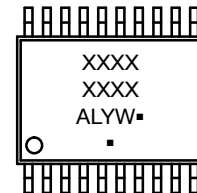


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

| | | |
|-------------------------|--------------------|--|
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