

MC14572UB

Hex Gate

The MC14572UB hex functional gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. The chip contains four inverters, one NOR gate and one NAND gate.

Features

- Diode Protection on All Inputs
- Single Supply Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- NOR Input Pin Adjacent to V_{SS} Pin to Simplify Use As An Inverter
- NAND Input Pin Adjacent to V_{DD} Pin to Simplify Use As An Inverter
- NOR Output Pin Adjacent to Inverter Input Pin For OR Application
- NAND Output Pin Adjacent to Inverter Input Pin For AND Application
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable*
- This Device is Pb-Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

| Parameter | Symbol | Value | Unit |
|---|-------------------|---------------------------|------|
| DC Supply Voltage Range | V_{DD} | -0.5 to +18.0 | V |
| Input or Output Voltage Range (DC or Transient) | V_{in}, V_{out} | -0.5 to V_{DD} + 0.5 | V |
| Input or Output Current (DC or Transient) per Pin | I_{in}, I_{out} | ±10 | mA |
| Power Dissipation, per Package (Note 1) | P_D | 500 | mW |
| Ambient Temperature Range | T_A | -55 to +125 | °C |
| Storage Temperature Range | T_{stg} | -65 to +150 | °C |
| Lead Temperature (8-Second Soldering) | T_L | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Package: -7.0 mW/°C From 65°C To 125°C

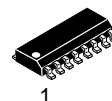
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



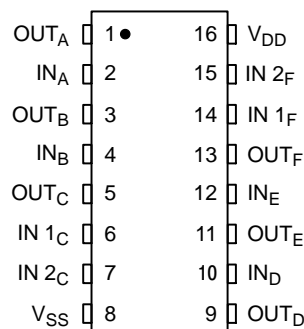
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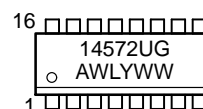


SOIC-16
D SUFFIX
CASE 751B

PIN ASSIGNMENT



MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

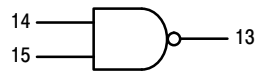
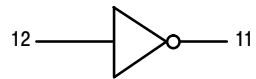
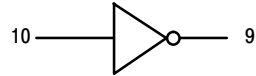
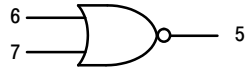
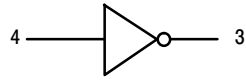
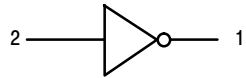
ORDERING INFORMATION

| Device | Package | Shipping† |
|-----------------|-------------------|------------------|
| MC14572UBDG | SOIC-16 (Pb-Free) | 48 Units / Rail |
| MC14572UBDR2G | SOIC-16 (Pb-Free) | 2500/Tape & Reel |
| NLV14572UBDR2G* | SOIC-16 (Pb-Free) | 2500/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

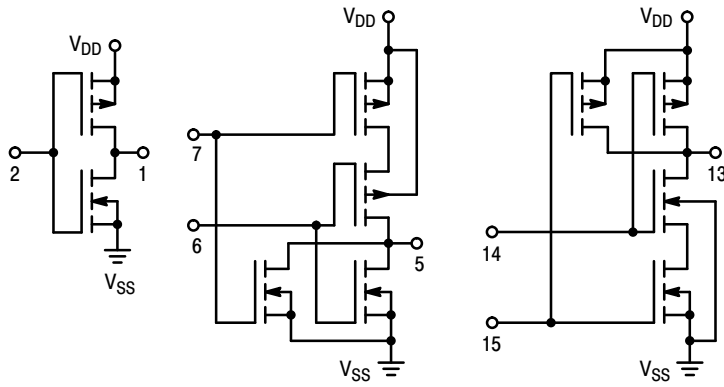
MC14572UB

LOGIC DIAGRAM



V_{DD} = PIN 16
 V_{SS} = PIN 8

CIRCUIT SCHEMATIC



MC14572UB

SWITCHING CHARACTERISTICS (Type 5) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

| Characteristic | Symbol | V_{DD} | Min | Typ (Note 6) | Max | Unit |
|--|-------------------------|-----------------|-------------|-----------------|-------------------|------|
| Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$ | t_{TLH} | 5.0 10 15 | – – – | 180 90 65 | 360 180 130 | ns |
| Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$ | t_{THL} | 5.0 10 15 | – – – | 100 50 40 | 200 100 80 | ns |
| Propagation Delay Time $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 5 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 17 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ | $t_{PLH},$ t_{PHL} | 5.0 10 15 | – – – | 90 50 40 | 180 100 80 | ns |

5. The formulas given are for the typical characteristics only at 25°C .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

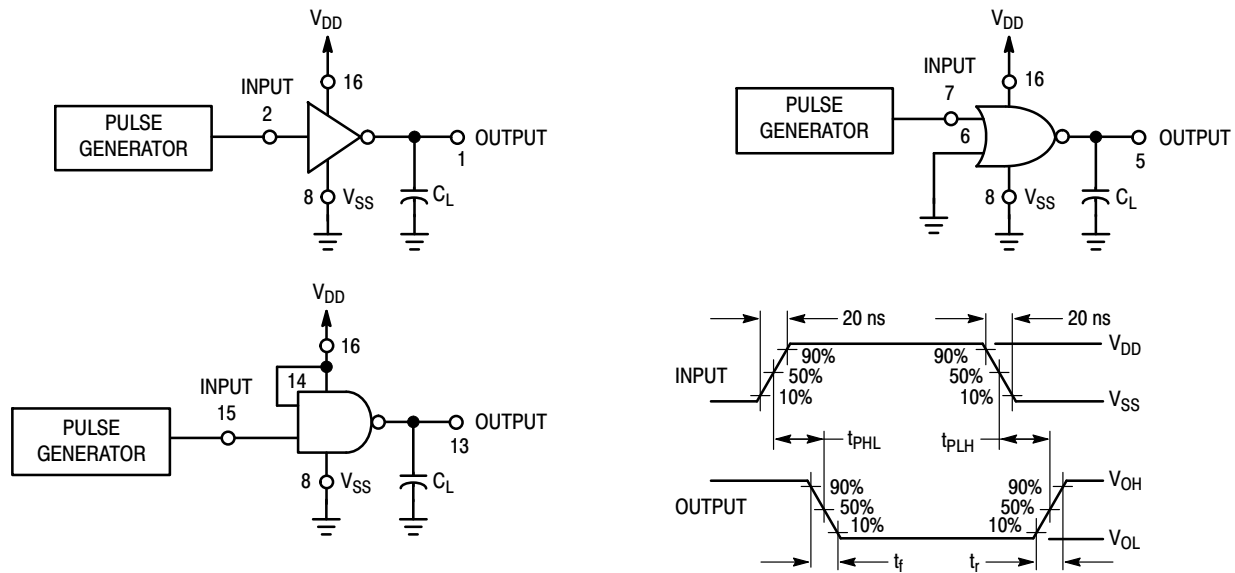
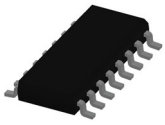


Figure 1. Switching Time Test Circuits and Waveforms

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

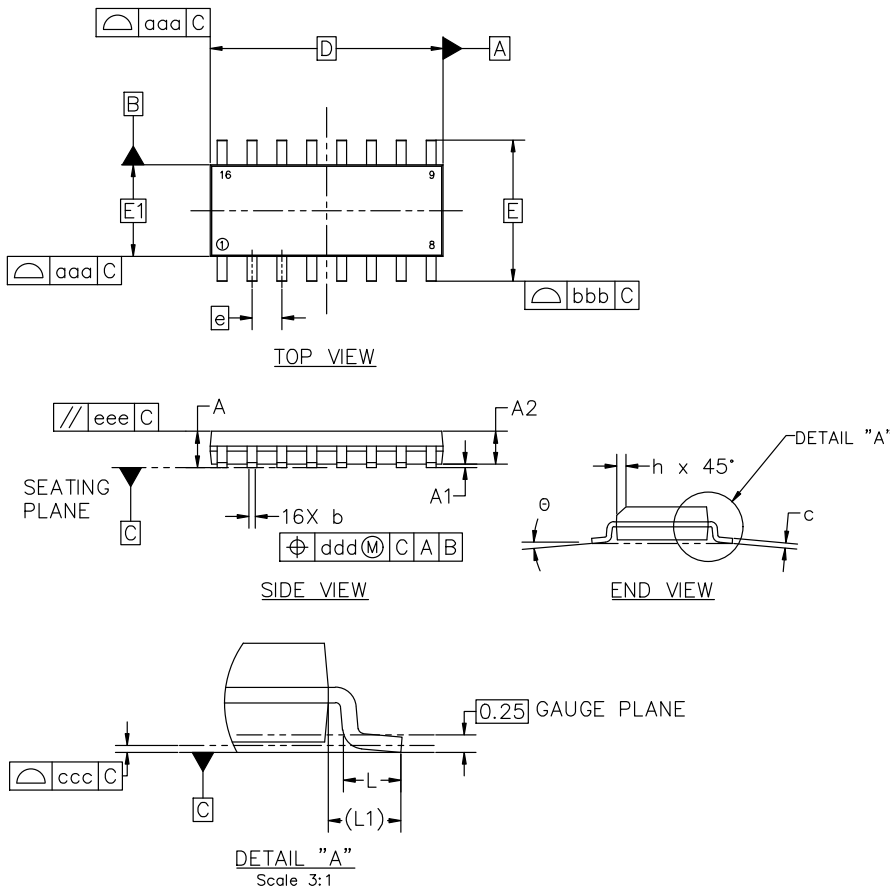


SOIC-16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

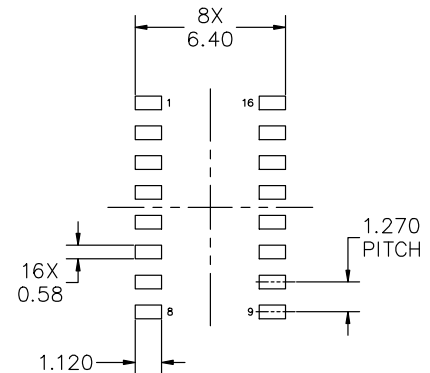
DATE 29 MAY 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



| MILLIMETERS | | | |
|--------------------------------|----------|------|------|
| DIM | MIN | NOM | MAX |
| A | 1.35 | 1.55 | 1.75 |
| A1 | 0.00 | 0.05 | 0.10 |
| A2 | 1.35 | 1.50 | 1.65 |
| b | 0.35 | 0.42 | 0.49 |
| c | 0.19 | 0.22 | 0.25 |
| D | 9.90 BSC | | |
| E | 6.00 BSC | | |
| E1 | 3.90 BSC | | |
| e | 1.27 BSC | | |
| h | 0.25 | --- | 0.50 |
| L | 0.40 | 0.83 | 1.25 |
| L1 | 1.05 REF | | |
| θ | 0° | --- | 7° |
| TOLERANCE OF FORM AND POSITION | | | |
| aaa | 0.10 | | |
| bbb | 0.20 | | |
| ccc | 0.10 | | |
| ddd | 0.25 | | |
| eee | 0.10 | | |



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

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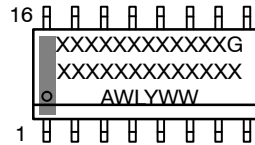
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SOIC-16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
 A = Assembly Location
 WL = Wafer Lot
 Y = Year
 WW = Work Week
 G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

| | | | |
|---|---|---|---|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR 15. EMITTER 16. COLLECTOR</p> | <p>STYLE 2:</p> <p>PIN 1. CATHODE 2. ANODE 3. NO CONNECTION 4. CATHODE 5. CATHODE 6. NO CONNECTION 7. ANODE 8. CATHODE 9. CATHODE 10. ANODE 11. NO CONNECTION 12. CATHODE 13. CATHODE 14. NO CONNECTION 15. ANODE 16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1 2. BASE, #1 3. EMITTER, #1 4. COLLECTOR, #1 5. COLLECTOR, #2 6. BASE, #2 7. EMITTER, #2 8. COLLECTOR, #2 9. COLLECTOR, #3 10. BASE, #3 11. EMITTER, #3 12. COLLECTOR, #3 13. COLLECTOR, #4 14. BASE, #4 15. EMITTER, #4 16. COLLECTOR, #4</p> | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. COLLECTOR, #3 6. COLLECTOR, #3 7. COLLECTOR, #4 8. COLLECTOR, #4 9. BASE, #4 10. EMITTER, #4 11. BASE, #3 12. EMITTER, #3 13. BASE, #2 14. EMITTER, #2 15. BASE, #1 16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. DRAIN, #3 6. DRAIN, #3 7. DRAIN, #4 8. DRAIN, #4 9. GATE, #4 10. SOURCE, #4 11. GATE, #3 12. SOURCE, #3 13. GATE, #2 14. SOURCE, #2 15. GATE, #1 16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. CATHODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE 15. ANODE 16. ANODE</p> | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH 2. COMMON DRAIN (OUTPUT) 3. COMMON DRAIN (OUTPUT) 4. GATE P-CH 5. COMMON DRAIN (OUTPUT) 6. COMMON DRAIN (OUTPUT) 7. COMMON DRAIN (OUTPUT) 8. SOURCE P-CH 9. SOURCE P-CH 10. COMMON DRAIN (OUTPUT) 11. COMMON DRAIN (OUTPUT) 12. COMMON DRAIN (OUTPUT) 13. GATE N-CH 14. COMMON DRAIN (OUTPUT) 15. COMMON DRAIN (OUTPUT) 16. SOURCE N-CH</p> | |

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