3.3 V LVTTL/LVCMOS to LVPECL Translator

MC100EPT622

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Description

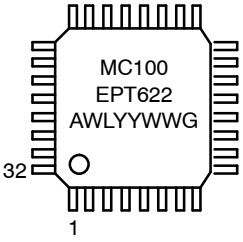
The MC100EPT622 is a 10−Bit LVTTL/LVCMOS to LVPECL translator. Because LVPECL (Positive ECL) levels are used only +3.3 V and ground are required. The device has an OR−ed enable input which can accept either LVPECL (ENPECL) or TTL/LVCMOS inputs (ENTTL). If the inputs are left open, they will default to the enable state. The device design has been optimized for low channel−to−channel skew.

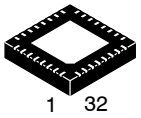
Features

- 450 ps Typical Propagation Delay
- Maximum Frequency > 1.5 GHz Typical
- PECL Mode
- Operating Range: V_{CC} = 3.0 V to 3.8 V with V_{EE} = 0 V
- PNP LVTTL Inputs for Minimal Loading
- Q Output Will Default HIGH with Inputs Open
- The 100 Series Contains Temperature Compensation
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

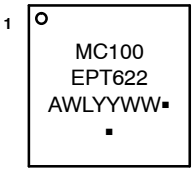
MARKING DIAGRAMS*

LQFP−32
FA SUFFIX
CASE 561AB





QFN32
MN SUFFIX
CASE 488AM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

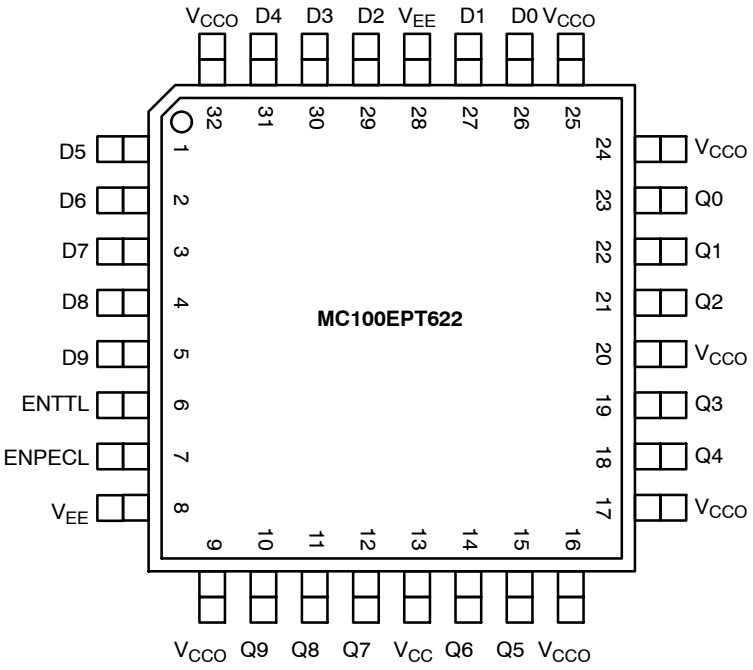
*For additional marking information, refer to Application Note AND8002/D.

Table 1. TRUTH TABLE

ENPECL	ENTTL	D	Q
H	X	H	H
H	X	L	L
X	H	H	H
X	H	L	L
L	L	X	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.



Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 32−Lead LQFP Pinout (Top View)

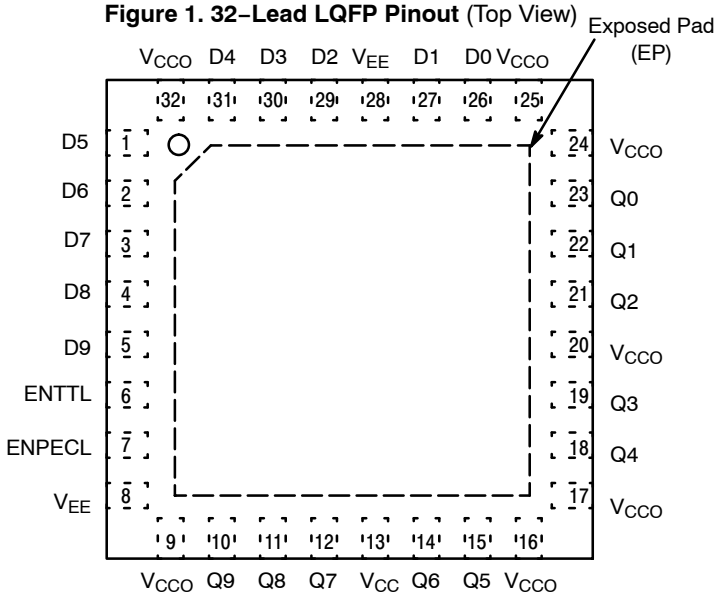


Figure 3. 32−Lead QFN Pinout (Top View)

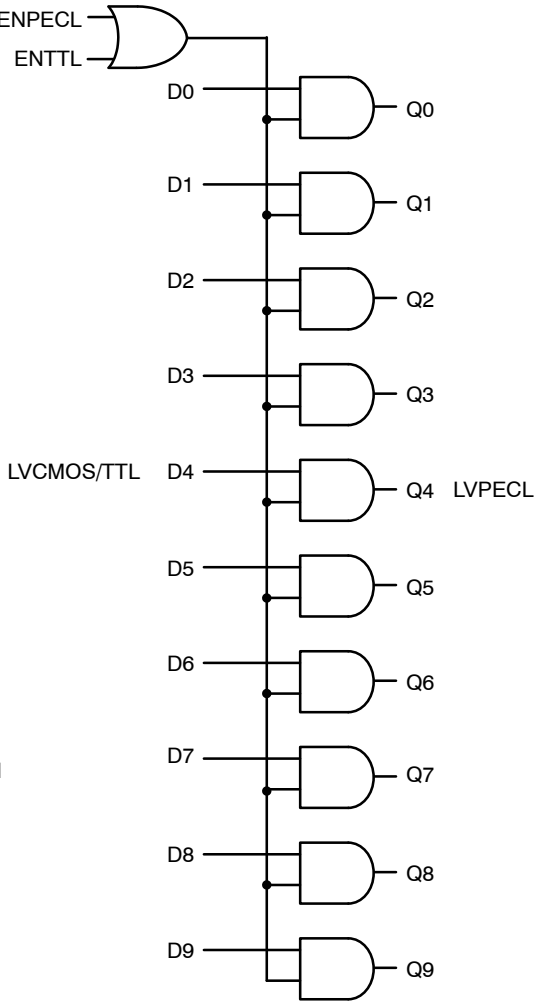


Figure 2. Logic Symbol

Table 1. PIN DESCRIPTION

Pin	Function
D0:9	Data Input (TTL)
Q0:9	Data Outputs (PECL)
ENTTL	Enable Control (TTL)
ENPECL	Enable Control (PECL)
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Ground
EP	The exposed pad (EP) on the QFN−32 package bottom is thermally connected to the die for improved heat transfer out of the package. THe exposed pad must be attached to a heat−sinking conduit. The pad is electrically connected to V_{EE}.

Table 2. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	N/A
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	 > 2 kV > 150 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack	Pb−Free Pkg
LQFP−32 QFN−32	Level 2 Level 1
Flammability Rating Oxygen Index: 28 to 34	 UL 94 V−0 @ 0.125 in
Transistor Count	596 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Power Supply	V_{EE} = 0 V		5	V
V_I	Input Voltage	V_{EE} = 0 V	$V_I \le V_{CC}$	5 to 0	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	32 LQFP 32 LQFP	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	32 LQFP	12 to 17	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	QFN−32 QFN−32	31 27	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P	QFN−32	12	°C/W
T_{sol}	Wave Solder			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. TTL INPUT DC CHARACTERISTICS (V_{CC} = 3.3 V, GND= 0.0 V, T_A = −40°C to 85°C)

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V			25	μA
I_{IHH}	Input HIGH Current MAX	V_{IN} = V_{CC}			100	μA
I_{IL}	Input LOW Current	V_{IN} = 0.5 V			−0.6	mA
V_{IK}	Input Clamp Voltage	I_{IN} = −18 mA	−1.2	−0.9		V
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

Table 5. PECL INPUT DC CHARACTERISTICS V_{CC} = 3.3 V, GND= 0.0 V, T_A = −40°C to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current	V_{IN} = 2420 mV			150	μA
I_{IL}	Input LOW Current	V_{IN} = 1490 mV			200	μA
V_{IH}	Input HIGH Voltage		2075		2420	mV
V_{IL}	Input LOW Voltage		1490		1675	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

Table 6. PECL OUTPUT DC CHARACTERISTICS V_{CC} = 3.3 V, GND = 0.0 V (Note 1)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	85	115	145	90	120	155	95	130	155	mA
V_{OH}	Output High Voltage (Note 2)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output Low Voltage (Note 2)	1355	1520	1700	1355	1520	1700	1355	1520	1700	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with V_{CC}.
2. All loading with 50 Ω to V_{CC}−2.0 V.

Table 7. AC CHARACTERISTICS V_{CC} = 3.0 V to 3.8 V (Note 3)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (See Figure 4)	1.0	1.5		1.0	1.5		1.0	1.5		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output (Figure 5, Note 4)										ps
	D to Q	100	450	800	100	500	875	100	500	800	
	ENPECL to Q	150	500	875	150	500	875	200	550	925	
	ENTTL to Q	300	450	800	300	500	800	300	500	800	
t_{JITTER}	Random Clock Jitter (RMS) (See Figure 4)		0.7	3.0		0.7	3.0		0.7	3.0	ps
t_r / t_f	Output Rise/Fall Times (20% − 80%)	100	200	450	100	200	250	100	200	300	ps
T_{SKEW}	Duty Cycle Skew (Note 5)										ps
	D to Q										
	Channel 0−7		120	375		120	375		120	375	
	Channel 8−9		200	775		200	775		200	775	
	ENPECL to Q		120	400		120	400		120	400	
	ENTTL to Q		100	275		100	275		100	275	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

3. Measured using a 2.4 V source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}−2.0 V.
4. 1.5 V to 50% point of the output.
5. Duty cycle skew $|t_{PLH} - t_{PHL}|$ on the specific path.

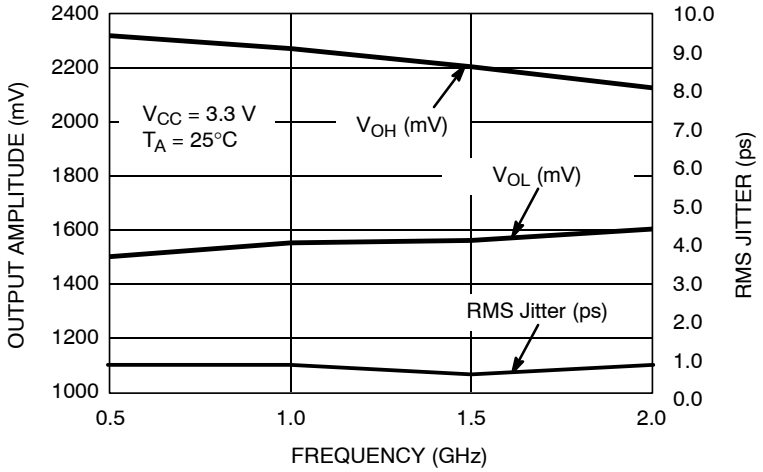


Figure 4. Average Output Amplitude/Jitter (3.3 V, 25°C)

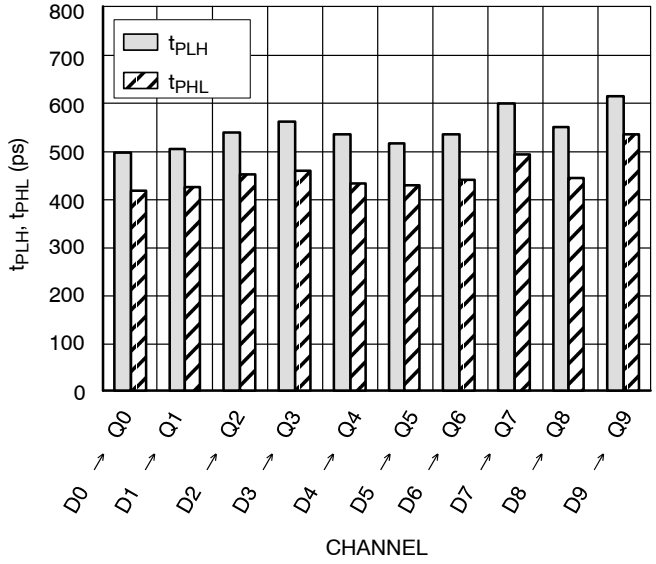


Figure 5. Average Propagation Delay (3.3 V, 25°C)

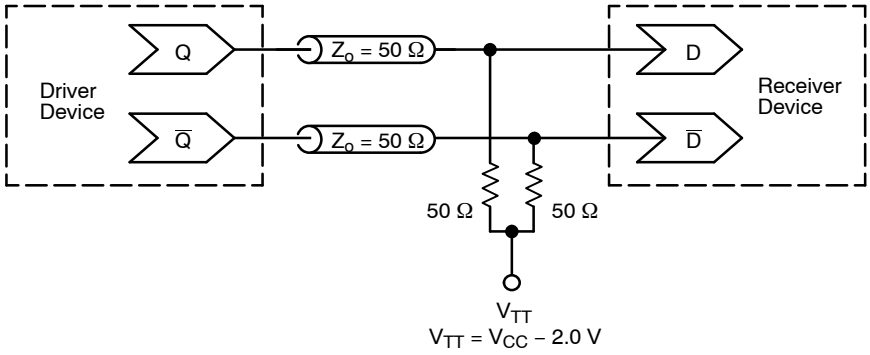


Figure 6. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping
MC100EPT622FAG	LQFP−32 (Pb−Free)	250 Units / Tray
MC100EPT622MNG	QFN32 (Pb−Free)	74 Units / Rail

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

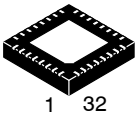
AND8090/D – AC Characteristics of ECL Devices

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

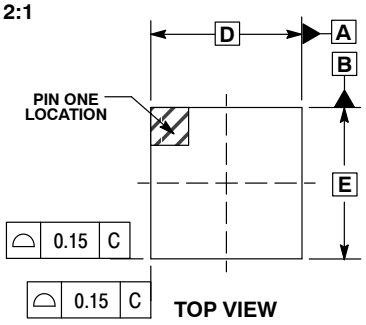
ON Semiconductor®

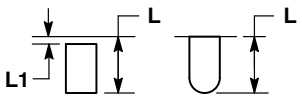
QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

DATE 23 OCT 2013

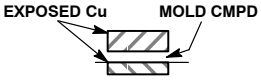


SCALE 2:1

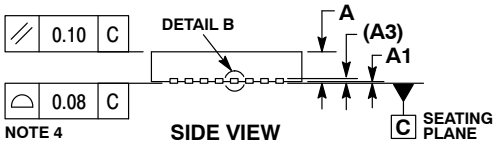


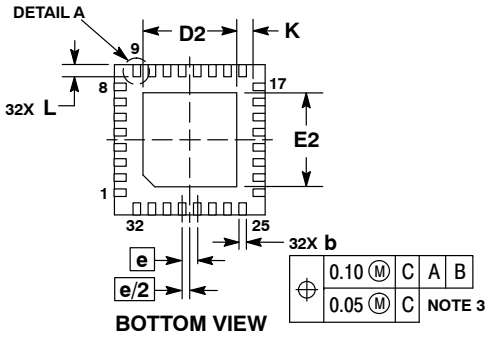


DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION

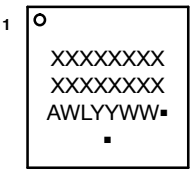




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15

GENERIC MARKING DIAGRAM*

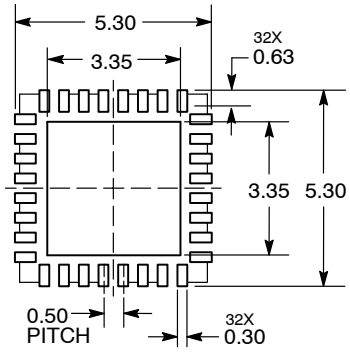


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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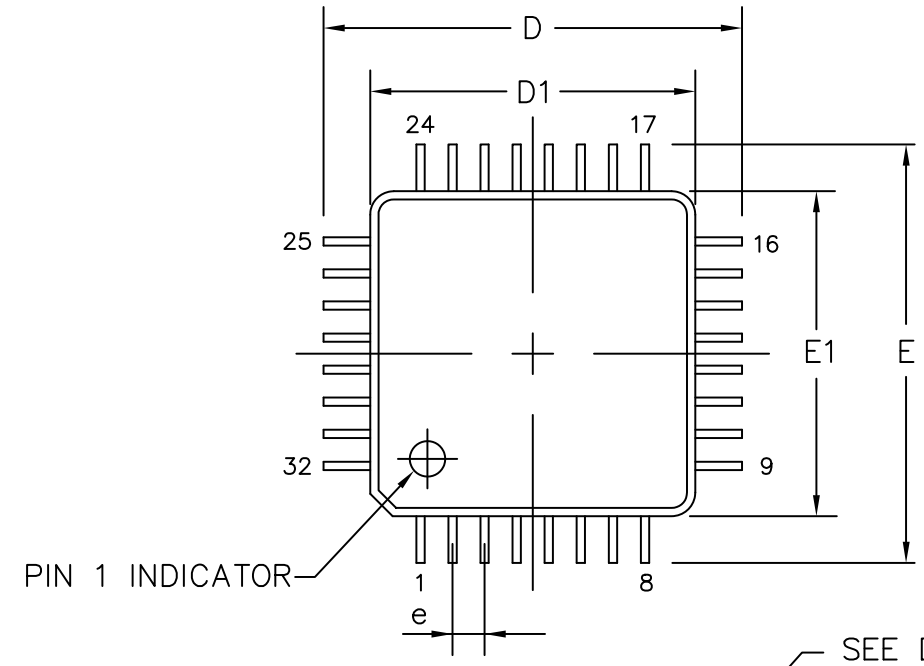
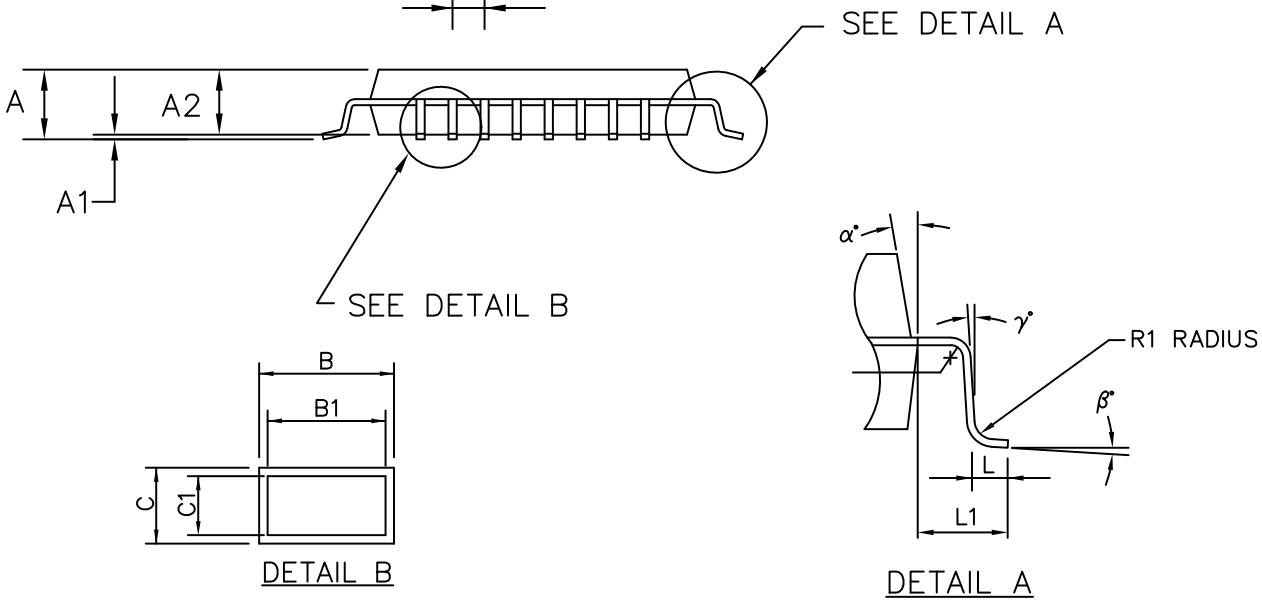
DESCRIPTION:	**QFN32 5x5 0.5P**	**PAGE 1 OF 1**

LQFP−32, 7x7
CASE 561AB−01
ISSUE O

DATE 19 JUN 2008



SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
B	0.30	0.37	0.45
B1	0.30	0.35	0.40
C	0.09	–	0.20
C1	0.09	–	0.16
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.80 BSC.		
L	0.45	0.60	0.75
L1	1.00		
R1	0.08	–	0.20
α°	11	–	13
β°	0	–	7
γ°	0	–	–



ALL DIMENSIONS IN MM

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DESCRIPTION:	**32 LEAD LQFP, 7X7**	**PAGE 1 OF 1**

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