

# 3.3 V 1:2 Fanout Differential LVPECL/LVDS to LVTTTL Translator

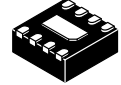
## MC100EPT26



SOIC-8 NB  
 D SUFFIX  
 CASE 751-07



TSSOP-8  
 DT SUFFIX  
 CASE 948R-02



DFN8  
 MN SUFFIX  
 CASE 506AA

### Description

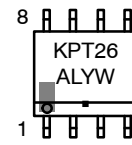
The MC100EPT26 is a 1:2 Fanout Differential LVPECL/LVDS to LVTTTL translator. Because LVPECL (Positive ECL) or LVDS levels are used only +3.3 V and ground are required. The small outline 8-lead package and the 1:2 fanout design of the EPT26 makes it ideal for applications which require the low skew duplication of a signal in a tightly packed PC board.

The  $V_{BB}$  output allows the EPT26 to be used in a Single-Ended input mode. In this mode the  $V_{BB}$  output is tied to the  $\overline{D0}$  input for a non-inverting buffer or the  $D0$  input for an inverting buffer. If used, the  $V_{BB}$  pin should be bypassed to ground with  $> 0.01 \mu\text{F}$  capacitor. For a Single-Ended direct connection, use an external voltage reference source such as a resistor divider. Do not use  $V_{BB}$  for a Single-Ended direct connection or port to another device.

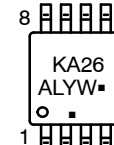
### Features

- 1.4 ns Typical Propagation Delay
- Maximum Frequency =  $> 275 \text{ MHz}$  Typical
- The 100 Series Contains Temperature Compensation
- Operating Range:  $V_{CC} = 3.0 \text{ V}$  to  $3.6 \text{ V}$  with  $GND = 0 \text{ V}$
- 24 mA TTL outputs
- Q Outputs Will Default LOW with Inputs Open or at  $V_{EE}$
- $V_{BB}$  Output
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

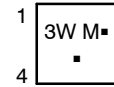
### MARKING DIAGRAMS\*



SOIC-8 NB



TSSOP-8



DFN8

- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

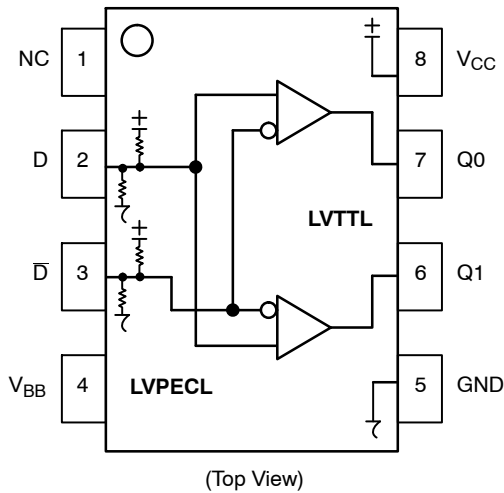
\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

| Device          | Package             | Shipping†        |
|-----------------|---------------------|------------------|
| MC100EPT26DG    | SOIC-8 NB (Pb-Free) | 98 Units/Tube    |
| MC100EPT26DR2G  | SOIC-8 NB (Pb-Free) | 2500 Tape & Reel |
| MC100EPT26DTG   | TSSOP-8 (Pb-Free)   | 100 Tape & Reel  |
| MC100RPT26DTR2G | TSSOP-8 (Pb-Free)   | 2500 Tape & Reel |
| MC100EPT26MNR4G | DFN8 (Pb-Free)      | 1000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# MC100EPT26



**Figure 1. 8-Lead Pinout and Logic Diagram**

**Table 1. PIN DESCRIPTION**

| Pin             | Function   |
|-----------------|--|
| Q0, Q1          | LVTTTL Outputs   |
| D0**, D1**      | Differential LVPECL Inputs Pair  |
| V <sub>CC</sub> | Positive Supply  |
| V <sub>BB</sub> | Output Reference Voltage   |
| GND             | Ground   |
| NC              | No Connect   |
| EP              | (DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open. |

\*\* Pins will default to V<sub>CC</sub>/2 when left open.

**Table 2. ATTRIBUTES**

| Characteristics   | Value                         |
|---|-------------------------------|
| Internal Input Pulldown Resistor  | 50 kΩ                         |
| Internal Input Pullup Resistor  | 50 kΩ                         |
| ESD Protection<br>Human Body Model<br>Machine Model<br>Charged Device Model | > 1.5 kV<br>> 100 V<br>> 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)               | Pb-Free Pkg                   |
| SOIC-8 NB<br>TSSOP-8<br>DFN8  | Level 1<br>Level 3<br>Level 1 |
| Flammability Rating Oxygen Index: 28 to 34                                  | UL 94 V-0 @ 0.125 in          |
| Transistor Count  | 117 Devices                   |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test                      |                               |

1. For additional information, see Application Note [AND8003/D](#).

# MC100EPT26

**Table 3. MAXIMUM RATINGS**

| Symbol           | Parameter                                | Condition 1        | Condition 2                      | Rating      | Unit |
|------------------|--|--------------------|----------------------------------|-------------|------|
| V <sub>CC</sub>  | Positive Power Supply                    | GND = 0 V          |                                  | 3.8         | V    |
| V <sub>IN</sub>  | Input Voltage                            | GND = 0 V          | V <sub>I</sub> ≤ V <sub>CC</sub> | 0 to 3.8    | V    |
| I <sub>BB</sub>  | V <sub>BB</sub> Sink/Source              |                    |                                  | ±0.5        | mA   |
| T <sub>A</sub>   | Operating Temperature Range              |                    |                                  | -40 to +85  | °C   |
| T <sub>stg</sub> | Storage Temperature Range                |                    |                                  | -65 to +150 | °C   |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm | SOIC-8 NB<br>SOIC-8 NB           | 190<br>130  | °C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)    | Standard Board     | SOIC-8 NB                        | 41 to 44    | °C/W |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm | TSSOP-8<br>TSSOP-8               | 185<br>140  | °C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)    | Standard Board     | TSSOP-8                          | 41 to 44    | °C/W |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm | DFN8<br>DFN8                     | 129<br>84   | °C/W |
| T <sub>sol</sub> | Wave Solder (Pb-Free)                    |                    |                                  | 265         | °C   |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)    | (Note 2)           | DFN8                             | 35 to 40    | °C/W |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

**Table 4. PECL INPUT DC CHARACTERISTICS** (V<sub>CC</sub> = 3.3 V; GND = 0.0 V (Note 3))

| Symbol             | Characteristic   | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit |
|--------------------|--|-------|------|------|------|------|------|------|------|------|------|
|                    |  | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |      |
| V <sub>IH</sub>    | Input HIGH Voltage (Single-Ended)                            | 2075  |      | 2420 | 2075 |      | 2420 | 2075 |      | 2420 | mV   |
| V <sub>IL</sub>    | Input LOW Voltage (Single-Ended)                             | 1355  |      | 1675 | 1355 |      | 1675 | 1355 |      | 1675 | mV   |
| V <sub>BB</sub>    | Output Voltage Reference                                     | 1775  | 1875 | 1975 | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | V    |
| V <sub>IHCMR</sub> | Input HIGH Voltage Common Mode Range (Differential) (Note 4) | 1.2   |      | 3.3  | 1.2  |      | 3.3  | 1.2  |      | 3.3  | V    |
| I <sub>IH</sub>    | Input HIGH Current   |       |      | 150  |      |      | 150  |      |      | 150  | μA   |
| I <sub>IL</sub>    | Input LOW Current  |       |      |      |      |      |      |      |      |      | μA   |
|                    | D  | -150  |      |      | -150 |      |      | -150 |      |      |      |
|                    | $\bar{D}$  | -150  |      |      | -150 |      |      | -150 |      |      |      |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

3. Input parameters vary 1:1 with V<sub>CC</sub>.

4. V<sub>IHCMR</sub> min varies 1:1 with GND, V<sub>IHCMR</sub> max varies 1:1 with V<sub>CC</sub>. The V<sub>IHCMR</sub> range is referenced to the most positive side of the differential input signal.

# MC100EPT26

**Table 5. TTL OUTPUT DC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ;  $GND = 0.0\text{ V}$ ;  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ )

| Symbol    | Characteristic               | Condition                 | Min | Typ | Max  | Unit |
|-----------|------------------------------|---------------------------|-----|-----|------|------|
| $V_{OH}$  | Output HIGH Voltage          | $I_{OH} = -3.0\text{ mA}$ | 2.4 |     |      | V    |
| $V_{OL}$  | Output LOW Voltage           | $I_{OL} = 24\text{ mA}$   |     |     | 0.5  | V    |
| $I_{CCH}$ | Power Supply Current         |                           | 10  | 25  | 35   | mA   |
| $I_{CCL}$ | Power Supply Current         |                           | 15  | 34  | 40   | mA   |
| $I_{OS}$  | Output Short Circuit Current |                           | -50 |     | -150 | mA   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

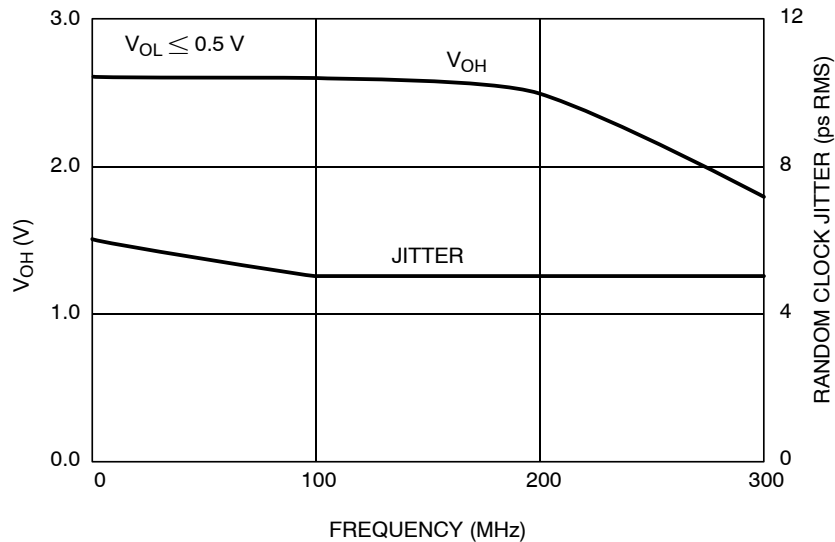
**Table 6. AC CHARACTERISTICS** ( $V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$ ;  $GND = 0.0\text{ V}$  (Note 5))

| Symbol                                   | Characteristic  | $-40^\circ\text{C}$ |     |      | $25^\circ\text{C}$ |     |      | $85^\circ\text{C}$ |     |      | Unit |
|--|---|---------------------|-----|------|--------------------|-----|------|--------------------|-----|------|------|
|  |   | Min                 | Typ | Max  | Min                | Typ | Max  | Min                | Typ | Max  |      |
| $f_{\max}$                               | Maximum Frequency (Figure 2)  | 275                 | 350 |      | 275                | 350 |      | 275                | 350 |      | MHz  |
| $t_{PLH}$ ,<br>$t_{PHL}$                 | Propagation Delay to Output Differential (Note 6)                                       | 1.2                 | 1.5 | 2.0  | 1.2                | 1.5 | 2.0  | 1.3                | 1.7 | 2.2  | ns   |
| $t_{SK+}$ ,<br>$t_{SK-}$ ,<br>$t_{SKPP}$ | Within Device Skew + +<br>Within Device Skew - -<br>Device-to-Device Skew (Note 7)      |                     | 15  | 60   |                    | 15  | 60   |                    | 20  | 85   | ps   |
| $t_{JITTER}$                             | Random Clock Jitter (RMS) (Figure 2)<br>@ $\leq 200\text{ MHz}$<br>@ $> 200\text{ MHz}$ |                     | 6   | 30   |                    | 6   | 30   |                    | 6   | 30   | ps   |
| $V_{PP}$                                 | Input Voltage Swing (Differential Configuration)  | 150                 | 800 | 1200 | 150                | 800 | 1200 | 150                | 800 | 1200 | mV   |
| $t_r$ ,<br>$t_f$                         | Output Rise/Fall Times<br>(0.8 V–2.0 V) $Q$ , $\bar{Q}$                                 | 330                 | 600 | 950  | 330                | 600 | 950  | 330                | 650 | 950  | ps   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

5. Measured with a 750 mV 50% duty-cycle clock source.  $R_L = 500\ \Omega$  to GND and  $C_L = 20\text{ pF}$  to GND. Refer to Figure 3.
6. Reference ( $V_{CC} = 3.3\text{ V} \pm 5\%$ ;  $GND = 0\text{ V}$ )
7. Skews are measured between outputs under identical transitions.



**Figure 2. Typical  $V_{OH}$  / Jitter versus Frequency ( $25^\circ\text{C}$ )**

## MC100EPT26

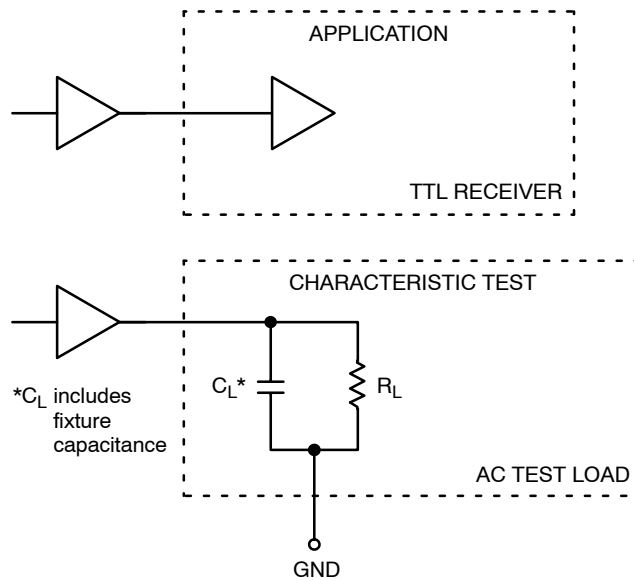


Figure 3. TTL Output Loading Used for Device Evaluation

### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

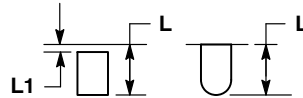
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 4:1

DFN8 2x2, 0.5P  
CASE 506AA  
ISSUE F

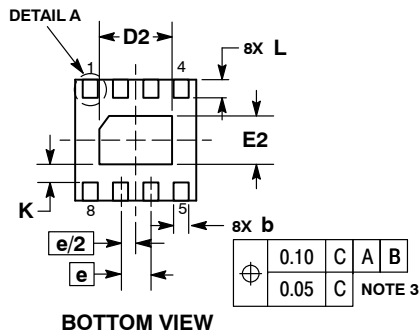
DATE 04 MAY 2016



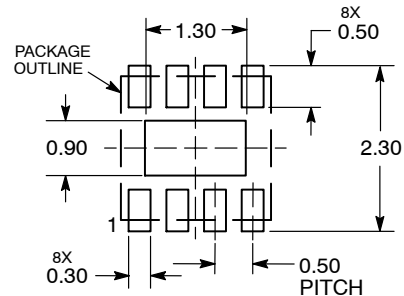
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS |      |
|-----|-------------|------|
|     | MIN         | MAX  |
| A   | 0.80        | 1.00 |
| A1  | 0.00        | 0.05 |
| A3  | 0.20 REF    |      |
| b   | 0.20        | 0.30 |
| D   | 2.00 BSC    |      |
| D2  | 1.10        | 1.30 |
| E   | 2.00 BSC    |      |
| E2  | 0.70        | 0.90 |
| e   | 0.50 BSC    |      |
| K   | 0.30 REF    |      |
| L   | 0.25        | 0.35 |
| L1  | ---         | 0.10 |

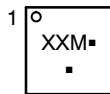


### RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

### GENERIC MARKING DIAGRAM\*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Device

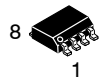
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |  |   |   |   |
|--|---|---|---|
| <p><b>STYLE 1:</b><br/> PIN 1. EMITTER<br/> 2. COLLECTOR<br/> 3. COLLECTOR<br/> 4. EMITTER<br/> 5. EMITTER<br/> 6. BASE<br/> 7. BASE<br/> 8. EMITTER</p>   | <p><b>STYLE 2:</b><br/> PIN 1. COLLECTOR, DIE, #1<br/> 2. COLLECTOR, #1<br/> 3. COLLECTOR, #2<br/> 4. COLLECTOR, #2<br/> 5. BASE, #2<br/> 6. EMITTER, #2<br/> 7. BASE, #1<br/> 8. EMITTER, #1</p>               | <p><b>STYLE 3:</b><br/> PIN 1. DRAIN, DIE #1<br/> 2. DRAIN, #1<br/> 3. DRAIN, #2<br/> 4. DRAIN, #2<br/> 5. GATE, #2<br/> 6. SOURCE, #2<br/> 7. GATE, #1<br/> 8. SOURCE, #1</p>                            | <p><b>STYLE 4:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. ANODE<br/> 4. ANODE<br/> 5. ANODE<br/> 6. ANODE<br/> 7. ANODE<br/> 8. COMMON CATHODE</p>   |
| <p><b>STYLE 5:</b><br/> PIN 1. DRAIN<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. DRAIN<br/> 5. GATE<br/> 6. GATE<br/> 7. SOURCE<br/> 8. SOURCE</p>   | <p><b>STYLE 6:</b><br/> PIN 1. SOURCE<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. SOURCE<br/> 5. SOURCE<br/> 6. GATE<br/> 7. GATE<br/> 8. SOURCE</p>  | <p><b>STYLE 7:</b><br/> PIN 1. INPUT<br/> 2. EXTERNAL BYPASS<br/> 3. THIRD STAGE SOURCE<br/> 4. GROUND<br/> 5. DRAIN<br/> 6. GATE 3<br/> 7. SECOND STAGE Vd<br/> 8. FIRST STAGE Vd</p>                    | <p><b>STYLE 8:</b><br/> PIN 1. COLLECTOR, DIE #1<br/> 2. BASE, #1<br/> 3. BASE, #2<br/> 4. COLLECTOR, #2<br/> 5. COLLECTOR, #2<br/> 6. EMITTER, #2<br/> 7. EMITTER, #1<br/> 8. COLLECTOR, #1</p>                              |
| <p><b>STYLE 9:</b><br/> PIN 1. EMITTER, COMMON<br/> 2. COLLECTOR, DIE #1<br/> 3. COLLECTOR, DIE #2<br/> 4. EMITTER, COMMON<br/> 5. EMITTER, COMMON<br/> 6. BASE, DIE #2<br/> 7. BASE, DIE #1<br/> 8. EMITTER, COMMON</p> | <p><b>STYLE 10:</b><br/> PIN 1. GROUND<br/> 2. BIAS 1<br/> 3. OUTPUT<br/> 4. GROUND<br/> 5. GROUND<br/> 6. BIAS 2<br/> 7. INPUT<br/> 8. GROUND</p>  | <p><b>STYLE 11:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. DRAIN 2<br/> 7. DRAIN 1<br/> 8. DRAIN 1</p>   | <p><b>STYLE 12:</b><br/> PIN 1. SOURCE<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 13:</b><br/> PIN 1. N.C.<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>  | <p><b>STYLE 14:</b><br/> PIN 1. N-SOURCE<br/> 2. N-GATE<br/> 3. P-SOURCE<br/> 4. P-GATE<br/> 5. P-DRAIN<br/> 6. P-DRAIN<br/> 7. N-DRAIN<br/> 8. N-DRAIN</p>   | <p><b>STYLE 15:</b><br/> PIN 1. ANODE 1<br/> 2. ANODE 1<br/> 3. ANODE 1<br/> 4. ANODE 1<br/> 5. CATHODE, COMMON<br/> 6. CATHODE, COMMON<br/> 7. CATHODE, COMMON<br/> 8. CATHODE, COMMON</p>               | <p><b>STYLE 16:</b><br/> PIN 1. EMITTER, DIE #1<br/> 2. BASE, DIE #1<br/> 3. EMITTER, DIE #2<br/> 4. BASE, DIE #2<br/> 5. COLLECTOR, DIE #2<br/> 6. COLLECTOR, DIE #2<br/> 7. COLLECTOR, DIE #1<br/> 8. COLLECTOR, DIE #1</p> |
| <p><b>STYLE 17:</b><br/> PIN 1. VCC<br/> 2. V2OUT<br/> 3. V1OUT<br/> 4. TXE<br/> 5. RXE<br/> 6. VEE<br/> 7. GND<br/> 8. ACC</p>  | <p><b>STYLE 18:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. CATHODE<br/> 8. CATHODE</p>   | <p><b>STYLE 19:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. MIRROR 2<br/> 7. DRAIN 1<br/> 8. MIRROR 1</p>   | <p><b>STYLE 20:</b><br/> PIN 1. SOURCE (N)<br/> 2. GATE (N)<br/> 3. SOURCE (P)<br/> 4. GATE (P)<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 21:</b><br/> PIN 1. CATHODE 1<br/> 2. CATHODE 2<br/> 3. CATHODE 3<br/> 4. CATHODE 4<br/> 5. CATHODE 5<br/> 6. COMMON ANODE<br/> 7. COMMON ANODE<br/> 8. CATHODE 6</p>  | <p><b>STYLE 22:</b><br/> PIN 1. I/O LINE 1<br/> 2. COMMON CATHODE/VCC<br/> 3. COMMON CATHODE/VCC<br/> 4. I/O LINE 3<br/> 5. COMMON ANODE/GND<br/> 6. I/O LINE 4<br/> 7. I/O LINE 5<br/> 8. COMMON ANODE/GND</p> | <p><b>STYLE 23:</b><br/> PIN 1. LINE 1 IN<br/> 2. COMMON ANODE/GND<br/> 3. COMMON ANODE/GND<br/> 4. LINE 2 IN<br/> 5. LINE 2 OUT<br/> 6. COMMON ANODE/GND<br/> 7. COMMON ANODE/GND<br/> 8. LINE 1 OUT</p> | <p><b>STYLE 24:</b><br/> PIN 1. BASE<br/> 2. EMITTER<br/> 3. COLLECTOR/ANODE<br/> 4. COLLECTOR/ANODE<br/> 5. CATHODE<br/> 6. CATHODE<br/> 7. COLLECTOR/ANODE<br/> 8. COLLECTOR/ANODE</p>                                      |
| <p><b>STYLE 25:</b><br/> PIN 1. VIN<br/> 2. N/C<br/> 3. REXT<br/> 4. GND<br/> 5. IOUT<br/> 6. IOUT<br/> 7. IOUT<br/> 8. IOUT</p>   | <p><b>STYLE 26:</b><br/> PIN 1. GND<br/> 2. dv/dt<br/> 3. ENABLE<br/> 4. ILIMIT<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. VCC</p>  | <p><b>STYLE 27:</b><br/> PIN 1. ILIMIT<br/> 2. OVLO<br/> 3. UVLO<br/> 4. INPUT+<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. DRAIN</p>  | <p><b>STYLE 28:</b><br/> PIN 1. SW_TO_GND<br/> 2. DASIC OFF<br/> 3. DASIC_SW_DET<br/> 4. GND<br/> 5. V_MON<br/> 6. VBULK<br/> 7. VBULK<br/> 8. VIN</p>  |
| <p><b>STYLE 29:</b><br/> PIN 1. BASE, DIE #1<br/> 2. EMITTER, #1<br/> 3. BASE, #2<br/> 4. EMITTER, #2<br/> 5. COLLECTOR, #2<br/> 6. COLLECTOR, #2<br/> 7. COLLECTOR, #1<br/> 8. COLLECTOR, #1</p>                        | <p><b>STYLE 30:</b><br/> PIN 1. DRAIN 1<br/> 2. DRAIN 1<br/> 3. GATE 2<br/> 4. SOURCE 2<br/> 5. SOURCE 1/DRAIN 2<br/> 6. SOURCE 1/DRAIN 2<br/> 7. SOURCE 1/DRAIN 2<br/> 8. GATE 1</p>                           |   |   |

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

### TSSOP 8 CASE 948R-02 ISSUE A

DATE 04/07/2000



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 2.90        | 3.10 | 0.114     | 0.122 |
| B   | 2.90        | 3.10 | 0.114     | 0.122 |
| C   | 0.80        | 1.10 | 0.031     | 0.043 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.40        | 0.70 | 0.016     | 0.028 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| K   | 0.25        | 0.40 | 0.010     | 0.016 |
| L   | 4.90 BSC    |      | 0.193 BSC |       |
| M   | 0°          | 6°   | 0°        | 6°    |

|                         |                    |  |
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