

LM339S, LM2901S

Single Supply Quad Comparators

These comparators are designed for use in level detection, low-level sensing and memory applications in consumer and industrial electronic applications.

Features

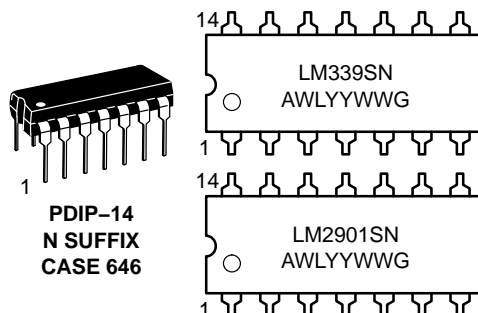
- Single or Split Supply Operation
- Low Input Bias Current: 25 nA (Typ)
- Low Input Offset Current: ± 5.0 nA (Typ)
- Low Input Offset Voltage
- Input Common Mode Voltage Range to GND
- Low Output Saturation Voltage: 130 mV (Typ) @ 4.0 mA
- TTL and CMOS Compatible
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



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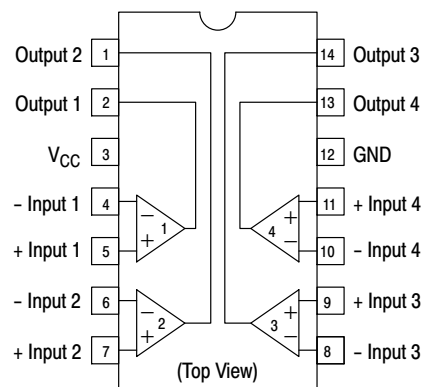
<http://onsemi.com>

MARKING DIAGRAMS



LMxxxx = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y, YY = Year
WW = Work Week
G = Pb-Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

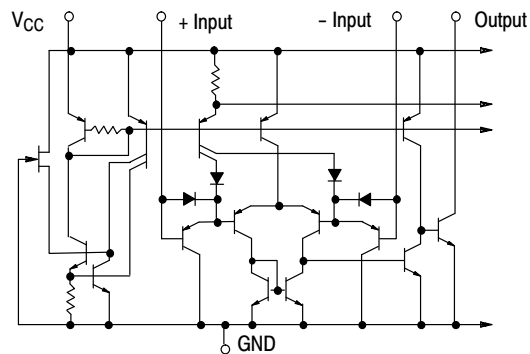
LM339S, LM2901S

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|---|------------------|----------------------------|
| Power Supply Voltage | V_{CC} | +36 or ± 18 | Vdc |
| Input Differential Voltage Range | V_{IDR} | 36 | Vdc |
| Input Common Mode Voltage Range | V_{ICMR} | -0.3 to V_{CC} | Vdc |
| Output Short Circuit to Ground (Note 1) | I_{SC} | Continuous | |
| Power Dissipation @ $T_A = 25^\circ\text{C}$ | P_D | 1.0 | W |
| | Plastic Package Derate above 25°C $1/R_{\theta JA}$ | 8.0 | $\text{mW}/^\circ\text{C}$ |
| Junction Temperature | T_J | 150 | $^\circ\text{C}$ |
| Operating Ambient Temperature Range | T_A | LM2901S | -40 to +105 |
| | | LM339S | 0 to +70 |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC} . Output short circuits to V_{CC} can cause excessive heating and eventual destruction.



NOTE: Diagram shown is for 1 comparator.

Figure 1. Circuit Schematic

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ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.0$ Vdc, $T_A = +25^\circ\text{C}$, unless otherwise noted)

| Characteristic | Symbol | LM339S | | | LM2901S | | | Unit |
|---|------------|--------|------------|----------------|---------|------------|----------------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage (Note 2) | V_{IO} | – | ± 2.0 | ± 5.0 | – | ± 2.0 | ± 7.0 | mVdc |
| Input Bias Current (Notes 2, 3) (Output in Analog Range) | I_{IB} | – | 25 | 250 | – | 25 | 250 | nA |
| Input Offset Current (Note 2) | I_{IO} | – | ± 5.0 | ± 50 | – | ± 5.0 | ± 50 | nA |
| Input Common Mode Voltage Range | V_{ICMR} | 0 | – | $V_{CC} - 1.5$ | 0 | – | $V_{CC} - 1.5$ | V |
| Supply Current $R_L = \infty$ (For All Comparators) $R_L = \infty, V_{CC} = 30$ Vdc | I_{CC} | – | 0.8 1.0 | 2.0 2.5 | – | 0.8 1.0 | 2.0 2.5 | mA |
| Voltage Gain $R_L \geq 15$ k Ω , $V_{CC} = 15$ Vdc | A_{VOL} | 50 | 200 | – | 25 | 100 | – | V/mV |
| Large Signal Response Time $V_I =$ TTL Logic Swing, $V_{ref} = 1.4$ Vdc, $V_{RL} = 5.0$ Vdc, $R_L = 5.1$ k Ω | – | – | 200 | – | – | 200 | – | ns |
| Response Time (Note 4) $V_{RL} = 5.0$ Vdc, $R_L = 5.1$ k Ω | – | – | 1.0 | – | – | 1.0 | – | μs |
| Output Sink Current $V_I(-) \geq +1.0$ Vdc, $V_I(+)=0$, $V_O \leq 1.5$ Vdc | I_{Sink} | 6.0 | 16 | – | 6.0 | 16 | – | mA |
| Saturation Voltage $V_I(-) \geq +1.0$ Vdc, $V_I(+)=0$, $I_{sink} \leq 4.0$ mA | V_{sat} | – | 130 | 400 | – | 130 | 400 | mV |
| Output Leakage Current $V_I(+)\geq +1.0$ Vdc, $V_I(-)=0$, $V_O = +5.0$ Vdc | I_{OL} | – | 0.1 | – | – | 0.1 | – | nA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. At the output switch point, $V_O = 1.4$ Vdc, $R_S \leq 100 \Omega$, 5.0 Vdc $\leq V_{CC} \leq 30$ Vdc, with the inputs over the full common mode range (0 Vdc to $V_{CC} - 1.5$ Vdc).
3. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.
4. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.

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PERFORMANCE CHARACTERISTICS ($V_{CC} = +5.0$ Vdc, $T_A = T_{low}$ to T_{high} (Note 5))

| Characteristic | Symbol | LM339S | | | LM2901S | | | Unit |
|---|------------|--------|-----|----------------|---------|-----|----------------|---------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage (Note 6) | V_{IO} | - | - | ± 9.0 | - | - | ± 15 | mVdc |
| Input Bias Current (Notes 6, 7) (Output in Analog Range) | I_{IB} | - | - | 400 | - | - | 500 | nA |
| Input Offset Current (Note 6) | I_{IO} | - | - | ± 150 | - | - | ± 200 | nA |
| Input Common Mode Voltage Range | V_{ICMR} | 0 | - | $V_{CC} - 2.0$ | 0 | - | $V_{CC} - 2.0$ | V |
| Saturation Voltage $V_{I(-)} \geq +1.0$ Vdc, $V_{I(+)} = 0$, $I_{sink} \leq 4.0$ mA | V_{sat} | - | - | 700 | - | - | 700 | mV |
| Output Leakage Current $V_{I(+)} \geq +1.0$ Vdc, $V_{I(-)} = 0$, $V_O = 30$ Vdc | I_{OL} | - | - | 1.0 | - | - | 1.0 | μ A |
| Differential Input Voltage All $V_I \geq 0$ Vdc | V_{ID} | - | - | V_{CC} | - | - | V_{CC} | Vdc |

- (LM339S) $T_{low} = 0^\circ\text{C}$, $T_{high} = +70^\circ\text{C}$
(LM2901S) $T_{low} = -40^\circ\text{C}$, $T_{high} = +105^\circ\text{C}$
- At the output switch point, $V_O \approx 1.4$ Vdc, $R_S \leq 100 \Omega$ 5.0 Vdc $\leq V_{CC} \leq 30$ Vdc, with the inputs over the full common mode range (0 Vdc to $V_{CC} - 1.5$ Vdc).
- The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.

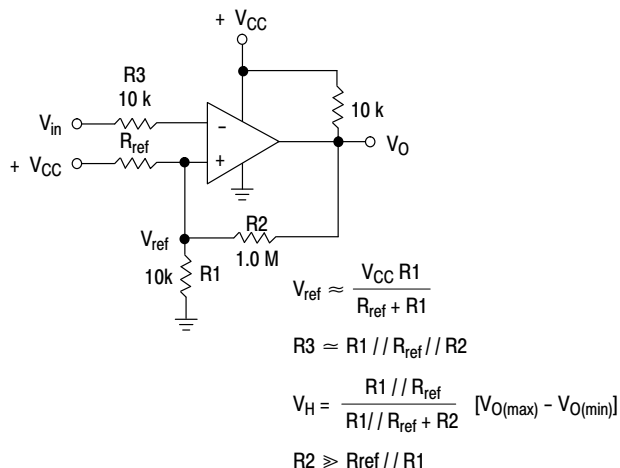


Figure 2. Inverting Comparator with Hysteresis

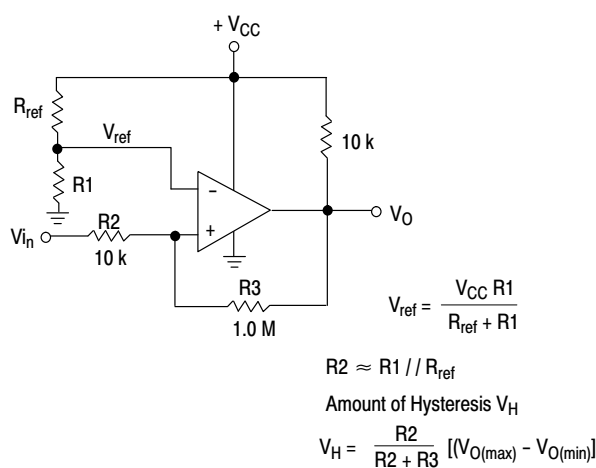
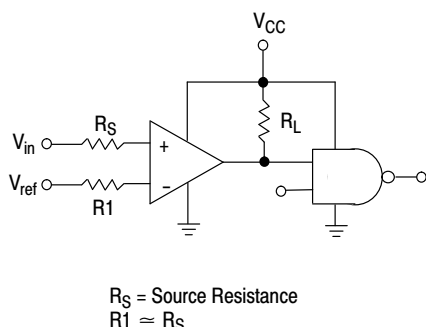


Figure 3. Noninverting Comparator with Hysteresis



| Logic | Device | V_{CC} (V) | R_L k Ω |
|-------|-------------|--------------|------------------|
| CMOS | 1/4 MC14001 | +15 | 100 |
| TTL | 1/4 MC7400 | +5.0 | 10 |

Figure 4. Driving Logic

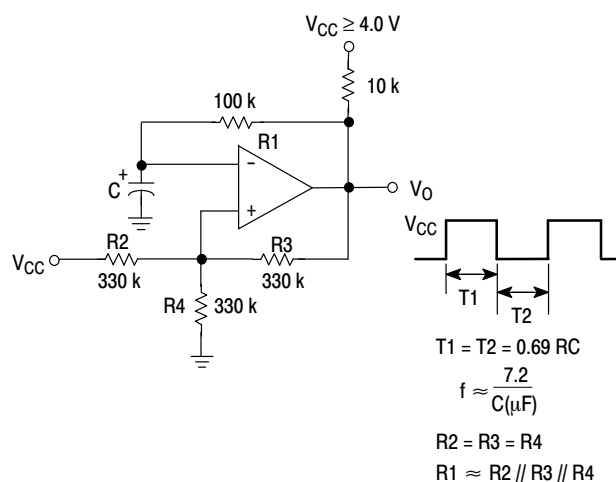


Figure 5. Squarewave Oscillator

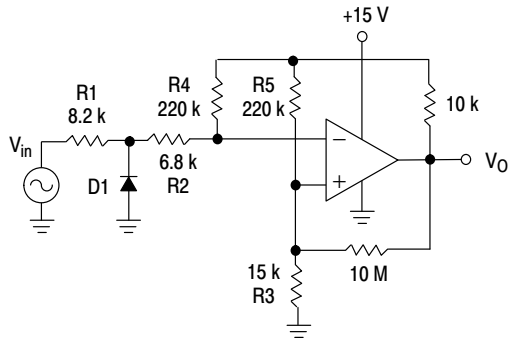
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APPLICATIONS INFORMATION

These quad comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors $< 10\text{ k}\Omega$ should be used. The

addition of positive feedback ($< 10\text{ mV}$) is also recommended. It is good design practice to ground all unused input pins.

Differential input voltages may be larger than supply voltages without damaging the comparator's inputs. Voltages more negative than -300 mV should not be used.

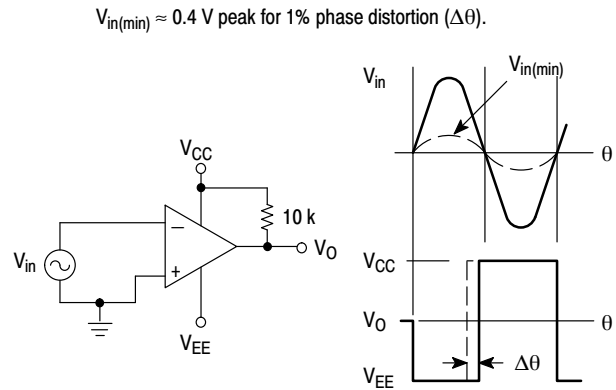


D1 prevents input from going negative by more than 0.6 V.

$$R1 + R2 = R3$$

$$R3 \leq \frac{R5}{10} \text{ for small error in zero crossing}$$

Figure 6. Zero Crossing Detector (Single Supply)



$$V_{in(min)} \approx 0.4\text{ V peak for } 1\% \text{ phase distortion } (\Delta\theta).$$

Figure 7. Zero Crossing Detector (Split Supplies)

ORDERING INFORMATION

| Device | Package | Shipping† |
|-----------|----------------------|-----------------|
| LM339SNG | PDIP-14 (Pb-Free) | 25 Units / Rail |
| LM2901SNG | PDIP-14 (Pb-Free) | 25 Units / Rail |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

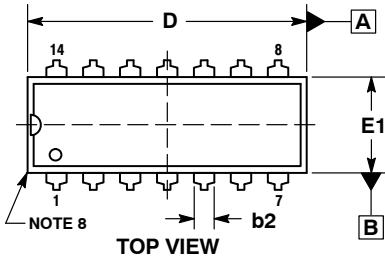
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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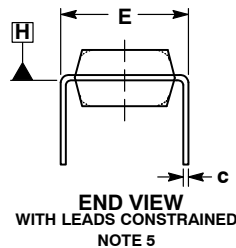


SCALE 1:1



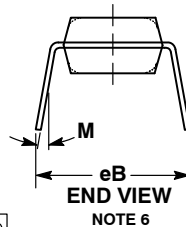
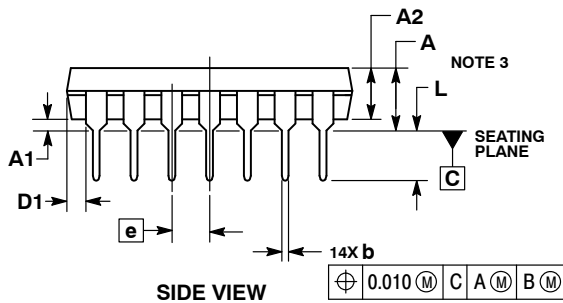
PDIP-14
CASE 646-06
ISSUE S

DATE 22 APR 2015



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).



| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | ---- | 0.210 | ---- | 5.33 |
| A1 | 0.015 | ---- | 0.38 | ---- |
| A2 | 0.115 | 0.195 | 2.92 | 4.95 |
| b | 0.014 | 0.022 | 0.35 | 0.56 |
| b2 | 0.060 TYP | | 1.52 TYP | |
| C | 0.008 | 0.014 | 0.20 | 0.36 |
| D | 0.735 | 0.775 | 18.67 | 19.69 |
| D1 | 0.005 | ---- | 0.13 | ---- |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| E1 | 0.240 | 0.280 | 6.10 | 7.11 |
| e | 0.100 BSC | | 2.54 BSC | |
| eB | ---- | 0.430 | ---- | 10.92 |
| L | 0.115 | 0.150 | 2.92 | 3.81 |
| M | ---- | 10° | ---- | 10° |

GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLES ON PAGE 2

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CASE 646-06
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DATE 22 APR 2015

STYLE 1:
 PIN 1. COLLECTOR
 2. BASE
 3. EMITTER
 4. NO
CONNECTION
 5. EMITTER
 6. BASE
 7. COLLECTOR
 8. COLLECTOR
 9. BASE
 10. EMITTER
 11. NO
CONNECTION
 12. EMITTER
 13. BASE
 14. COLLECTOR

STYLE 2:
 CANCELLED

STYLE 3:
 CANCELLED

STYLE 4:
 PIN 1. DRAIN
 2. SOURCE
 3. GATE
 4. NO
CONNECTION
 5. GATE
 6. SOURCE
 7. DRAIN
 8. DRAIN
 9. SOURCE
 10. GATE
 11. NO
CONNECTION
 12. GATE
 13. SOURCE
 14. DRAIN

STYLE 5:
 PIN 1. GATE
 2. DRAIN
 3. SOURCE
 4. NO CONNECTION
 5. SOURCE
 6. DRAIN
 7. GATE
 8. GATE
 9. DRAIN
 10. SOURCE
 11. NO CONNECTION
 12. SOURCE
 13. DRAIN
 14. GATE

STYLE 6:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 7:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON
 CATHODE

STYLE 8:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 9:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

STYLE 10:
 PIN 1. COMMON
 CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON
 CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 11:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

STYLE 12:
 PIN 1. COMMON CATHODE
 2. COMMON ANODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. COMMON ANODE
 7. COMMON CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

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