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DATA SHEET
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Voltage Regulator - Adjustable Output, Negative

1.5 A

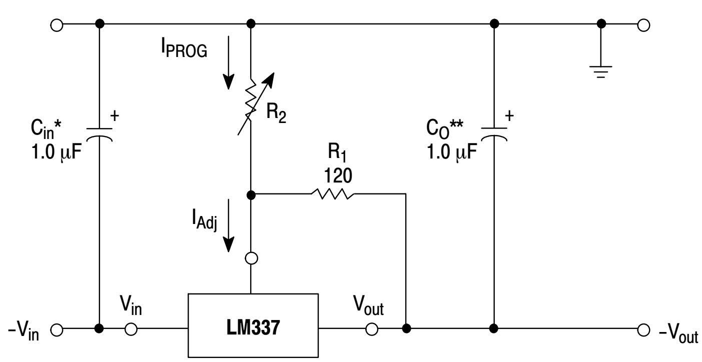
LM337

The LM337 is an adjustable 3−terminal negative voltage regulator capable of supplying in excess of 1.5 A over an output voltage range of −1.2 V to −37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow−out proof.

The LM337 serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM337 can be used as a precision current regulator.

Features

- Output Current in Excess of 1.5 A
- Output Adjustable between −1.2 V and −37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting Constant with Temperature
- Output Transistor Safe−Area Compensation
- Floating Operation for High Voltage Applications
- Eliminates Stocking many Fixed Voltages
- Available in Surface Mount D^{2}PAK and Standard 3−Lead Transistor Package
- These Devices are Pb−Free and are RoHS Compliant



*C_{in} is required if regulator is located more than 4 inches from power supply filter. A 1.0 µF solid tantalum or 10 µF aluminum electrolytic is recommended.

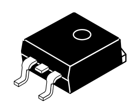
**C_O is necessary for stability. A 1.0 µF solid tantalum or 10 µF aluminum electrolytic is recommended.

$$V_{out} = -1.25\,V\left(1 + \frac{R_2}{R_1}\right)$$

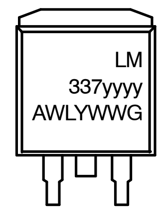
Figure 1. Standard Application

THREE−TERMINAL ADJUSTABLE NEGATIVE VOLTAGE REGULATOR

MARKING DIAGRAMS

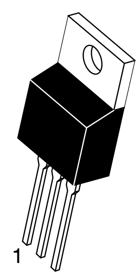


D^{2}PAK
D2T SUFFIX
CASE 936



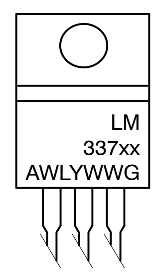
Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

Pin 1. Adjust
2. V_{in}
3. V_{out}



TO−220AB
T SUFFIX
CASE 221AB

Heatsink surface connected to Pin 2.



xx	=	BT, T
yyyy	=	BD2T, D2T
A	=	Assembly Location
WL	=	Wafer Lot
Y	=	Year
WW	=	Work Week
G	=	Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
Input−Output Voltage Differential	V_I–V_O	40	Vdc
Power Dissipation Case 221A T_A = +25°C Thermal Resistance, Junction−to−Ambient Thermal Resistance, Junction−to−Case Case 936 (D^2PAK) T_A = +25°C Thermal Resistance, Junction−to−Ambient Thermal Resistance, Junction−to−Case	 P_D θ_{JA} θ_{JC} P_D θ_{JA} θ_{JC}	 Internally Limited 65 5.0 Internally Limited 70 5.0	 W °C/W °C/W W °C/W °C/W
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

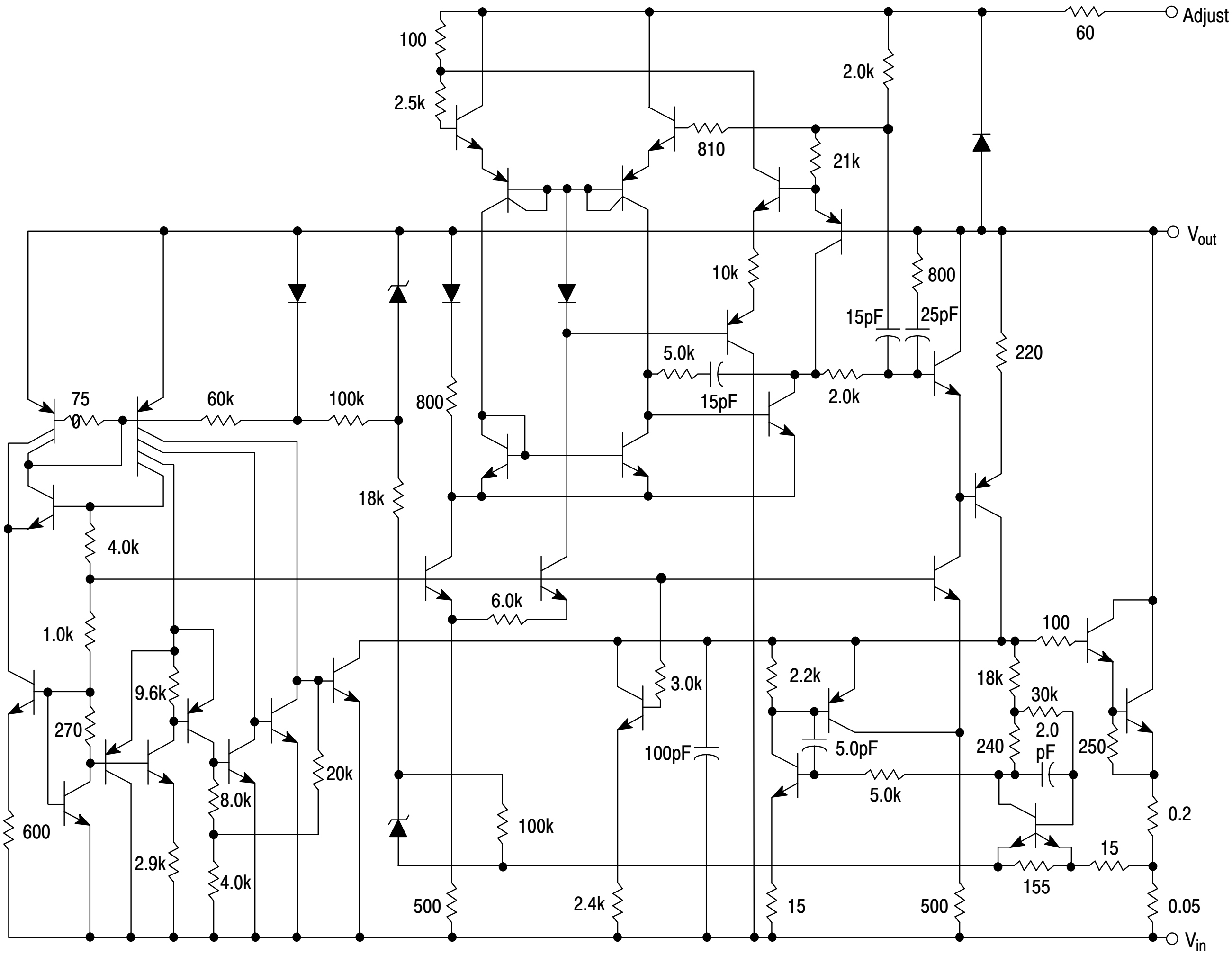
ELECTRICAL CHARACTERISTICS ($|V_I$–$V_O|$ = 5.0 V; I_O = 0.5 A for T package; T_J = T_{low} to T_{high} [Note 1]; I_{max} and P_{max} [Note 2].)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 3), T_A = +25°C, 3.0 V ≤ $|V_I$–$V_O|$ ≤ 40 V	1	Reg_{line}	–	0.01	0.04	%/V
Load Regulation (Note 3), T_A = +25°C, 10 mA ≤ I_O ≤ I_{max} $|V_O|$ ≤ 5.0 V $|V_O|$ ≥ 5.0 V	2	Reg_{load}	 – –	 15 0.3	 50 1.0	 mV % V_O
Thermal Regulation, T_A = +25°C (Note 5), 10 ms Pulse		Reg_{therm}	–	0.003	0.04	% V_O/W
Adjustment Pin Current	3	I_{Adj}	–	65	100	μA
Adjustment Pin Current Change, 2.5 V ≤ $|V_I$–$V_O|$ ≤ 40 V, 10 mA ≤ I_L ≤ I_{max}, P_D ≤ P_{max}, T_A = +25°C	1, 2	ΔI_{Adj}	–	2.0	5.0	μA
Reference Voltage, T_A = +25°C, 3.0 V ≤ $|V_I$–$V_O|$ ≤ 40 V, 10 mA ≤ I_O ≤ I_{max}, P_D ≤ P_{max}, T_J = T_{low} to T_{high}	3	V_{ref}	−1.213 −1.20	−1.250 −1.25	−1.287 −1.30	V
Line Regulation (Note 3), 3.0 V ≤ $|V_I$–$V_O|$ ≤ 40 V	1	Reg_{line}	–	0.02	0.07	%/V
Load Regulation (Note 3), 10 mA ≤ I_O ≤ I_{max} $|V_O|$ ≤ 5.0 V $|V_O|$ ≥ 5.0 V	2	Reg_{load}	 – –	 20 0.3	 70 1.5	 mV % V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	–	0.6	–	% V_O
Minimum Load Current to Maintain Regulation ($|V_I$–$V_O|$ ≤ 10 V) ($|V_I$–$V_O|$ ≤ 40 V)	3	I_{Lmin}	 – –	 1.5 2.5	 6.0 10	mA
Maximum Output Current $|V_I$–$V_O|$ ≤ 15 V, P_D ≤ P_{max}, T Package $|V_I$–$V_O|$ ≤ 40 V, P_D ≤ P_{max}, T_J = +25°C, T Package	3	I_{max}	 – –	 1.5 0.15	 2.2 0.4	A
RMS Noise, % of V_O, T_A = +25°C, 10 Hz ≤ f ≤ 10 kHz		N	–	0.003	–	% V_O
Ripple Rejection, V_O = −10 V, f = 120 Hz (Note 4) Without C_{Adj} C_{Adj} = 10 μF	4	RR	 – 66	 60 77	 – –	dB
Long−Term Stability, T_J = T_{high} (Note 6), T_A = +25°C for Endpoint Measurements	3	S	–	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance, Junction−to−Case, T Package		$R_{\theta JC}$	–	4.0	–	°C/W

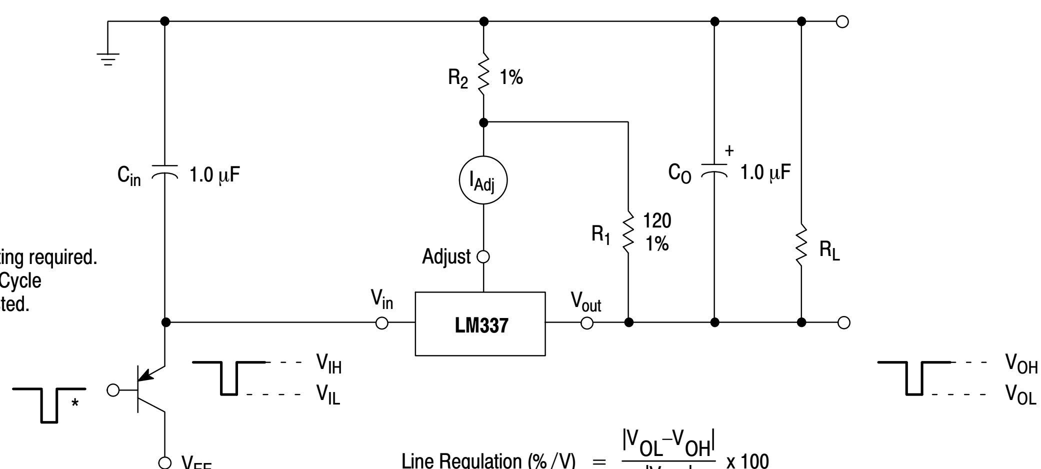
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. T_{low} to T_{high} = 0° to +125°C, for LM337T, D2T. T_{low} to T_{high} = −40° to +125°C, for LM337BT, BD2T.
2. I_{max} = 1.5 A, P_{max} = 20 W
3. Load and line regulation are specified at constant junction temperature. Change in V_O because of heating effects is covered under the Thermal Regulation specification. Pulse testing with a low duty cycle is used.
4. C_{Adj}, when used, is connected between the adjustment pin and ground.
5. Power dissipation within an IC voltage regulator produces a temperature gradient on the die, affecting individual IC components on the die. These effects can be minimized by proper integrated circuit design and layout techniques. Thermal Regulation is the effect of these temperature gradients on the output voltage and is expressed in percentage of output change per watt of power change in a specified time.
6. Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

Representative Schematic Diagram

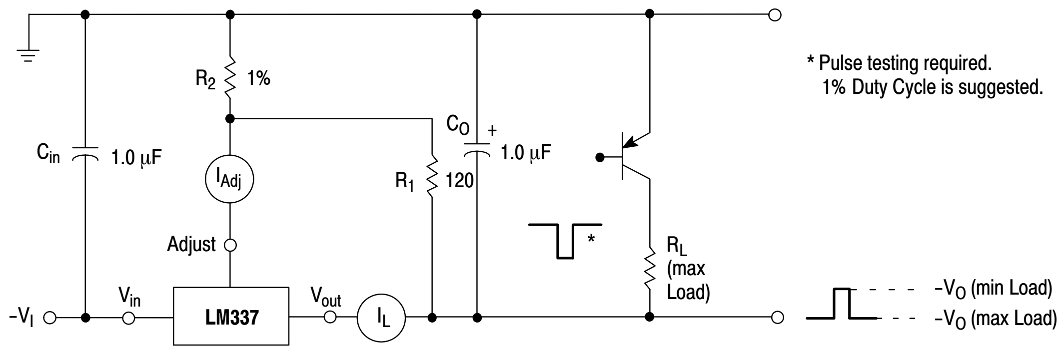


This device contains 39 active transistors.



$$\text{Line Regulation (\%/V)} = \frac{|V_{OL} - V_{OH}|}{|V_{OH}|} \times 100$$

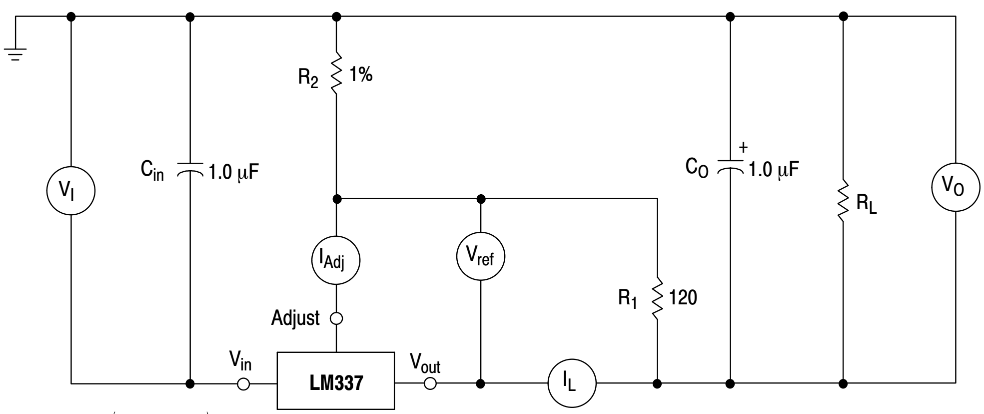
Figure 1. Line Regulation and ΔI_{Adj}/Line Test Circuit



Load Regulation (mV) = V_O (min Load) − V_O (max Load)

$$\text{Load Regulation } (\%\ V_O) = \frac{V_O \text{ (min Load)} - V_O \text{ (max Load)}}{V_O \text{ (min Load)}} \times 100$$

Figure 2. Load Regulation and ΔI_{Adj}/Load Test Circuit

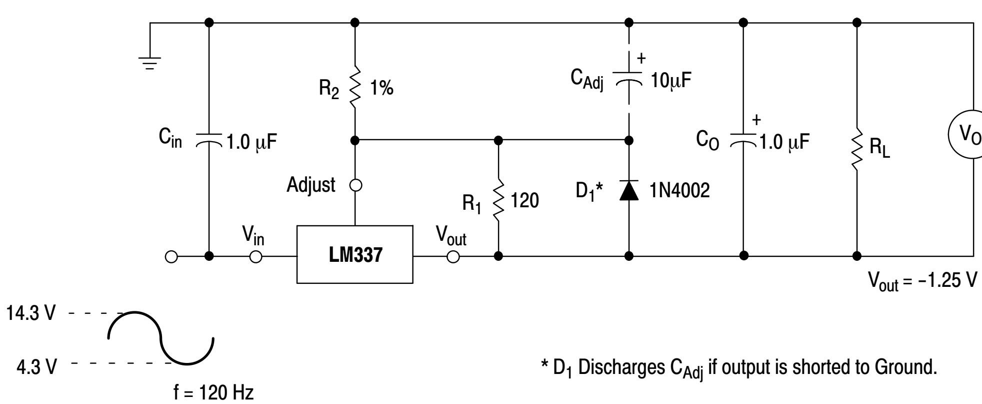


To Calculate R_2: $\quad R_2 = \left(\frac{V_O}{V_{ref}} - 1\right) R_1$

This assumes I_{Adj} is negligible.

* Pulse testing required.
1% Duty Cycle is suggested.

Figure 3. Standard Test Circuit



* D_1 Discharges C_{Adj} if output is shorted to Ground.

Figure 4. Ripple Rejection Test Circuit

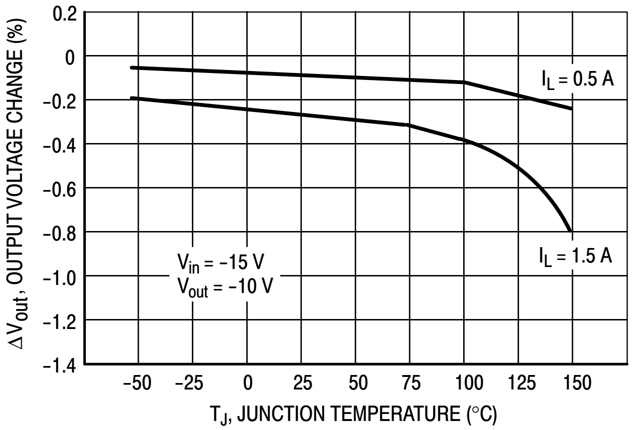


Figure 5. Load Regulation

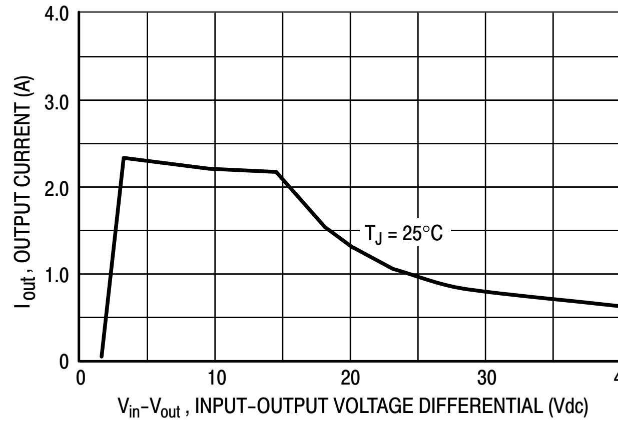


Figure 6. Current Limit

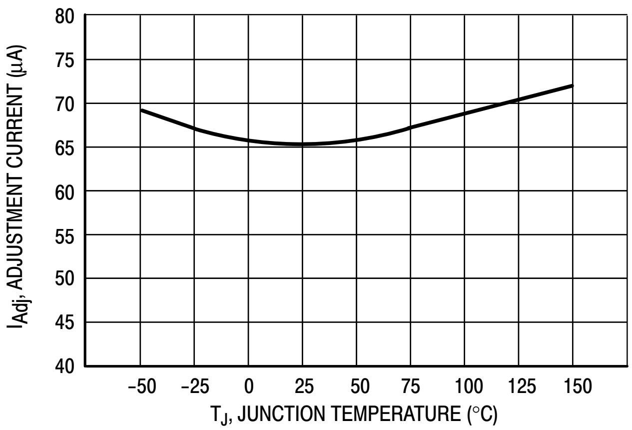


Figure 7. Adjustment Pin Current

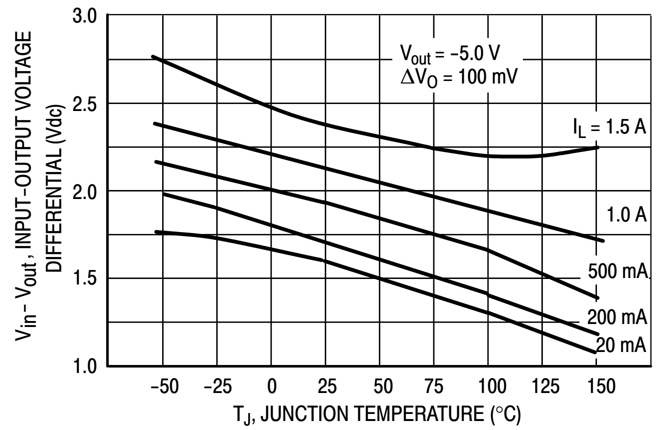


Figure 8. Dropout Voltage

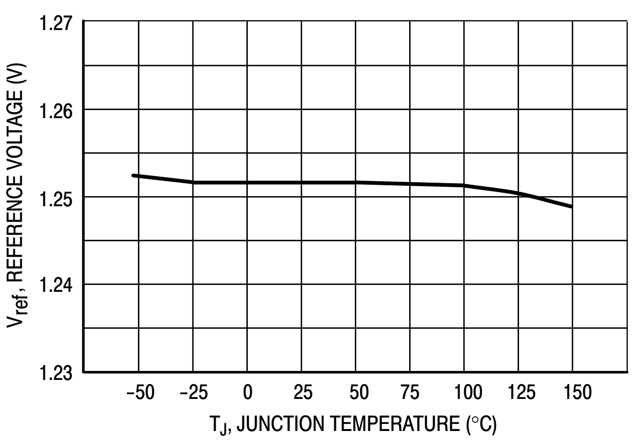


Figure 9. Temperature Stability

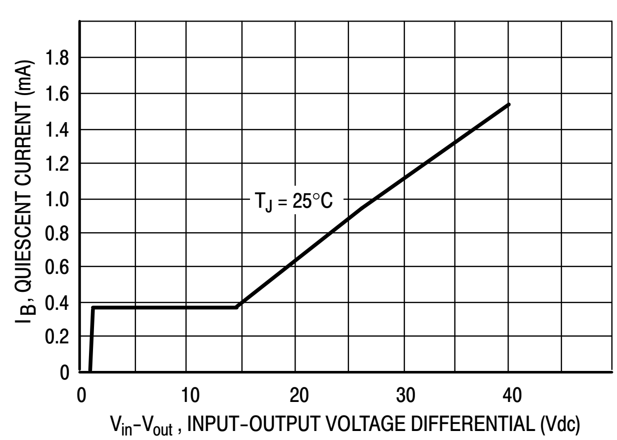


Figure 10. Minimum Operating Current

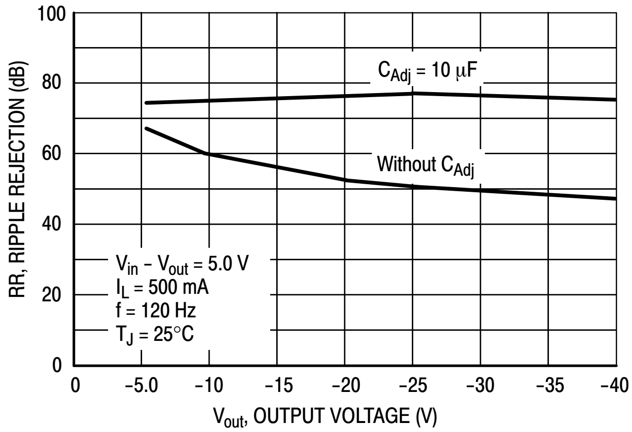


Figure 11. Ripple Rejection versus Output Voltage

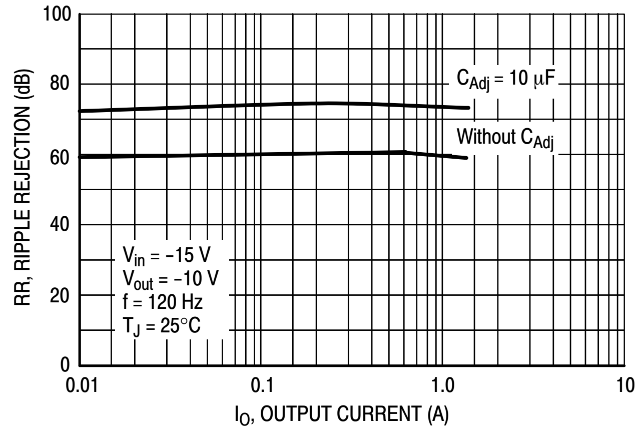


Figure 12. Ripple Rejection versus Output Current

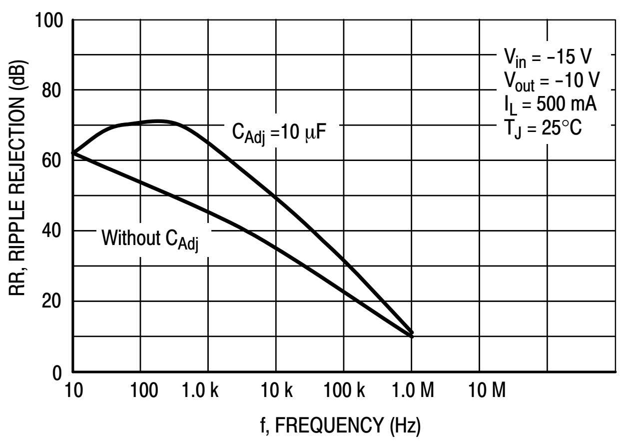


Figure 13. Ripple Rejection versus Frequency

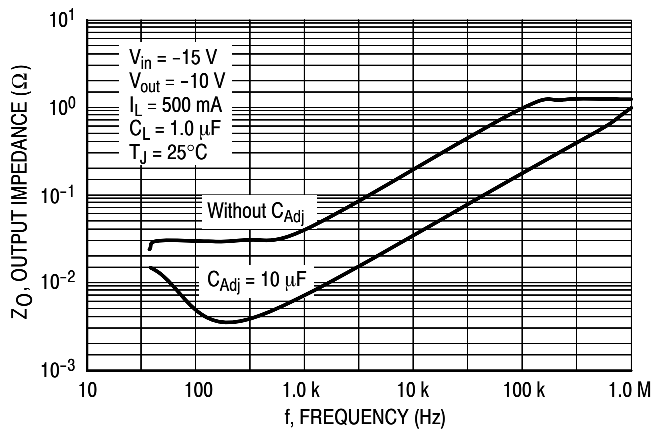


Figure 14. Output Impedance

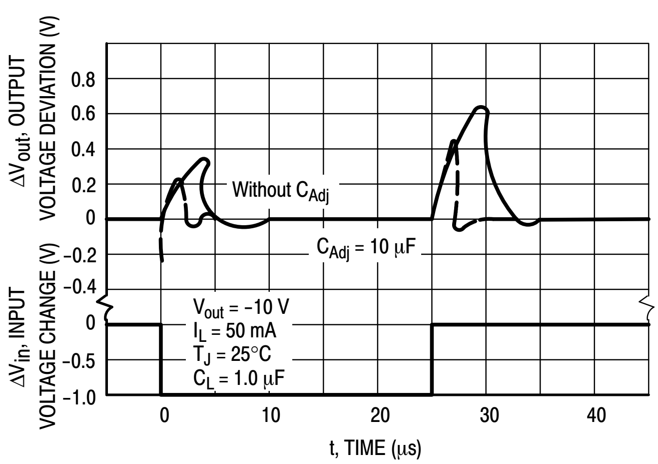


Figure 15. Line Transient Response

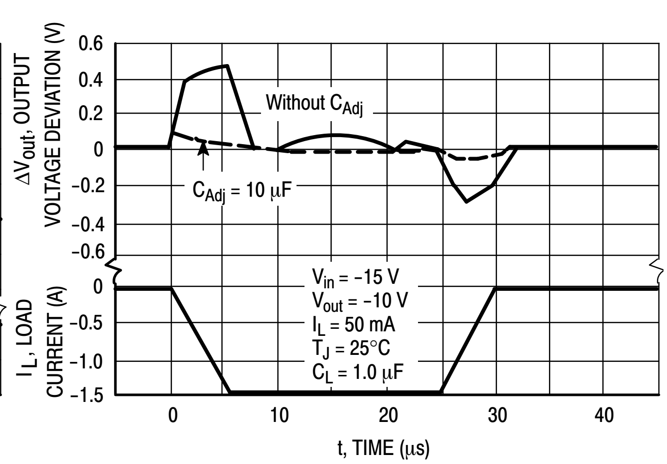


Figure 16. Load Transient Response

APPLICATIONS INFORMATION

Basic Circuit Operation

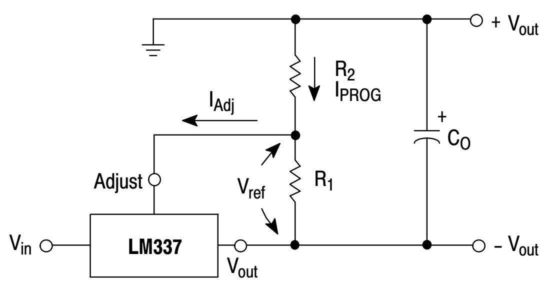
The LM337 is a 3−terminal floating regulator. In operation, the LM337 develops and maintains a nominal −1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R_1 (see Figure 17), and this constant current flows through R_2 from ground.

The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R_2}{R_1}\right) + I_{Adj} R_2$$

Since the current into the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM337 was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM337 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.



V_{ref} = −1.25 V Typical

Figure 17. Basic Circuit Configuration

Load Regulation

The LM337 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R_1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R_2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 1.0 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

An output capacitance (C_O) in the form of a 1.0 μF tantalum or 10 μF aluminum electrolytic capacitor is required for stability. Using the classical tantalum or aluminum electrolytic capacitor types with non−reduced ESR (Equivalent Series Resistance) value is necessary. Low−ESR or similar capacitor types with reduced ESR value and ceramic capacitors can cause instability or continuous oscillations in the application.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM337 with the recommended protection diodes for output voltages in excess of −25 V or high capacitance values (C_O > 25 μF, C_{Adj} > 10 μF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{Adj} from the discharging through the IC during an input short circuit.

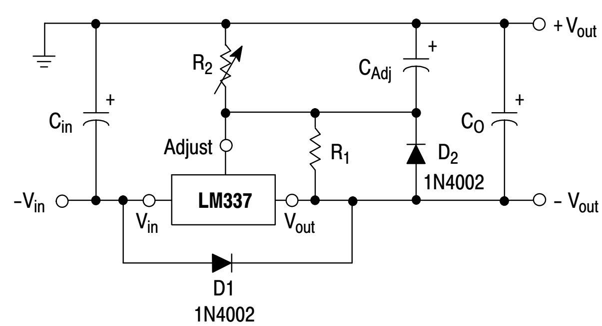


Figure 18. Voltage Regulator with Protection Diodes

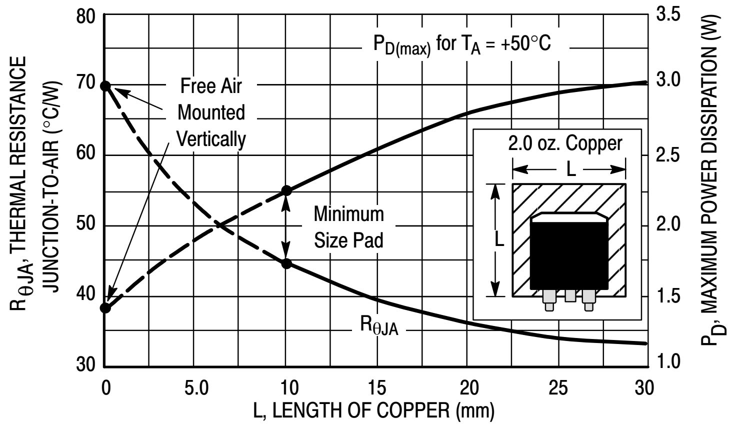
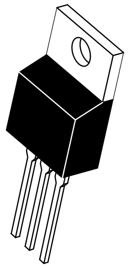


Figure 19. D^2PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping†
LM337BD2TR4G	T_J = −40° to +125°C	D^2PAK (Pb−Free)	800 / Tape & Reel
LM337BTG		TO−220AB (Pb−Free)	50 Units / Rail
LM337D2TR4G	T_J = 0° to +125°C	D^2PAK (Pb−Free)	800 / Tape & Reel
LM337TG		TO−220AB (Pb−Free)	50 Units / Rail

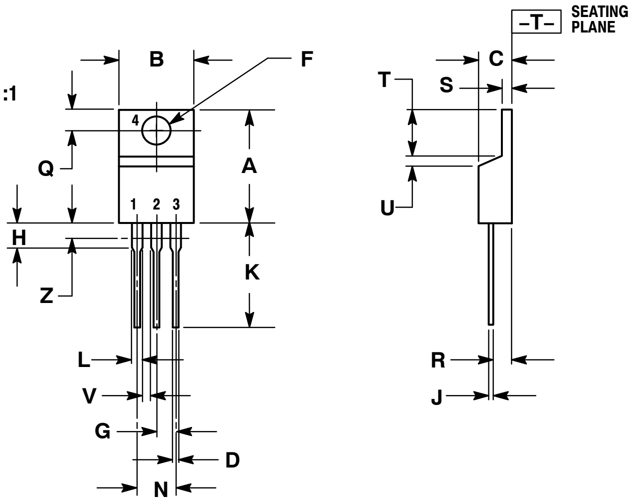
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 1:1

TO−220, SINGLE GAUGE
CASE 221AB
ISSUE A

DATE 16 NOV 2010



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. PRODUCT SHIPPED PRIOR TO 2008 HAD DIMENSIONS S = 0.045 − 0.055 INCHES (1.143 − 1.397 MM)

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.020	0.024	0.508	0.61
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

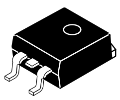
STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

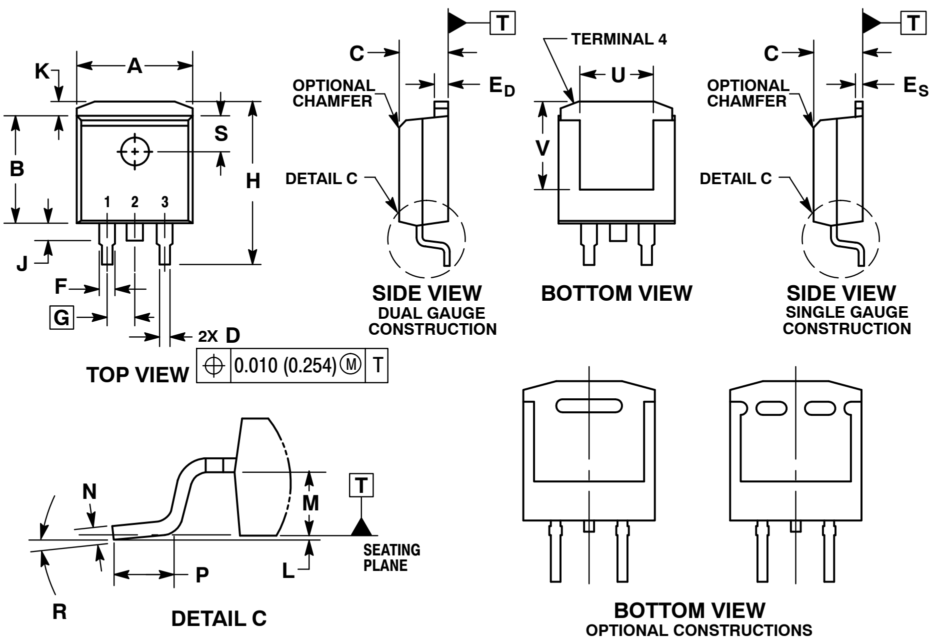
DOCUMENT NUMBER:	98AON23085D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	TO−220, SINGLE GAUGE	PAGE 1 OF 1



SCALE 1:1

D²PAK
CASE 936−03
ISSUE E

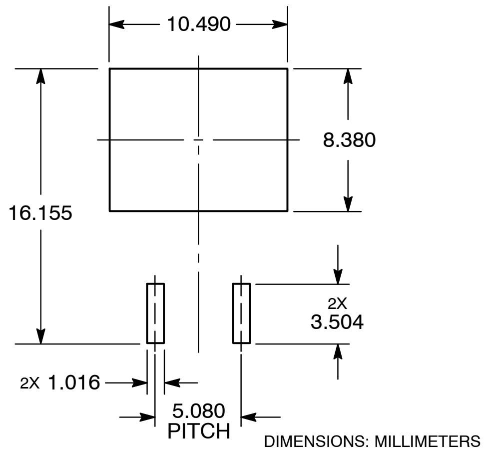
DATE 29 SEP 2015



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.
6. SINGLE GAUGE DESIGN WILL BE SHIPPED AFTER FPCN EXPIRATION IN OCTOBER 2011.

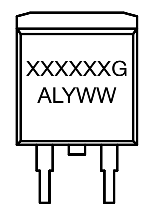
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E_D	0.045	0.055	1.143	1.397
E_S	0.018	0.026	0.457	0.660
F	0.051 REF		1.295 REF	
G	0.100 BSC		2.540 BSC	
H	0.539	0.579	13.691	14.707
J	0.125 MAX		3.175 MAX	
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	0°	8°	0°	8°
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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