

Optical Image Stabilization (OIS) Controller & Driver

CMOS LSI

LC898121XA



WLCSP40, 2.44 x 3.94
CASE 567JB

Overview

The LC898121XA is a system LSI integrating a digital signal processing function for Optical Image Stabilization (OIS) and a saturation-driven H bridge driver function.

Features

Digital Signal Processing

- Built-in Digital Servo Circuit
- Built-in Gyro Filter
- AD Converter
 - ◆ 12 Bit
 - ◆ Input 3ch
 - ◆ Equipped with a Sample-hold Circuit
- DA Converter
 - ◆ 8 Bit
 - ◆ Output 2ch
- Built-in Serial I/F Circuit (4-wire SPI or 2-wire I²C-Bus Interface)
- Built-in Hall Bias Circuit
- Built-in Hall Amp
- Built-in OSC (Oscillator)
 - ◆ Typ. 48 MHz
- Built-in LDO (Low Drop-Out Regulator)
 - ◆ Generation Logic Power (Typ 1.8 V)
- Digital Gyro I/F for the Companies (Please Refer for the Details)

Motor Driver

- Saturation-drive H Bridge x2ch
- I_O max: 300 mA

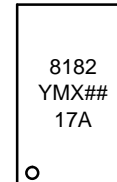
Package

- WLCSP40, 2.44 mm x 3.94 mm, Thickness Max 0.65 mm
- This is a Pb-Free and Halogen Free Device

Power Supply Voltage

- DA/VGA: DAOPVDD = 2.6 V to 3.6 V
- AD: ADVDD = 2.6 V to 3.6 V
- IO/OSC/LDO: DVDD30 = 2.6 V to 3.6 V
- Driver: VM = 2.6 V to 5.5 V
- Core Logic: Use built-in LDO/External VDD: DVDD18 = 1.8 V ±10%

MARKING DIAGRAM



8121 = Specific Device Code
Y = Year
M = Month
X = Assembly Location
= Conversion Character Representing Assembly Lot

ORDERING INFORMATION

| Device | Package | Shipping† |
|---------------|--|-----------------------|
| LC898121XA-MH | WLCSP40, 2.44 x 3.94 (Pb-Free / Halogen Free) | 4000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

LC898121XA

BLOCK DIAGRAM

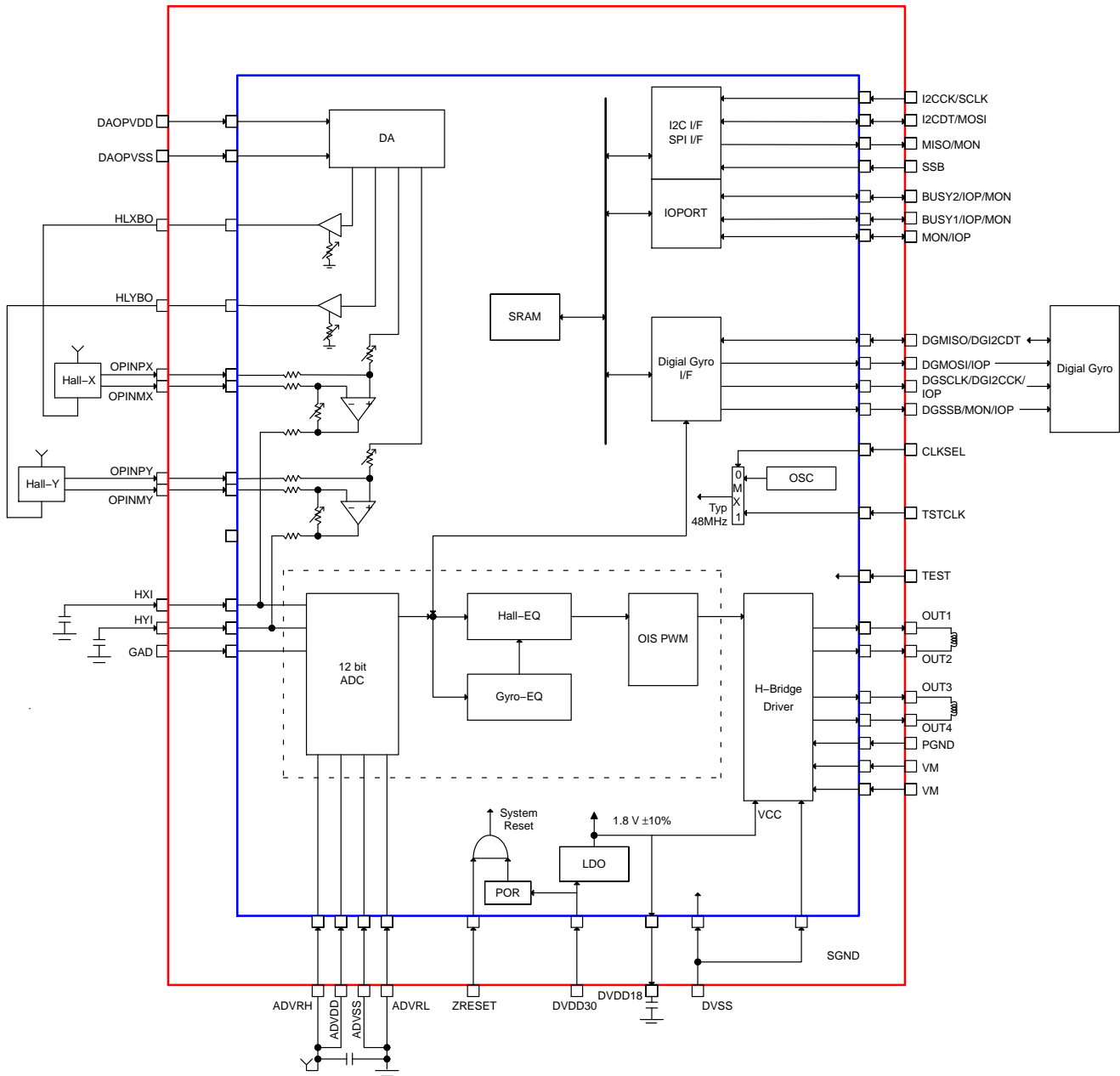


Figure 1. Example of Wiring Diagram [Hall] in LC898121XA (WLP40)

LC898121XA

PIN ASSIGNMENT

| | E | D | C | B | A |
|---|--------|--------|---------|---------|--------|
| 8 | OPINPX | OPINMY | ADVDD | ADVSS | HXI |
| 7 | OPINMX | OPINPY | ADVRH | ADVRL | HYI |
| 6 | HLXBO | HLYBO | DAOPVDD | DAOPVSS | I2CCK |
| 5 | DGSKLK | DGMOSI | GAD | MISO | I2CDT |
| 4 | DGMISO | DGSSB | MON | SSB | DVDD18 |
| 3 | DVSS | CLKSEL | TSTCLK | TEST | DVDD30 |
| 2 | VM | BUSY2 | BUSY1 | ZRESET | VM |
| 1 | OUT4 | OUT3 | PGND | OUT2 | OUT1 |

| | | | |
|---|---------------|---|-------------------------------|
|  | Driver |  | Digital GND |
|  | AD 3 V |  | Digital 3 V VDD |
|  | VGA & DAC 3 V |  | Logic Core 1.8 V VDD (Output) |

Figure 2. WLP40 Bottom View

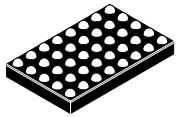
LC898121XA

PIN DESCRIPTION (Type – I: INPUT, O: OUTPUT, B: BIDIRECTION, P: Power)

| Ball No | Pin Name | Type | Description |
|---------|----------|------|---|
| A1 | OUT1 | O | Driver Output |
| A2 | VM | P | Driver VDD (2.6 V to 5.5 V) |
| A3 | DVDD30 | P | Logic 3 V VDD (2.6 V to 3.6 V) |
| A4 | DVDD18 | P | LDO Power supply out (Logic Core VDD (typ 1.8 V)) |
| A5 | I2CDT | B | I2C_IF data (B) / SPI IF data (I) |
| A6 | I2CCK | I | I2C_IF clock / SPI IF clock |
| A7 | HYI | I | Hall-Y AD input |
| A8 | HXI | I | Hall-X AD input |
| B1 | OUT2 | O | Driver output |
| B2 | ZRESET | I | HardWafer Reset |
| B3 | TEST | I | SPI & External clock case sets [1]. other cases set [0] |
| B4 | SSB | B | SPI I/F Chip Select (I) / General-purpose IOPORT(B) / inner signal monitor (O) |
| B5 | MISO | B | SPI I/F data (O) / inner signal monitor / General-purpose IOPORT |
| B6 | DAOPVSS | P | DA&OpAmp VSS |
| B7 | ADVRL | I | ADC ReferenceVoltage Low input |
| B8 | ADVSS | I | AD GND |
| C1 | PGND | P | Driver GND |
| C2 | BUSY1 | B | BUSY1 (O) / General-purpose IOPORT (B) / inner signal monitor (O) |
| C3 | TSTCLK | I | CLKSEL = 1: External Clock, CLKSEL = 0: change pin of I ² C (0) and SPI (1) |
| C4 | MON | B | inner signal monitor / general-purpose IOPORT |
| C5 | GAD | I | General AD input |
| C6 | DAOPVDD | P | DA&OpAmp VDD (2.6 V to 3.6 V) |
| C7 | ADVRH | I | ADC ReferenceVoltage High input |
| C8 | ADVDD | P | AD VDD (2.6 V to 3.6 V) |
| D1 | OUT3 | O | Driver output |
| D2 | BUSY2 | B | BUSY2 (O) / General-purpose IOPORT (B) / inner signal monitor (O) |
| D3 | CLKSEL | I | change pin of OSC (0) and External clock (1) |
| D4 | DGSSB | B | Digital Gyro SPI IF Chip Select (O) / inner signal monitor (O) / General-purpose IOPORT (B) |
| D5 | DGMOSI | B | Digital Gyro (4-wire) IF data (O) / General-purpose IOPORT (B) |
| D6 | HLXBO | O | Hall-Y Bias (Current drive) |
| D7 | OPINPY | I | Hall-Y OpAmp input+ |
| D8 | OPINMY | I | Hall-Y OpAmp input- |
| E1 | OUT4 | O | Driver output |
| E2 | VM | P | Driver VDD (2.6 V to 5.5 V) |
| E3 | DVSS | P | Logic GND |
| E4 | DGMISO | B | Digital Gyro SPI IF data (I) / Digital Gyro I ² C IF data (B) |
| E5 | DGSCLK | B | Digital Gyro SPI IF clock (O) / Digital Gyro I ² C IF clock (O) / General purpose IOPORT (B) |
| E6 | HLXBO | O | Hall-Y Bias (Current drive) |
| E7 | OPINMX | I | Hall-X OpAmp input- |
| E8 | OPINPX | I | Hall-X OpAmp input+ |

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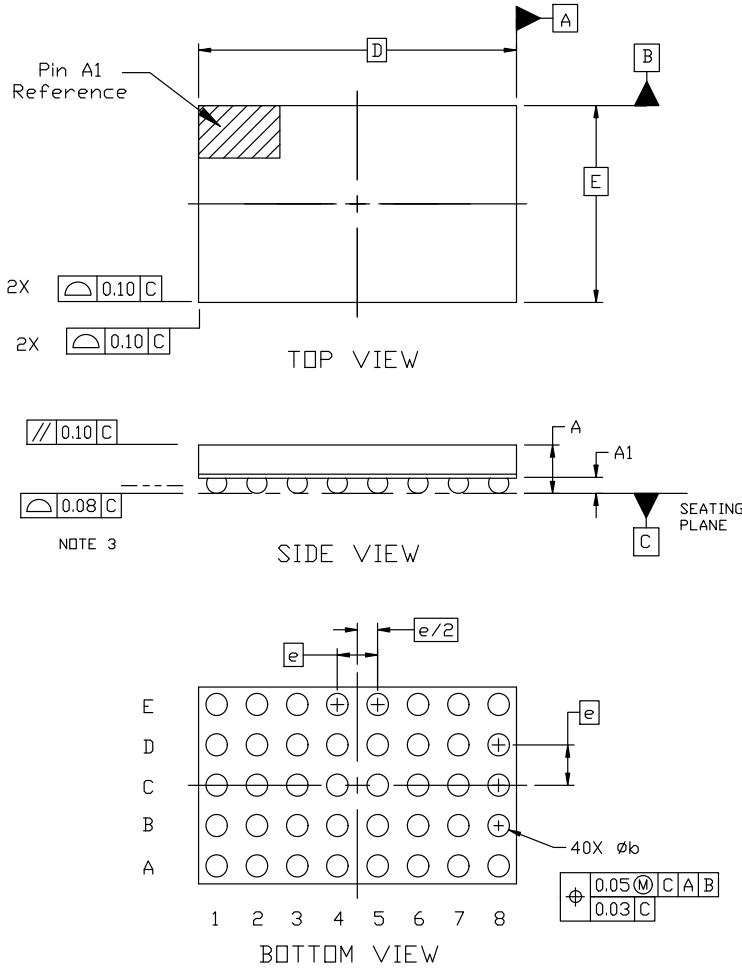
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 4:1

WLCSP40, 2.44x3.94
CASE 567JB
ISSUE A

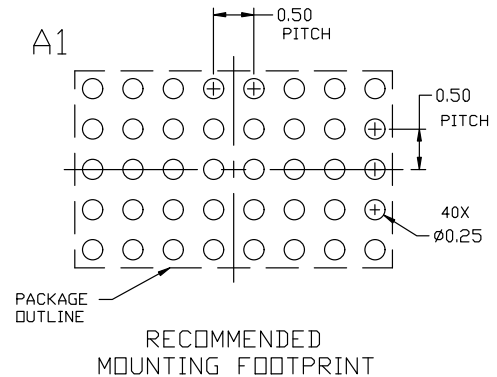
DATE 20 DEC 2022



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN. | MAX. |
| A | --- | 0.65 |
| A1 | 0.14 | 0.24 |
| b | 0.22 | 0.32 |
| D | 3.94 BSC | |
| E | 2.44 BSC | |
| e | 0.50 BSC | |



* For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
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| DESCRIPTION: | WLCSP40, 2.44X3.94 | PAGE 1 OF 1 |

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