HBD853/D
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Energy Efficient Innovations

Power Factor Correction (PFC) Handbook

Choosing the Right Power Factor Controller Solution

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Table of Contents

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Key Contributors

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Dhaval Dalal is a power electronics consultant based in Bangalore, India. From 2002 to 2008, he worked at ON Semiconductor, where he was responsible for defining strategy, roadmaps, and technical content of many products for power supply applications. He holds 5 patents on power conversion. Dhaval has published numerous papers on power management, and presented invited talks on the subject. He has over 25 years of power supply industry experience. Dhaval holds a Bachelor of Technology (EE) degree from IIT−Bombay; a Master of Science in Electrical Engineering degree from Virginia Tech; and a Master of Management of Technology from NTU. He also participates in many initiatives of PSMA.

Patrick Wang is an Application Engineer at ON Semiconductor in Taipei, Taiwan, where he focuses on developing applications solutions and controllers for ac-dc power supplies. Patrick has 18 years of experience in power supply design and applications. He has written multiple application notes on power factor correction; published technical articles on EDN; and led webinars on power efficiency and thermal management. He holds a Bachelor of Control Engineering degree from National Chiao Tung University in Taiwan.

Laurent Jenck is currently Vice President of Marketing and Business Development at Energy Recovery Products. From 1999 to 2012, he worked at ON Semiconductor, where he directed the lighting segment, and previously directed system application engineering, focusing on the development of power supply reference designs. Laurent has 22 years of international experience in product marketing and business/operations management. He holds a Master of Science in Electrical Engineering degree from INSA in Lyon-France, and a Master of Business Administration degree from ASU.

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FOREWORD

Designing power supplies in a global energy efficiency context

Designing power supplies has always been a challenging task. But just as many of the traditional problems have been solved, emerging regulatory standards governing efficiency levels are about to start the cycle over again.

The first phase of this cycle is already well underway and has focused on improving standby power consumption levels (passive mode). The next phase is tackling the tougher problem of improving active mode efficiency levels. Government agencies around the world, driven by the US Environmental Protection Agency (EPA) and its ENERGY STAR® program and by the China National Institute of Standardization (CNIS), are announcing new performance standards for active mode efficiency for power supplies.

The standards are aggressive and it will take the joint efforts of manufacturers and their suppliers (including semiconductor suppliers) to provide solutions that meet the new challenges.

Amidst these trends, power factor correction (PFC) or harmonic reduction requirements as mandated by IEC 61000−3−2 stands out as the biggest inflection point in power supply architectures in recent years. With increasing power levels for all equipment and widening applicability of the harmonic reduction standards, more and more power supply designs are incorporating PFC capability. Designers are faced with the difficult tasks of incorporating the appropriate PFC stage while meeting the other regulatory requirements such as standby power reduction, active mode efficiency and EMI limits.

ON Semiconductor is committed to providing optimal solutions for any given power supply requirement. Our commitment is reflected in providing design guidance in choosing between many options for topology and components. In this handbook we have attempted to provide a detailed comparison between various options for PFC implementation while keeping it in the context of total system requirements. As new technologies and components are developed, the balance of choice may shift from one approach to the other, but the methodology used in this handbook will remain applicable and provide a means for the power supply designer to arrive at the best choice for a given application.

We at ON Semiconductor sincerely hope this book will help you to design efficient, economical PFC circuits for your products. Please see our Web site, www.onsemi.com, for up-to-date information on this subject.

Preface

Choices for the power factor correction solutions range from passive circuits to a variety of active circuits. Depending on the power level and other specifics of the application, the appropriate solution will differ. The advances in the discrete semiconductors in recent years, coupled with availability of lower priced control ICs have made the active PFC solutions more appropriate in a wider range of applications. When evaluating the PFC solutions, it is important to look at them in the context of full system implementation cost and performance.

In this handbook, a number of different PFC approaches are evaluated for a 300 W (400 V, 0.75 A) application. An overview of select single-stage isolated converters including an LED driver is also presented. By providing step-by-step design guidelines and system level comparisons, it is hoped that this effort will help the power electronics designers select the right approach for their application.

Chapter 1 provides a comprehensive overview of PFC circuits and details of operation and design considerations for commonly used PFC circuits.

Chapter 2 describes the methodology used for comparing different active PFC approaches for a given application (400 V, 0.75 A output). It also briefly introduces the proposed approaches.

Chapter 3 contains the design guidelines, discussion and salient operational results for current− and voltage−mode critical conduction mode topologies (CrM).

Chapter 4 contains the design guidelines, discussion and salient operational results for the Frequency Clamped CrM topology.

Chapter 5 contains the design guidelines, discussion and salient operational results for the current-controlled and valley-switching frequency foldback mode topologies (CCFF and VSFF).

Chapter 6 contains the design guidelines, discussion and salient operational results for the continuous conduction mode topology (CCM).

Chapter 7 contains the information on the interleaved PFC topology and salient operational results.

Chapter 8 contains the information on the bridgeless PFC approach and salient operational results.

Chapter 9 contains information on the single stage PFC operation and salient operational results.

Chapter 10 provides a detailed analysis of the results obtained from the three different implementations (CrM, FCCrM and CCM) for the same applications. Comparative analyses and rankings are provided for the topologies for given criteria. It also includes guidelines for the designers based on the results described in the previous chapters.

CHAPTER 1

Overview of Power Factor Correction Approaches

Abstract

Designing power factor correction (PFC) into modern switched-mode power supplies (SMPS) has evolved over the past few years due to the introduction of many new controller integrated circuits (ICs). Today, it is possible to design a variety of PFC circuits with different modes of operation, each with its own set of challenges. As the number of choices has increased, so has the complexity of making the choice and then executing the design. In this chapter, the design considerations and details of operation for the most popular approaches are provided.

Introduction

Power factor correction shapes the input current of off-line power supplies to maximize the real power available from the mains. Ideally, the electrical appliance should present a load that emulates a pure resistor, in which case the reactive power drawn by the device is zero. Inherent in this scenario is the absence of input current harmonics---the current is a perfect replica of the input voltage (usually a sine wave) and is exactly in phase with it. In this case the current drawn from the mains is at a minimum for the real power required to perform the needed work, and this minimizes losses and costs associated not only with the distribution of the power, but also with the generation of the power and the capital equipment involved in the process. The freedom from harmonics also minimizes interference with other devices being powered from the same source.

Another reason to employ PFC in many of today's power supplies is to comply with regulatory requirements. Today, electrical equipment in Europe and Japan must comply with the IEC61000-3-2. This requirement applies to most electrical appliances with input power of 75 W (Class D equipment) or greater, and it specifies the maximum amplitude of line-frequency harmonics up to and including the 39^{th} harmonic. Additionally, many energy efficiency requirements also carry a PFC requirement such as the Energy Star 5.0 for Computers and Energy Star 2.0 for External Power Supplies, and for TV effective November 2008.

Definition

Power factor correction is simply defined as the ratio of real power to apparent power, or:

$$PF = \frac{Real\ Power}{Apparent\ Power} \quad \begin{matrix} (expressed\ in\ Watts) \\ (expressed\ in\ VA) \end{matrix}$$

where the real power is the average, over a cycle, of the instantaneous product of current and voltage, and the apparent power is the product of the rms value of current times the rms value of voltage. If both current and voltage are sinusoidal and in phase, the power factor is 1.0. If both are sinusoidal but not in phase, the power factor is the cosine of the phase angle. In elementary courses in electricity this is sometimes taught as the definition of power factor, but it applies only in the special case, where both the current and voltage are pure sine waves. This occurs when the load is composed of resistive, capacitive and inductive elements and all are linear (invariant with current and voltage).

Switched-mode power supplies present nonlinear impedance to the mains, as a result of the input circuitry. The input circuit usually consists of a half-wave or full-wave rectifier followed by a storage capacitor capable of maintaining a voltage of approximately the peak voltage of the input sine wave until the next peak comes along to recharge the capacitor. In this case current is drawn from the input only at the peaks of the input waveform, and this pulse of current must contain enough energy to sustain the load until the next peak. It does this by dumping a large charge into the capacitor during a short time, after which the capacitor slowly discharges the energy into the load until the cycle repeats. It is not unusual for the current pulse to be 10% to 20% of the cycle, meaning that the current during the pulse must be 5 to 10 times the average current. Figure 1−1 illustrates this situation.

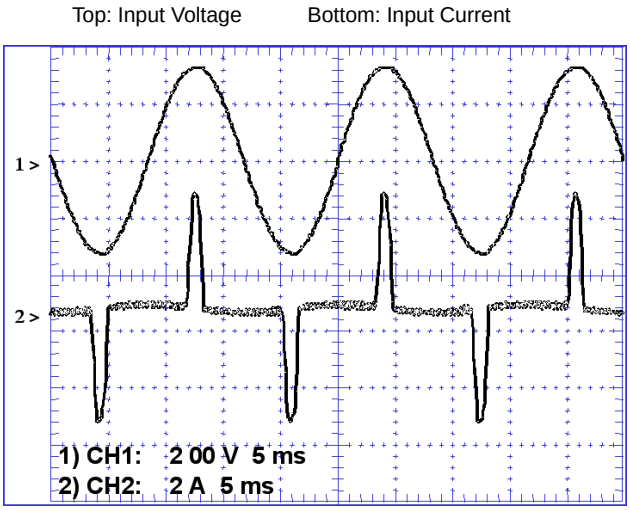


Figure 1−1. Input Characteristics of a Typical Switched-Mode Power Supply without PFC

Note that the current and voltage are perfectly in phase, in spite of the severe distortion of the current waveform. Applying the “cosine of the phase angle” definition would lead to the erroneous conclusion that this power supply has a power factor of 1.0.

Figure 1−2 shows the harmonic content of the current waveform in Figure 1−1. The fundamental (in this case 60 Hz) is shown with reference amplitude of 100%, and the higher harmonics are then given with their amplitudes shown as percentages of the fundamental amplitude. Note that the even harmonics are barely visible; this is a result of the symmetry of the waveform.

Since only the fundamental component produces real power, while the other harmonics contribute to the apparent power, the actual power factor is well below 1.0. This deviation is represented by a term called distortion factor and is primarily responsible for the non-unity power factor in SMPS. The general equation governing the relationship between the real power and apparent power is given by:

Real power expressed in W ↘ ↙ *Apparent power expressed in VA*

$$\langle P_{in} \rangle = V_{in(rms)} \cdot I_{in(rms)} \cdot \cos\varphi \cdot \cos\theta$$

Where cosφ is the displacement factor coming from the phase angle φ between the voltage and current waveforms and cosθ is the distortion factor. Incidentally, the power factor of the power supply with the waveform in Figure 1−2 is approximately 0.6.

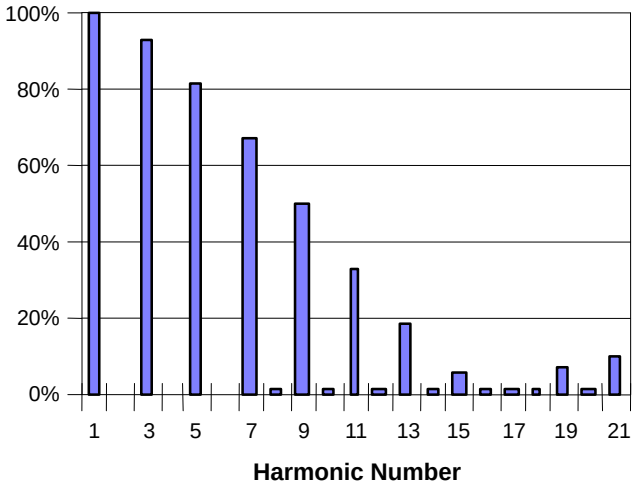


Figure 1−2. Harmonic Content of the Current Waveform in Figure 1−1

For reference, Figure 1−3 shows the input of a power supply with perfect power factor correction. It has a current waveform that mimics the voltage waveform, both in shape and in phase. Note that its input current harmonics are nearly zero.

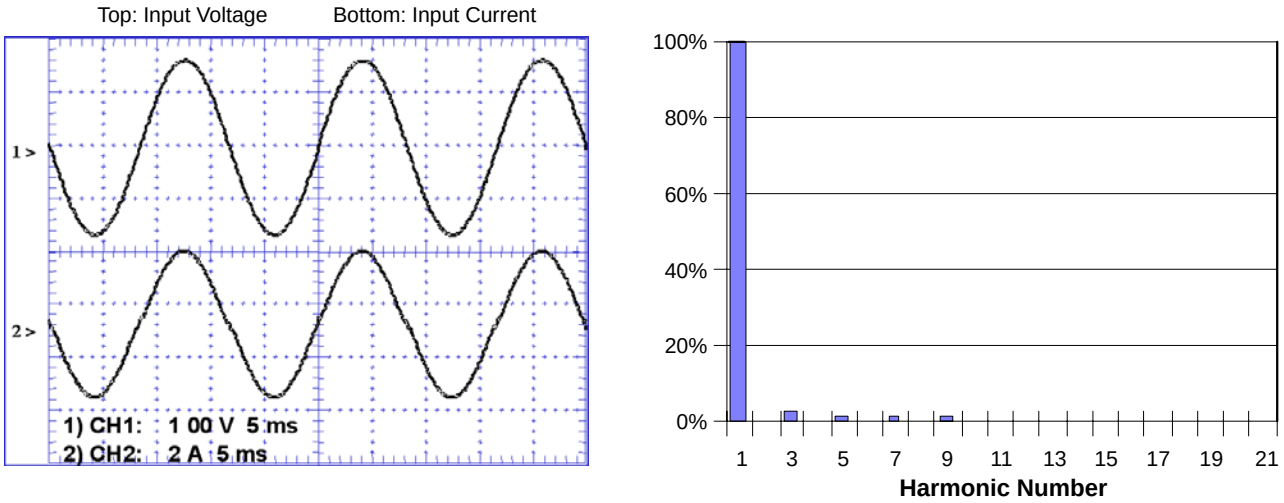


Figure 1−3. Input Characteristics of a Power Supply with Near-Perfect PFC

Power Factor Correction vs. Harmonic Reduction

It is clear from the previous illustrations that high power factor and low harmonics go hand-in-hand. It is generally thought that specifying limits for each of the harmonics will do the better job of controlling the “pollution” of the input current, both from the standpoint of minimizing the current and reducing interference with other equipment. So, while the process of shaping this input current is commonly called “power factor correction,” the measure of its success in the case of the international regulations is the harmonic content. In the case of SMPS, usually the displacement factor is close to unity, so the following relationships between the harmonic distortion and power factor apply.

$$THD(\%) = 100 \cdot \sqrt{\sum_{p=2}^{\infty} \frac{Ip^2}{I_1{}^2}} \qquad \cos\theta = PF = \sqrt{\frac{1}{1 + THD^2}}$$

Here, THD is the Total Harmonic Distortion which is quadratic sum of the unwanted harmonics over the fundamental that gives the relative weight of the harmonic content with respect to the fundamental. The second equation uses the absolute value of THD (not percentage) and demonstrates that THD has to be zero for PF to be unity.

Types of Power Factor Correction

The input characteristics shown in Figure 1−3 were obtained with “active” power factor correction, using a switched-mode boost converter placed between the input rectifier and the storage capacitor, with the converter controlled by a PFC IC (Integrated Circuit) and its attendant circuitry in a manner to shape the input current to match the input voltage waveform. This is the most popular type of PFC used in today’s power supplies, as shown in Figure 1−4. It isn’t the only type, however. There are no rules demanding that the PFC task be accomplished by active circuits (transistors, ICs, etc.). Any method of maintaining the harmonics below the regulatory limits is fair game. It turns out that one inductor, placed in the same location as the active circuit, can do the job. An adequate inductor will reduce the peaks of the current and spread the current out in time well enough to reduce the harmonics enough to meet the regulations. This method has been used in some power supplies where the large size of the inductor and its weight (due to its iron core and copper winding) are not objectionable. At higher power levels, the size and weight of the passive approach become unpopular. Figure 1−5 shows the input characteristics of three different 250 W PC power supplies, all with the current waveforms at the same scale factor. As shown, the peak current levels in passive PFC circuit are still 33% higher than the peak currents in active circuits. In addition, while the harmonic levels of the second levels may meet the IEC61000-3-2, it will fail the more stringent 0.9 PF requirement being imposed by some recent regulations.

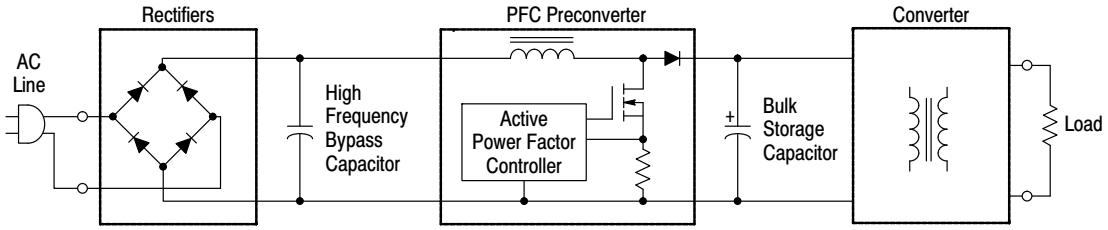


Figure 1−4. PFC Preconverter Stage

In recent years, market trends (rising cost of copper and magnetic core material and falling costs of semiconductors) have tilted the balance decidedly in favor of active PFC even in the most cost-sensitive consumer applications. Coupled with the additional system benefits afforded by the active PFC circuits [1], this seems to be a trend that is likely to continue in the future and lead to more advanced active PFC solutions becoming available to the designers.

Waveforms:
1. Input current with no PFC
2. Input current with passive PFC
3. Input current with active PFC
4. Input voltage

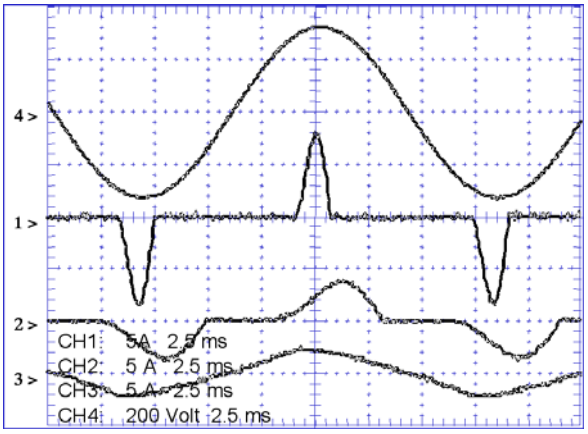


Figure 1−5. Input Characteristics of PC Power Supplies with Different PFC Types (None, Passive, and Active)

Input Line Harmonics Compared to IEC61000-3-2

Figure 1−6 shows the input harmonics of three 250 W PC power supplies, along with the limits according to IEC61000-3-2. These limits are for Class D devices, which include personal computers, televisions and monitors. The harmonic amplitudes are proportioned to the input power of these devices. For lighting products, class C limits are applied, which are also proportional to input power and even more stringent. In the case of other products not used in such high volume, the limits are fixed at the values corresponding to 600 W input. The performance of the passive PFC, as shown in this graph, just barely complies with the limit for the third harmonic (harmonic number 3).

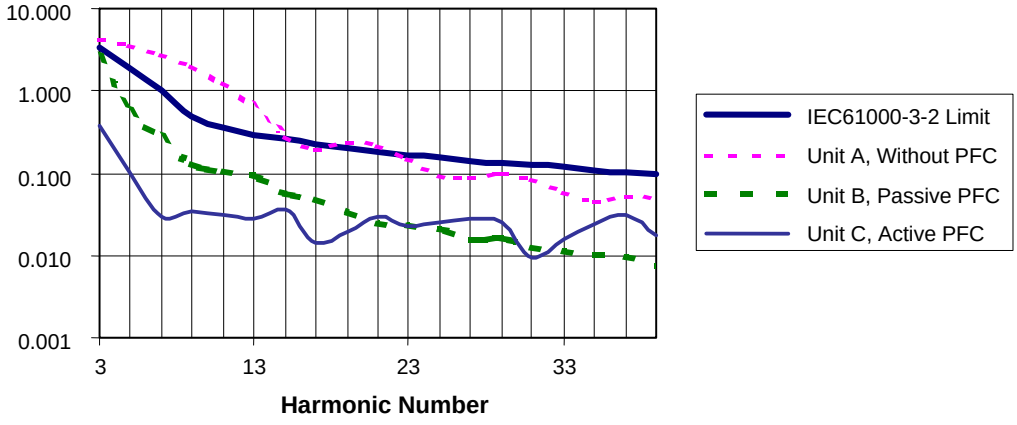


Figure 1−6. Input Harmonics of Three PC Power Supplies Relative to IEC61000-3-2 Limits

Passive PFC

Figure 1−7 shows the input circuitry of the PC power supply with passive PFC. Note the line-voltage range switch connected to the center tap of the PFC inductor. In the 230-V position (switch open) both halves of the inductor winding are used and the rectifier functions as a full-wave bridge. In the 115-V (switch closed) position only the left half of the inductor and the left half of the rectifier bridge are used, placing the circuit in the half-wave doubler mode. As in the case of the full-wave rectifier with 230 Vac input, this produces 325 Vdc (230 • $\sqrt{2}$) at the output of the rectifier. This 325 Vdc bus is, of course, unregulated and moves up and down with the input line voltage.

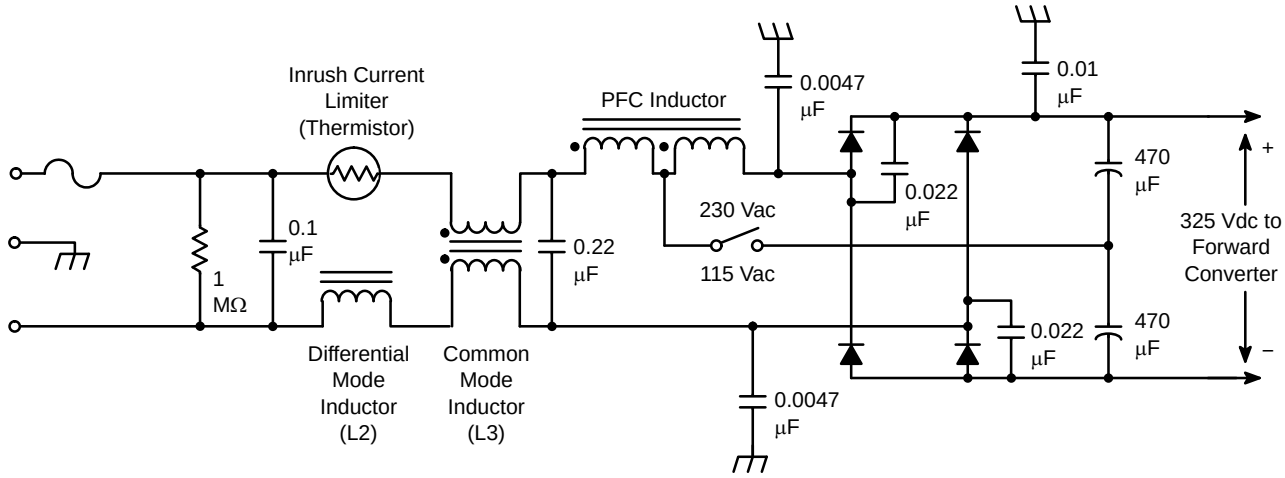


Figure 1−7. Passive PFC in a 250 W PC Power Supply

The passive PFC circuit suffers from a few disadvantages despite its inherent simplicity. First, the bulkiness of the inductor restricts its usability in many applications. Second, as mentioned above, for worldwide operation, a line-voltage range switch is required. Incorporation of the switch makes the appliance/system prone to operator errors if the switch selection is not properly made. Finally, the voltage rail not being regulated leads to a cost and efficiency penalty on the dc-dc converter that follows the PFC stage.

Critical Conduction Mode (CrM) Controllers

Critical Conduction Mode or Transitional Mode (also known as Borderline Conduction Mode BCM) controllers are very popular for lighting and other lower power applications. These controllers are simple to use as well as inexpensive. A typical application circuit is shown in Figure 1−8.

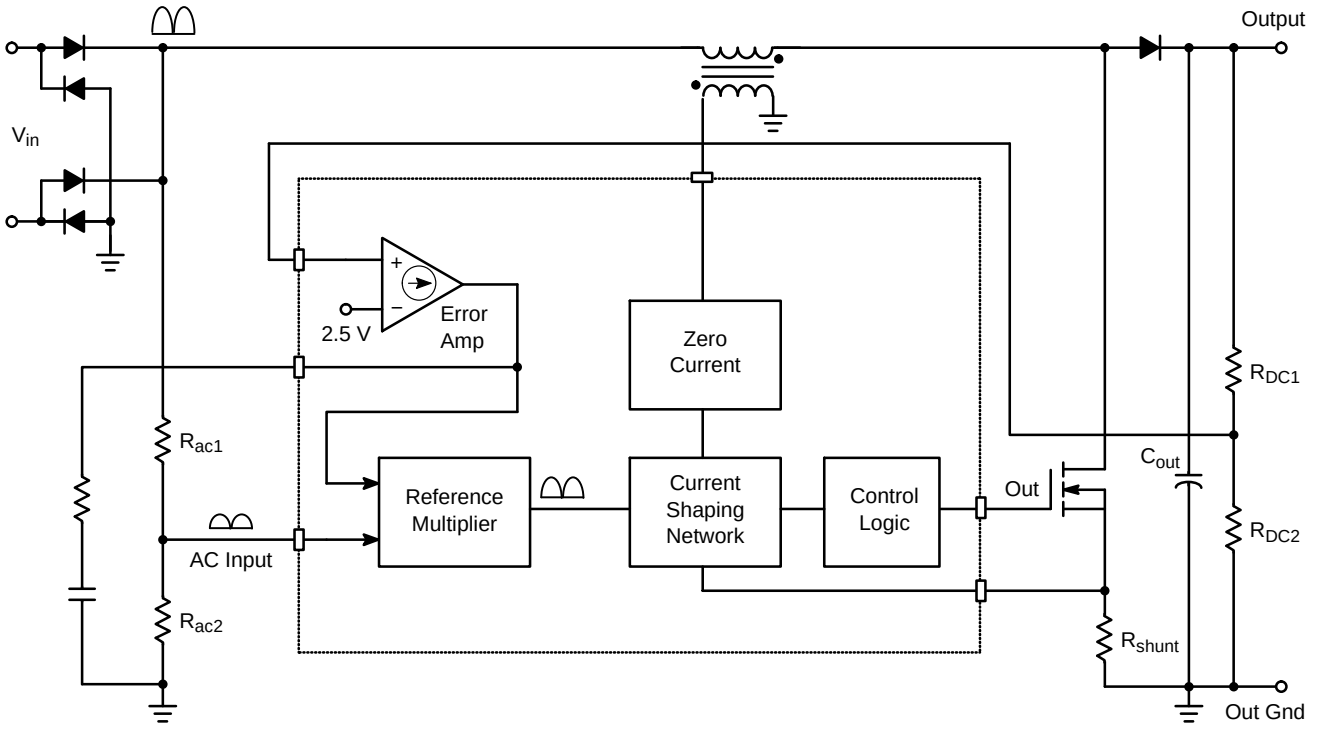


Figure 1−8. Basic Schematic for a Critical Conduction Mode Converter

The basic CrM PFC converter uses a control scheme (current mode control) similar to that shown above. An error amplifier with a low frequency pole provides an error signal into the reference multiplier. The other input to the multiplier is a scaled version of the input rectified ac line voltage. The multiplier output is the product of the near dc signal from the error amplifier and the full-wave rectified sine waveform at the ac input.

The signal out of the multiplier is also a full-wave rectified sine wave that is scaled by a gain factor (error signal), and is used as the reference for the input voltage. The amplitude of this signal is adjusted to maintain the proper average power to cause the output voltage to remain at its regulated value.

The current shaping network forces the current to follow the waveform out of the multiplier, although the line frequency current signal (after filtering) will be half of the amplitude of this reference. The current shaping network functions as follows:

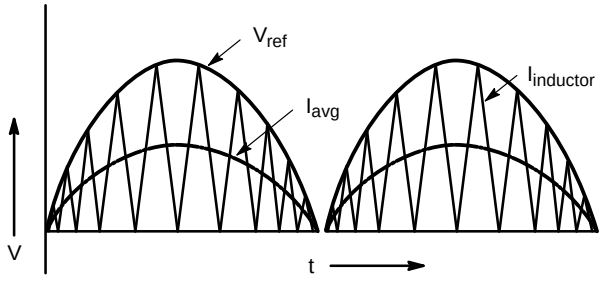


Figure 1−9. CrM Waveforms

In the waveforms of Figure 1−9, Vref is the signal out of the multiplier. This signal is fed into one input of a comparator, with the other input connected to the current waveform.

When the power switch turns on, the inductor current ramps up until the signal across the shunt reaches the level of Vref. At this point the comparator changes states and turns off the power switch. With the switch off, the current ramps down until it reaches zero. The zero current sense circuit measures the voltage across the inductor, which will fall to zero when the current reaches zero. At this point the switch is turned on and the current again ramps up.

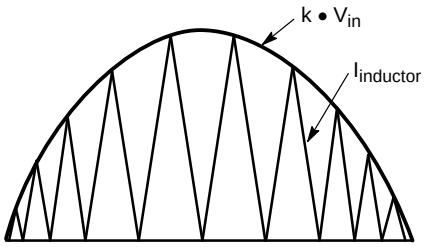
As the name implies, this control scheme keeps the inductor current at the borderline limit between continuous and discontinuous conduction, or critical conduction. This is important, because the wave shape is always known, and therefore, the relationship between the average and peak current is also known. For a triangular waveform, the average is exactly one half of the peak. This means that the average current signal (Inductor current • Rsense) will be at a level of one half of the reference voltage.

The frequency of this type of regulator varies with line and load. At high line and light load, the frequency is at a maximum, but also varies throughout the line cycle (high frequency near zero crossing and low frequency near the peak).

Critical Conduction Mode without a Multiplier (Voltage Mode)

A novel approach to the critical conduction mode controller is available in some ON Semiconductor ICs, most recent example being NCP1607. These chips provide the same input-output function as the controllers described above; however they accomplish this without the use of a multiplier.

As was explained in the previous section, the current waveform for a CrM controller ramps from zero to the reference signal and back to zero. The reference signal is a scaled version of the rectified input voltage, and as such can be referred to as k • Vin, where k is a scaling constant from the ac voltage divider, error amplifier and multiplier in a classic circuit. Given this, and knowing the relation of the slope of the inductor with the input voltage, the following are true:



$$I_{pk} = k \cdot v_{in(t)} \quad and \quad I_{pk} = \Delta I = \frac{v_{in(t)}}{L} \cdot t_{on}$$

Figure 1−10. CRM Current Envelope

Equating the peak current for these two equations gives:

$$k \cdot v_{in(t)} = \frac{v_{in(t)}}{L} t_{on} \qquad Therefore,\ t_{on} = k \cdot L$$

This equation shows that t_{on} is a constant for a given reference signal (k • v_{in}). T_{off} will vary throughout the cycle, which is the cause of the variable frequency that is necessary for critical conduction. The fact that the on time is constant for a given line and load condition is the basis for this control circuit.

In the circuit of Figure 1−11, the programmable one-shot timer determines the on time for the power switch. When the on period is over, the PWM will switch states and turn off the power switch. The zero current detector senses the inductor current, and when it reaches zero, the switch is turned on again. This creates the same dc output as with the classic scheme, without the use of the multiplier. The benefit of the voltage mode CrM control is that the multiplier is not needed and the input voltage sensing network is eliminated. In addition, the current sensing is needed only for protection purpose.

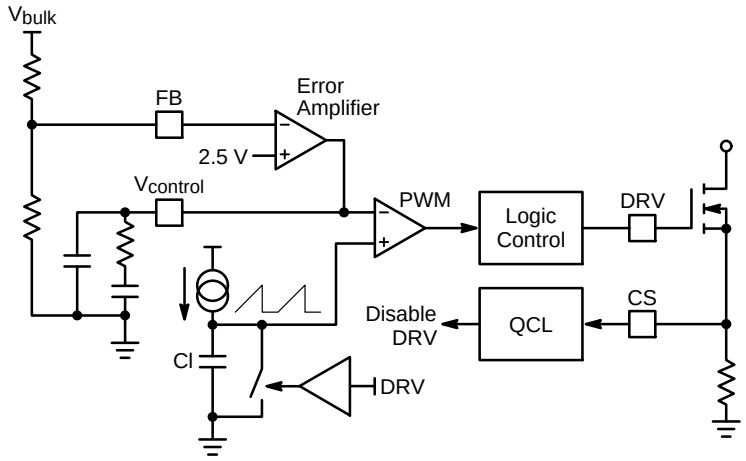


Figure 1−11. Simplified Schematic of CrM Controller Without Multiplier

Since a given value of on time is only valid for a given load and line condition, a low frequency error amplifier for the dc loop is connected to the one-shot. The error signal modifies the charging current and therefore, the on time of the control circuit so that regulation over a wide range of load and line conditions can be maintained.

Frequency Clamped Critical Conduction Mode (FCCrM)

Although the Critical Conduction Mode is widely used in the industry, it has some known limitations. The primary limitation being the variable switching frequency which reaches peak at light loads and also near the zero crossing of the sinusoid. Some solutions which clamped the frequency excursion by putting a maximum frequency clamp resulted in the distortion of current (since the Ton was not adjusted for this) and lower power factor as the inductor entered the discontinuous mode of operation. This is illustrated in Figure 1−12.

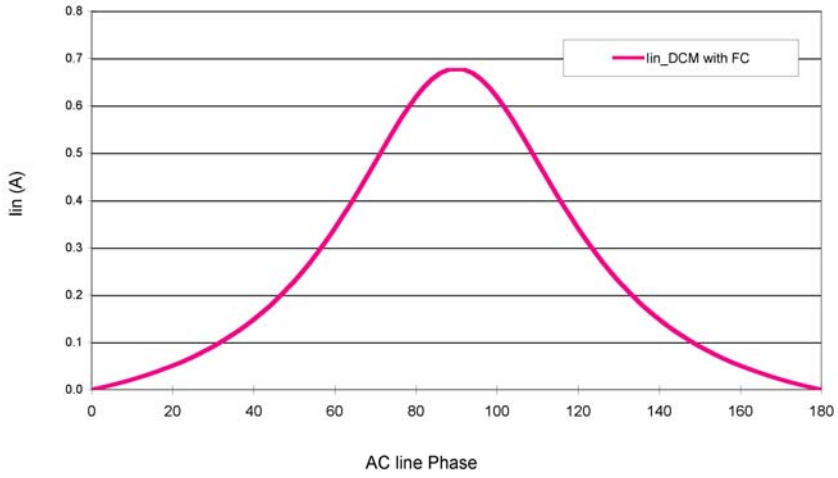


Figure 1−12. CrM Line Current Distortion Due to Frequency Clamping

Recently, a new technique has been introduced which allows true power factor correction even in discontinuous mode (DCM). This technique is summarized in Figure 1−13 and following equations.

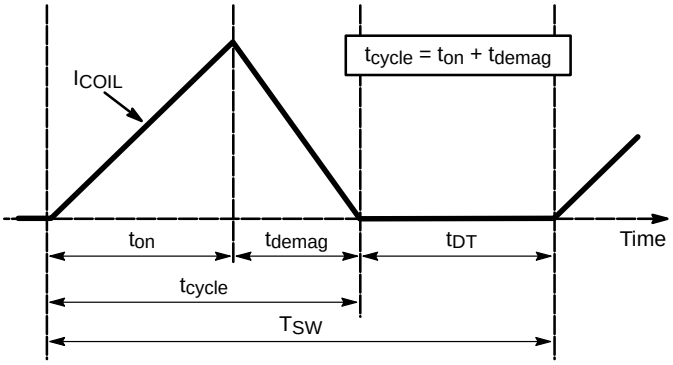


Figure 1−13. DCM Operating Waveforms

With reference to Figure 1−13, the coil peak current is given by:

$$I_{coil,pk} = \frac{v_{in}(t)}{L} \cdot t_{on}$$

The average coil current over a switching cycle (which is also taken as the instantaneous line current for that switching cycle, since the switching frequency is much higher compared to the line frequency at which the line voltage varies) is given by:

$$\langle I_{coil} \rangle_{T_{SW}} = \frac{I_{coil,pk}}{2} \cdot \frac{t_{cycle}}{T_{SW}} = i_{in}(t)$$

Combining these equations and simplifying leads to:

$$i_{in}(t) = \frac{v_{in}(t)}{2 \cdot L} \cdot \left(t_{on} \cdot \frac{t_{cycle}}{T_{SW}} \right)$$

From this equation, we can deduce that, if we devise an algorithm that keeps $t_{on} \bullet t_{cycle} / T_{sw}$ constant for a given load and line condition, we can achieve a sinusoidal line current and unity power factor even in the discontinuous mode. ON Semiconductor has introduced NCP1605 which incorporate this principle.

Despite its benefit of fixed frequency, the DCM is not the ideal mode in all situations as it leads to highest peak current levels. A comparison of the three different modes of operation is shown in Figure 1−14.

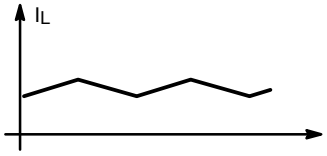
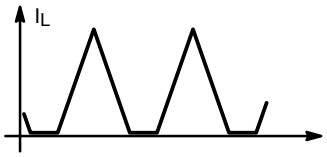
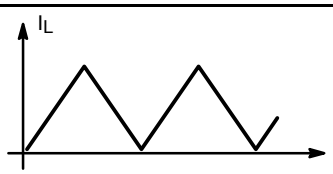
Rating	Symbol	Unit
	**C**ontinuous **C**onduction **M**ode (CCM)	• Always hard-switching • Inductor value is largest • Minimized rms current
	**D**iscontinuous **C**onduction **M**ode (DCM)	• Highest rms current • Reduce coil inductance • Best stability
	**Cr**itical Conduction **M**ode (CrM)	• Largest rms current • Switching frequency is not fixed

Figure 1−14. Comparison of PFC Operating Modes

A more judicious choice would be to allow the PFC to slide between the DCM and CrM modes seamlessly and extract the best of both worlds. So, at light loads, when CrM can go to high switching frequency, it is preferable to go into DCM. Similarly, when the load current is higher, it is desirable to stay in CrM to avoid the high peak currents. This optimization is best depicted by Figure 1−15. NCP1601 and NCP1605 offer programmable frequency clamp that enables selection of appropriate mode boundary. As shown in Figure 1−15, the option 3 is the ideal solution as it combines the best of both worlds (low frequency variation and contained peak currents). More details and results of this mode of operation are provided in Chapter 4.

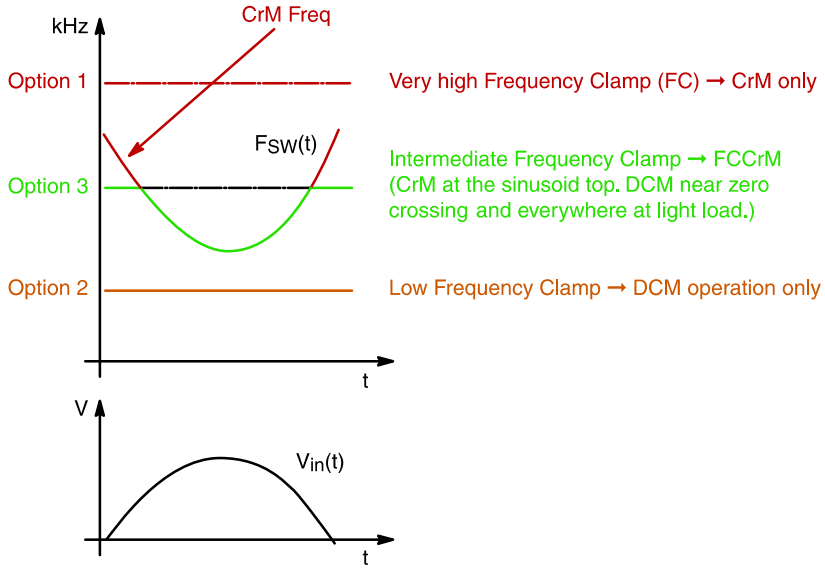


Figure 1−15. PFC Mode Selection Through Frequency Clamping

The NCP1605 contains a number of other features including a circuit that will allow the output voltage to follow the input voltage. This is called follower boost operation (shown in Figure 1−16). In the follower boost mode, the output voltage is regulated at a programmed level above the peak of the input voltage. In most cases, the output of the PFC converter is connected to a dc-dc converter. Many dc-dc converter topologies (e.g. flyback converters) are capable of regulating over a wide range of input voltages, so a constant input voltage is not necessary. On the other hand, if a topology can not function well over a wide input range, the follower boost output range needs to be narrowed (if it is used).

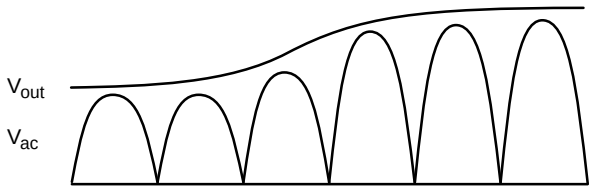


Figure 1−16. Follower Boost

Follower boost operation offers the advantages of a smaller and therefore, less expensive inductor, and reduced on-time losses for the power FET [2]. This is normally used in systems where the lowest possible system cost is the main objective.

Continuous Conduction Mode (CCM) Control

The Continuous conduction mode control has been widely used in a broad range of applications because it offers several benefits. First, the peak current stress is low and that leads to lower losses in the switches and other components. Also, input ripple current is low and at constant frequency, making the filtering task much easier. The following attributes of the CCM operation need further consideration.

Vrms^2 Control

As is the case with many of the PFC controllers on the market, one essential element is a reference signal that is a scaled replica of the rectified input voltage, which is used as a reference for the circuit that shapes the current waveform. These chips all use a multiplier to accomplish this function; however, the multiplier system is more complex than a conventional two-input multiplier.

Figure 1−17 shows the classic approach to continuous-mode PFC. The boost converter is driven by an average current-mode pulse width modulator (PWM) that shapes the inductor current (the converter's input current) according to the current command signal, V_i. This signal, V_i, is a replica of the input voltage, V_{in}, scaled in magnitude by V_{DIV}. V_{DIV} results from dividing the voltage error signal by the square of the input voltage (filtered by C_f, so that it is simply a scaling factor proportional to the input amplitude).

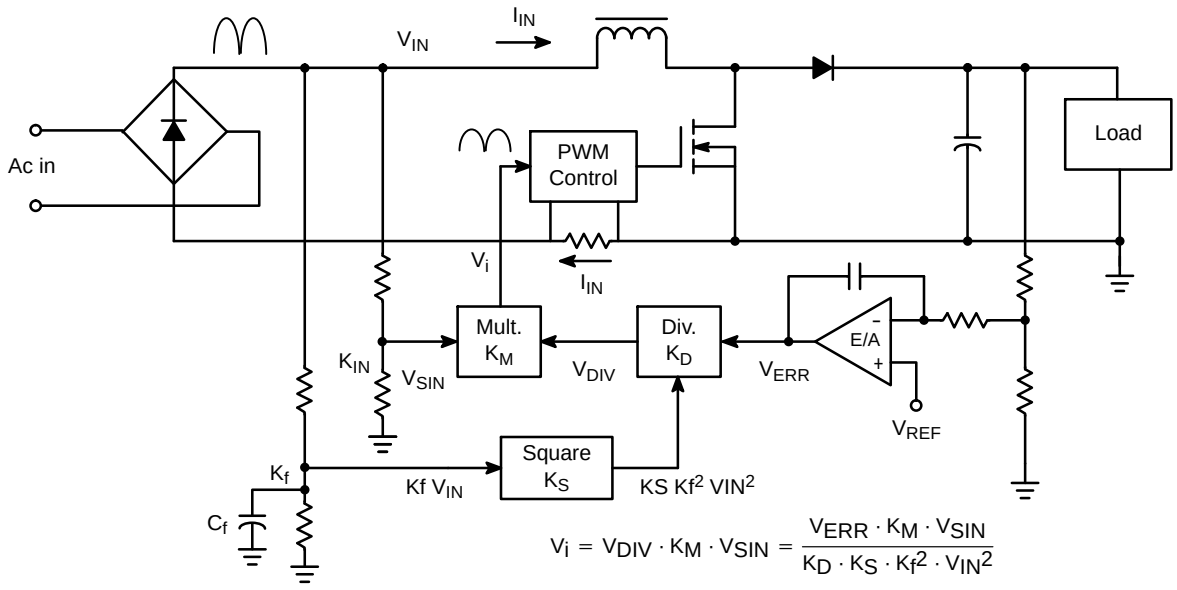


Figure 1−17. Block Diagram of the Classic PFC Circuit

It may seem unusual that the error signal is divided by the square of the input voltage magnitude. The purpose is to make the loop gain (and hence the transient response) independent of the input voltage. The voltage squared function in the denominator cancels with the magnitude of V_{SIN} and the transfer function of the PWM control (current slope in the inductor is proportional to the input voltage). The disadvantage of this scheme lies in the production variability of the multiplier. This makes it necessary to overdesign the power-handling components, to account for the worst-case power dissipation.

Average Current Mode Control

The ac reference signal output from the multiplier (Vi) represents the wave shape, phase and scaling factor for the input current of the PFC converter in Figure 1−17. The job of the PWM control block is to make the average input current match the reference. To do this, a control system called average current mode control is implemented in these controllers [3], [4]. This scheme is illustrated in Figure 1−18.

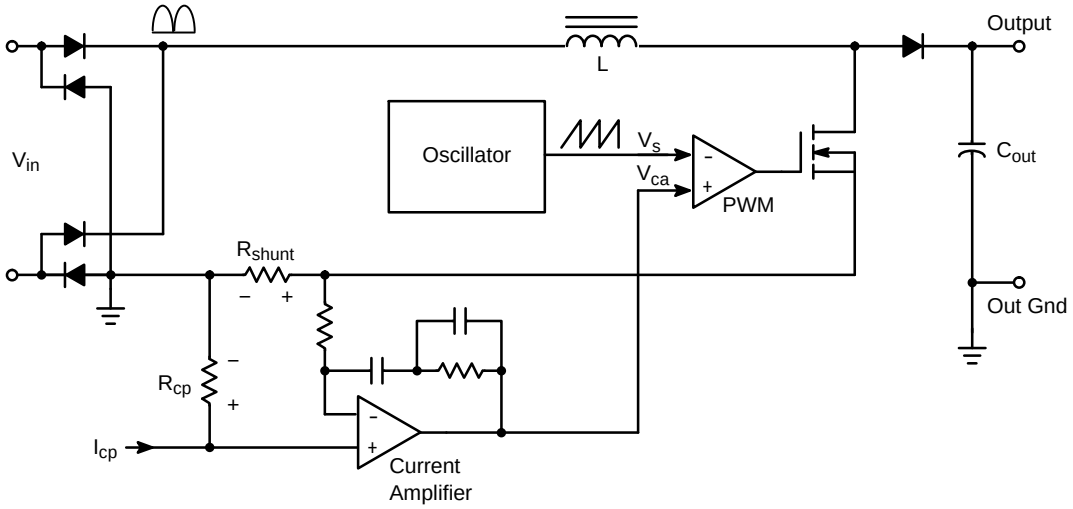


Figure 1−18. Diagram for Average Current Mode Control Circuit

Average current mode control employs a control circuit that regulates the average current (input or output) based on a control signal I_{cp}. For a PFC controller, I_{cp} is generated by the low frequency dc loop error amplifier (and it is simply the current equivalent of the signal Vi as depicted in Figure 1−17. The current amplifier is both an integrator of the current signal and an error amplifier. It controls the wave shape regulation, while the I_{cp} signal controls the dc output voltage. The current I_{cp} develops a voltage across R_{cp}. For the current amplifier to remain in its linear state, its inputs must be equal. Therefore, the voltage dropped across R_{shunt} must equal the voltage across R_{cp}, since there can be no dc current in the input resistor to the non-inverting input of the current amplifier. The output of the current amplifier is a “low frequency” error signal based on the average current in the shunt, and the I_{cp} signal.

This signal is compared to a sawtooth waveform from an oscillator, as is the case with a voltage mode control circuit. The PWM comparator generates a duty cycle based on these two input signals.

ON Semiconductor NCP1650 Family

ON Semiconductor offers a line of highly integrated PFC controllers, with a novel control scheme [5]. This chip’s control circuit uses elements from the critical conduction mode units, as well as an averaging circuit not used before in a power factor correction chip. The basic regulator circuit includes a variable ac reference, low frequency voltage regulation error amplifier and current shaping network.

This chip incorporates solutions to several problems that are associated with PFC controllers, including transient response, and multiplier accuracy. It also includes other features that reduce total parts count for the power converter [6]. The simplified block diagram of this approach is shown in Figure 1−19. More details of this approach can be found in the references provided at the end of this chapter.

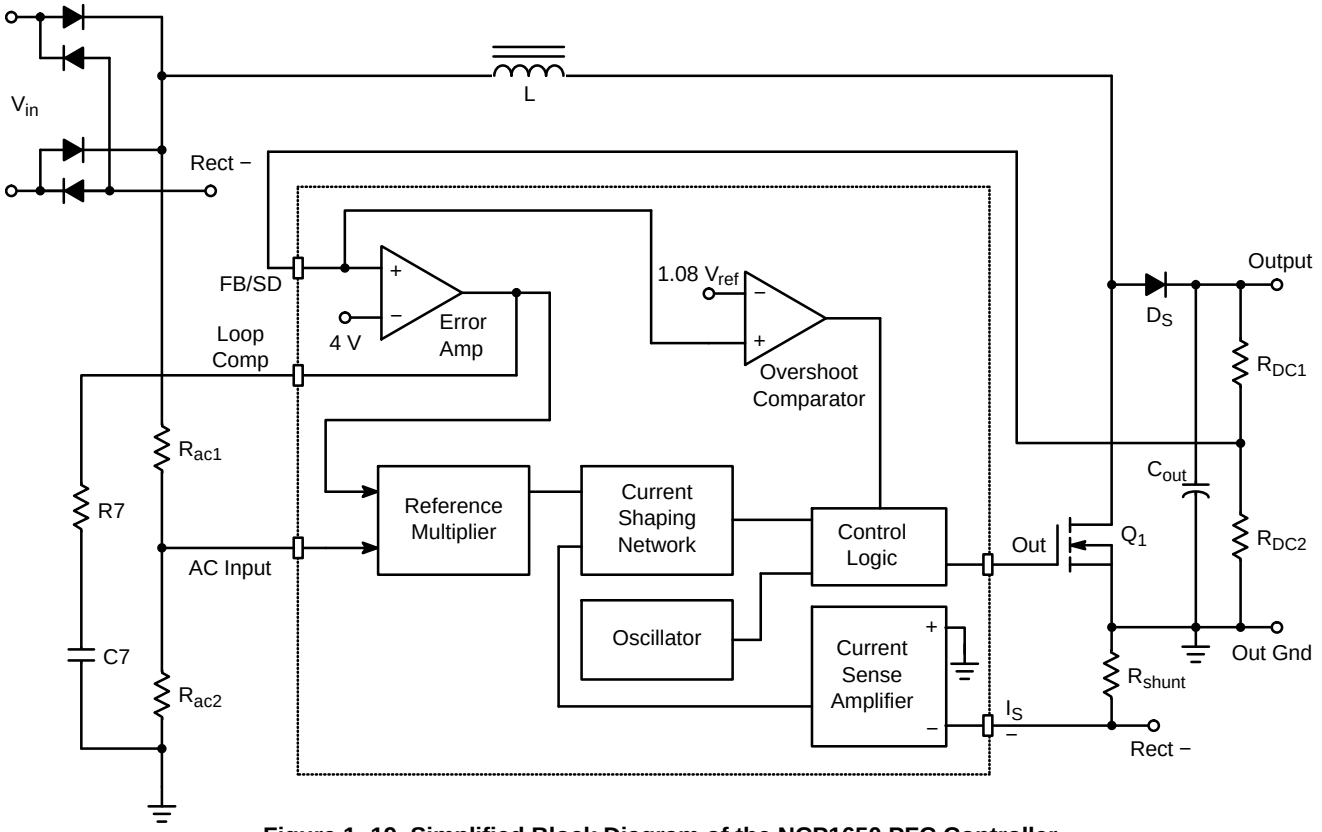


Figure 1−19. Simplified Block Diagram of the NCP1650 PFC Controller

In addition to the NCP1650, which works in a traditional boost PFC topology, the NCP165x family also consists of NCP1652. The NCP1652 allows a single-stage, isolated step-down power conversion with PFC for many low-mid power applications where the output voltage is not very low and can handle some ripple. As shown in Figure 1−20, the NCP1652 based flyback converter provides a uniquely simple alternative to two-stage approaches commonly used. The NCP1652 includes all the relevant significant feature improvements of the NCP1650 and also includes a high-voltage start-up circuitry.

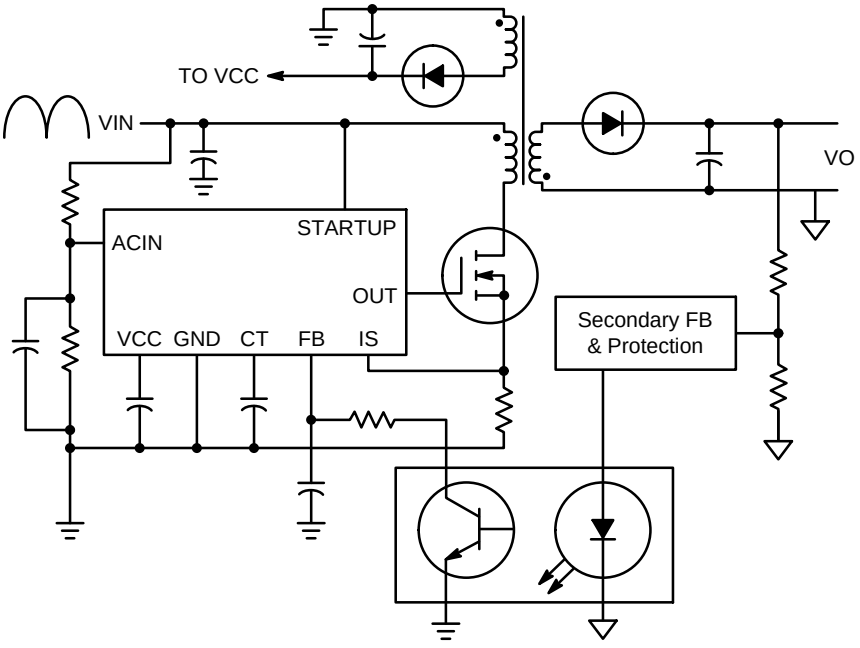


Figure 1−20. Single Stage PFC Using the NCP1652

Predictive Control of CCM PFC

The preceding section outlined some of the inherent complexities of CCM PFC control and how NCP1650 helps overcome some of those complexities. In recent years, a newer control technique has been introduced which greatly simplifies the control algorithm of the CCM PFC controllers. As incorporated in the NCP1653 and NCP1654 from ON Semiconductor, this technique is known as predictive control since it uses the sensed current to determine (predict) the required duty cycle instead of generating the reference signal based on input voltage sensing.

The average inductor current in a system with good PF must be proportional to the input voltage:

$$\langle i_{coil}(t) \rangle_{T_{SW}} = I_{in}(t) \propto V_{in}(t), \text{ and } d_{off} = \frac{V_{in}}{V_{out}}$$

for CCM operation, where d_{off} is the duty cycle of power switch off time.

Hence $d_{off} \propto \langle i_{coil}(t) \rangle_{T_{SW}}$

The way the predictive CCM PFC controller works is to control the power switch on time by summing a ramp signal with a signal proportional to the coil current. As a result, the higher the sensed coil current, lower the on time and higher the off time, satisfying the relationship above. Figure 1−21 shows the current shaping scheme. Some ramp is summed with a signal proportional to the coil current.

$$v_{sum} = V_{sense} + \frac{I_{ref} \cdot t_{on}}{C_{ramp}}$$

The power switch stops conducting when V_{sum} exceeds the current reference. Hence, one can deduct t_{on} and consequently d_{off}.

$$d_{off} = 1 - \frac{t_{on}}{T_{SW}}$$

$$d_{off} = 1 - \frac{(I_{ref} \cdot T_{SW}) - (C_{ramp} \cdot V_{ref})}{I_{ref} \cdot T_{SW}} + \frac{C_{ramp} \cdot V_{sense}}{I_{ref} \cdot T_{SW}}$$

If $I_{ref} \cdot T_{SW} = C_{ramp} \cdot Vref$, i.e. I_{ref}, C_{ramp}, and V_{ref} also act as the oscillator to control the operating frequency, one can obtain

$$d_{off} = \frac{V_{sense}}{V_{ref}} = k \cdot I_{coil}(t)$$

which leads to near-unity power factor. More details on this approach are provided in a later chapter.

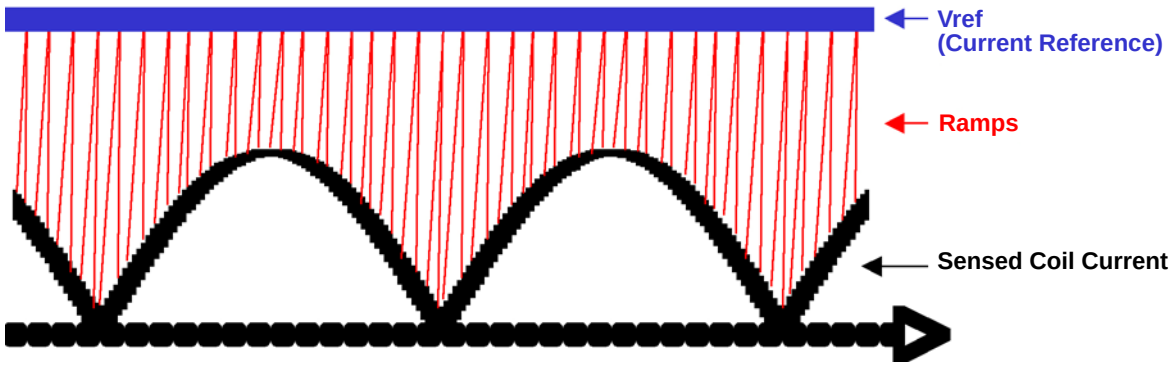


Figure 1−21. Predictive CCM Control Waveforms

Advanced Approaches for PFC

The major control algorithms (CrM, CCM and DCM) and their combinations allow many options for the designers. In addition to these, the search for higher efficiency and modularity has lead to advanced architectures being utilized for the leading edge applications. These approaches are getting into the mainstream applications only now. However, given their highly advanced nature, the designer has to be careful about staying clear of any intellectual property (IP) implications when considering these approaches. In this handbook, two such advanced approaches are presented in later chapters.

The bridgeless PFC solutions arose from the recognition that the diode bridge at the front-end of any PFC typically contributes 2% power losses at full load, low line. If the bridge can either be eliminated or combined with other functions, these losses can be averted. With this in mind, many topologies have been presented in the industry publications and also have been used in some of the higher end applications (UPS being one of them) in the past few years. The bridgeless solutions involve distinctly more complex control and also require acute awareness of the grounding loops when implementing them. Most known implementations involve moving the boost inductor to the ac side of the bridge and replacing the lower diodes of the rectifier bridge with switches in order to replicate boost converters for each leg.

Another recent trend is to apply the interleaving concept to the PFC circuits. In interleaving operation, a single converter is replaced by 2 or more paralleled converters each operating out of phase so that the ripple current when summed at the output or input has a cancelling effect and results in lower filtering requirements. Other benefits of interleaving are modularization, heat dispersion and ability to optimize cost/performance of a smaller module which is much easier due to component availability. Against this, there are potential negatives such as higher component count and a more complex control function.

Component Selection for PFC Circuits

The basic PFC boost converter is one of the simplest converter types (along with buck and buck-boost converters) around. Consequently, the number of components required for power stage is minimal – one inductor, one power switch, one diode and one output capacitor. So, when adding an active PFC circuit to an existing power converter, the component requirements are not very complex. Additional components such as the input bridge and EMI filter are already existent in all ac connected power converters.

While the power stage is simple, the component selection is by no means trivial and there are many critical choices to be made while optimizing the design for required performance. Given the recent trend for higher efficiency, the component selection plays an even more significant role and it has been shown that a proper component selection alone can boost the PFC efficiency by 2-3% for a given topology.

PFC Inductor

The PFC inductor (also referred to as boost inductor or coil or PFC choke), is very important to the operation of the PFC circuit. It must be designed to prevent saturation and consistently provide good power factor. The value of inductance is selected based on commonly available equations. For CCM, the value of inductor tends to be higher than the value for the DCM or CrM operation. However, that does not mean that the size of the inductor is always higher for the CCM operation. The size depends on the inductance value and the rms current through the inductor. The key consideration is in selecting the right core material and winding size for a given inductor. The higher peak-peak current ripple means that the core losses are higher for the CrM operation. It is often more difficult to use a cheap powder iron core for the CrM operation and achieve the required efficiency. The other key consideration is the type of core. Toroids are the most popular because they offer low cost, but if the number of winding turns is high, a bobbin based winding may facilitate easier winding. Some advanced designs use this approach with Ferrite cores to get better flux control.

PFC Diode

The choice of PFC diode plays a crucial role in the efficiency and EMI performance of a CCM boost converter. At the instance of the boost switch turn-on, the diode is carrying significant current in the CCM operation. Since this diode is a high voltage diode, it typically suffers from reverse recovery phenomenon (forced by slower recombination of minority carriers) which adds to the losses and ringing. It is important to use ultrafast diodes (preferably with soft recovery characteristics) to mitigate this problem. In recent years, alternative rectifier solutions based on more advanced materials have been proposed, but cost constraints limit their applicability in mainstream applications. For the CrM or FCCrM operations, the requirement is different since the diode always turns off at zero current and hence there are no reverse recovery issues to be faced. In these applications, the important criterion is to optimize the forward drop of the diode to improve efficiency. ON Semiconductor has recently introduced PFC diodes (MUR550 series) for these applications.

PFC Switch

The choice of PFC switch is based on the cost vs. performance trade-off. The recent advances in MOSFET technology has helped in moving this trade-off more quickly in the direction of higher performance. With a 500 V or 600 V FET, the important issue is to select the FET with right level of $R_{ds(on)}$ to get low conduction losses without increasing switching losses significantly. Blindly selecting the lowest available $R_{ds(on)}$ FET will not yield the highest efficiency and will actually increase the cost of implementation. Of equal importance is effective MOSFET drain capacitance. This capacitance must be charged and discharged every switching cycle. Choosing a MOSFET with low capacitance will reduce switching losses and increase efficiency.

Current Sense Resistor

The current sense resistor is another important contributor to conduction losses and it is important to minimize the voltage drop across it at full load. In higher end designs, this is achieved by employing current sense transformers. However, in more typical designs, the choice of current sense resistor is dictated by the requirements of the PFC controllers. Many controllers require a fixed 1 V signal and that leads to contribution of about 1% losses. In many of ON Semiconductor's PFC controllers, through negative sensing scheme, the current sense signal is user programmable and hence can be optimized further.

Conclusion

The number of choices available to the PFC designer has grown significantly over the past few years. This is due to the increased interest in complying with IEC61000-3-2 and its derivatives, coupled with an enthusiastic spirit of competition among the semiconductor suppliers. The end users reap increasing benefits as PFC becomes better and more cost effective. Power Supply designers benefit from the increasing capability of these IC controllers, with more options available to execute the designs.

On the other hand, the designer's job has become more complicated as a result of the plethora of design approaches at his fingertips. Just surveying them is difficult enough, but understanding each of them well enough to make an informed, cost-effective choice is a big challenge. It has been an objective of this chapter to increase the designer's awareness of this trend and to provide some insight into the details. In the remaining chapters of this handbook, we expand on the individual approaches and attempt to provide benchmarking that will make this selection easier.

References

The following references were chosen for their relevance to the material in this paper, and are but a small sample of the vast library available to the interested reader.

[1] “Boosting Power Supply Efficiency for Desktop Computers”, Dhaval Dalal, Power Electronics Technology Magazine, February 2005. http://powerelectronics.com/mag/power_boosting_power_supply/
[2] “An Innovative Controller for Compact and Cost-Effective PFC Solutions”, Joel Turchi, ON Semiconductor, www.chipcenter.com/analog/tn029.htm.
[3] “High Power Factor Preregulators for Off-Line Power Supplies”, Lloyd H. Dixon, Jr., Unitrode (now Texas Inst.), Power Supply Design Seminar, SEM-800, 1991.
[4] “Average Current Mode Control of Switching Power Supplies”, Lloyd H. Dixon, Jr., Unitrode (now Texas Inst.), Application Note U140.
[5] “NCP1650/D Power Factor Controller”, Rev. 1, Alan Ball, ON Semiconductor, March 2002.
[6] “NCP1650 Benchtop Assistance”, AND8084, Rev 0, Alan Ball, ON Semiconductor, May 2002.

CHAPTER 2

Methodology for Comparison of Active PFC Approaches

There are many different driving factors for designing PFC circuits as outlined in Chapter 1. Depending on end applications requirements and the prominent driving factors, the choice of a PFC circuit will vary. Until very recently, only one or two topologies have been widely utilized for PFC implementations. For higher power circuits, the traditional topology of choice is the boost converter operating in continuous conduction mode (CCM) and with average current mode control (ACMC). For lower power applications, typically the critical conduction mode (CrM) boost topology is utilized. As the range of circuits and applications incorporating PFC has expanded, the need for more diversified PFC solutions has grown. Many of the emerging solutions use variations of the established topologies, while some truly novel techniques have also emerged.

It is often difficult to provide an instantaneous answer to the question: “Which approach is the most suitable for a given application or power range?” The answer depends in part on the design priorities and various trade-offs. However, the other part of the answer lies in benchmarking of different approaches for a given application. In this handbook, results of such a benchmarking effort have been presented with detailed analysis. Previous version of the PFC handbook by ON Semiconductor (published in 2003) also presented similar benchmarking, but the technology enhancements since then have shifted the basis of comparison somewhat.

The choice of a correct application is critical in carrying out such a benchmarking study. It is commonly accepted that at power levels below 200 W, the CrM approach is more appropriate, while for power levels above 300 W, the CCM approach is admittedly sensible. However, in the market, there is no dearth of power supplies which implement CCM at lower power and CrM at higher power – ultimately, it is the designer’s comfort factor that counts. The power range of 200−300 W represents the gray area where either approach could be used. As a result, it is most pertinent to evaluate the performance of different approaches somewhere within this power range. A 270 W (output) power level was chosen as a target application. Also, since most applications are required to operate over universal input voltage (88−264 Vac, 50/60 Hz), that was chosen as the input voltage range. All the systems were designed to a hold-up time (line drop-out) specification of 16 ms (1 line cycle). The output voltage for the benchmarking is chosen to be 385 Vdc which is commonly used for the universal input PFC applications.

Choice of Approaches

From the approaches described in Chapter 1 and other available approaches, following were identified as the suitable candidates for this benchmarking. The accompanying figures for each approach depict the complete system implementation including input filtering.

1. Critical Conduction Mode (CrM) boost converter with fixed output voltage. As shown in Figure 2−1, this approach creates a fixed (385 V) output voltage at the PFC output using NCP1607 – a new voltage mode CrM controller from ON Semiconductor.

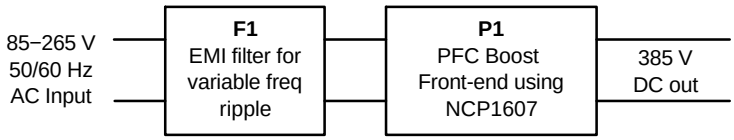


Figure 2−1. Critical Conduction Mode PFC

2. Frequency Clamped Critical Conduction Mode (FCCrM) boost converter with variable output voltage. As shown in Figure 2−2, this approach uses the Frequency Clamped CrM (where the DCM and CrM approaches are judiciously mixed), to generate the 385 V dc output. NCP1605 is used as the PFC controller.

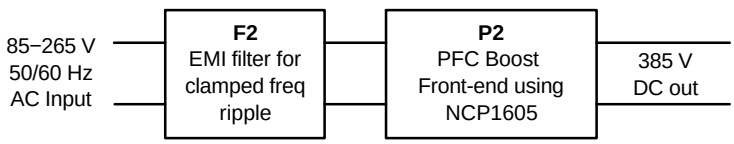


Figure 2−2. Frequency Clamped Critical Conduction Mode PFC

3. Continuous conduction mode boost converter with fixed output voltage. As shown in Figure 2−3, this approach creates a fixed (385 V) output voltage using a CCM boost topology. The NCP1654 is used as the PFC controller for this approach.

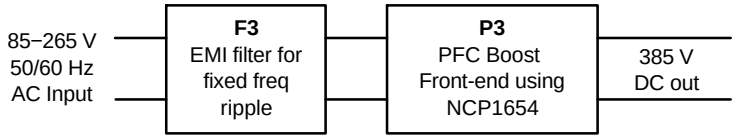


Figure 2−3. Continuous Conduction Mode PFC

4. Interleaved converter with fixed output voltage. Since there is an increasing level of interest in interleaving of PFC, additional benchmarking is provided for the interleaved converter in the same power range as shown in Figure 2−4.

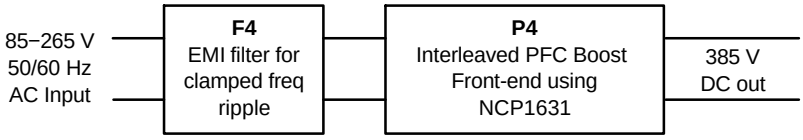


Figure 2−4. Interleaved PFC

Test Methodology

All the above PFC approaches (P1−P4) were designed, built and characterized. Each converter went through minor modifications in order to achieve local optimization without making major component changes. It is recognized that each approach can be optimized further through a more aggressive design and selection of components. However, the focus of this work was to compare the different approaches and the design approach for all the circuits was very similar. Each PFC circuit was tested for the following parameters:

1. Operation over line and load ranges (V_{in} = 85 to 265 Vac, zero to full load)
2. Line and load regulation
3. Input current total harmonic distortion (THD), individual harmonic contributions, and power factor
4. Power Conversion Efficiency (V_{in} = 100, 115, 230 Vac, P_{out} = 20%, 50% and 100% of full load)

The test set-up is depicted in Figure 2−5 below.

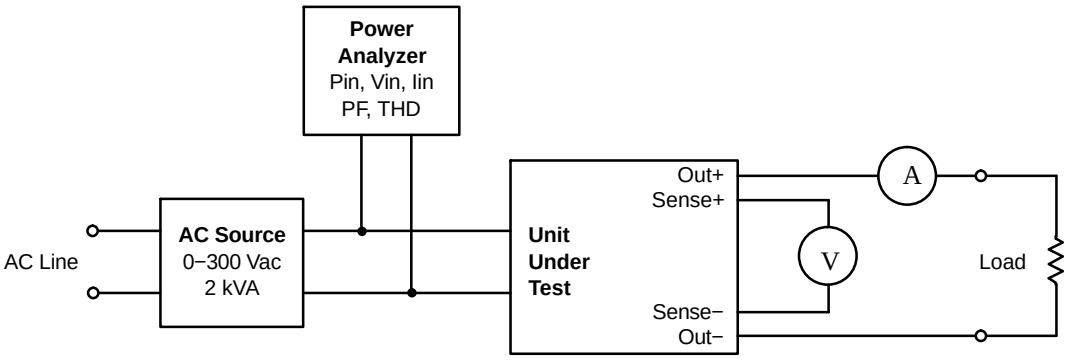


Figure 2−5. Test Set-Up for Performance Measurements

Equipment used for measurements
AC Source: Chroma AC Source (6520)
Power Analyzer: YOKOGAWA Precision Power Analyzer (WT21)
Load: Chroma Electronic Load (63105) was used
Voltmeter: Agilent Digital Multimeter (34401A)
Current Meter: Current measurement were done by the Agilent Digital Multimeter (34401A)

The circuits were tested utilizing an isolated ac source with input voltages ranging from 85 to 265 Vac. Input parameters were measured with the power analyzer. They included input power (Pin), rms input voltage (Vin), rms input current (Iin), power factor level (PF), and total harmonic distortion (THD). All the measurements were made after the circuit was thermally stabilized by operating it at full load and 100 Vac input for 30 minutes.

The output voltage was measured directly at the output sense pins using a Kelvin sensing scheme. There was virtually no current flowing through the sense leads and therefore no voltage drop that can cause an erroneous reading. On the contrary, measuring output voltage across the resistor load can cause a wrong reading as voltage drops occur between the UUT and the load, the voltage drop varying with the amount of current flowing. The load current was measured using the current meter built in the Agilent Digital Multimeter.

The tests were conducted in similar settings for all the boards. However, it should be realized that there is always an element of inaccuracy in PFC power measurements due to the nature of these measurements. This inaccuracy is more pronounced at lighter load conditions, so the reader is advised to take this into account whenever interpreting the results presented in this handbook and also those taken in any lab environment.

Criteria for Comparisons

The comparisons were carried out between the performances of circuits P1−P3. These are summarized in Chapter 10. The key metrics for comparing power systems are cost, size and performance. It is not possible to provide an absolute cost metric for this handbook as the cost structures depend on many factors. However, the comparisons take into account relative costs of different approaches and provide details of the trade-offs involved. The size comparison is based on comparison of the sizes of major power train components for the different approaches.

Trend Chart/Effects on Variations in Conditions

While all the comparisons are made based on identical input and output conditions to provide a true comparative picture, in real life, different applications will have varying requirements. In such cases, one approach or topology may be more suitable for a given application than others. Following variations in operating or applications conditions are explored in Chapter 10.

1. Cost/complexity as a function of power
2. Efficiency as a function of power
3. Filter cost/complexity as a function of power
4. Single Line condition (instead of universal line operation)

CHAPTER 3

Critical Conduction Mode (CrM) PFC

PFC Converter Modes

The boost converter is the most popular topology used in PFC applications. It can operate in various modes such as continuous conduction mode (CCM), discontinuous conduction mode (DCM), and critical conduction mode (CrM). This chapter provides the analysis of the CrM operation using the NCP1607. As shown in Chapter 1, in this mode the inductor current reaches zero before the start of the next cycle and the frequency varies with line and load conditions. One benefit of CrM is that the current loop is intrinsically stable and there is no need for ramp compensation. In addition, the inductor current reaching zero every cycle causes the diode to turn off without reverse recovery losses and enables the use of a less expensive boost diode without performance penalties. Similarly, the MOSFET turn-on can be at a low voltage, which reduces switching losses. This chapter contains the background, design details, and results of a CrM PFC converter. It should be noted that the critical conduction mode is also known as boundary conduction mode (BCM), borderline conduction mode (BCM), and transition conduction mode (TCM). It is also mistakenly referred to as discontinuous conduction mode. The true DCM PFC is different and only recently introduced by ON Semiconductor and is covered in Chapter 4.

Basics of CrM Operation

The overview of the CrM operation is provided in Chapter 1. This chapter presents a detailed view of the basic operation. The power switch ON state and OFF state are the two fundamental states of operation for a CrM converter. Figure 3−1 shows the idealized circuit diagrams and waveforms for each state. A few key equations for understanding the operation of the CrM converter are derived next. The first relationship is derived from the triangular nature of the inductor (coil) current waveform.

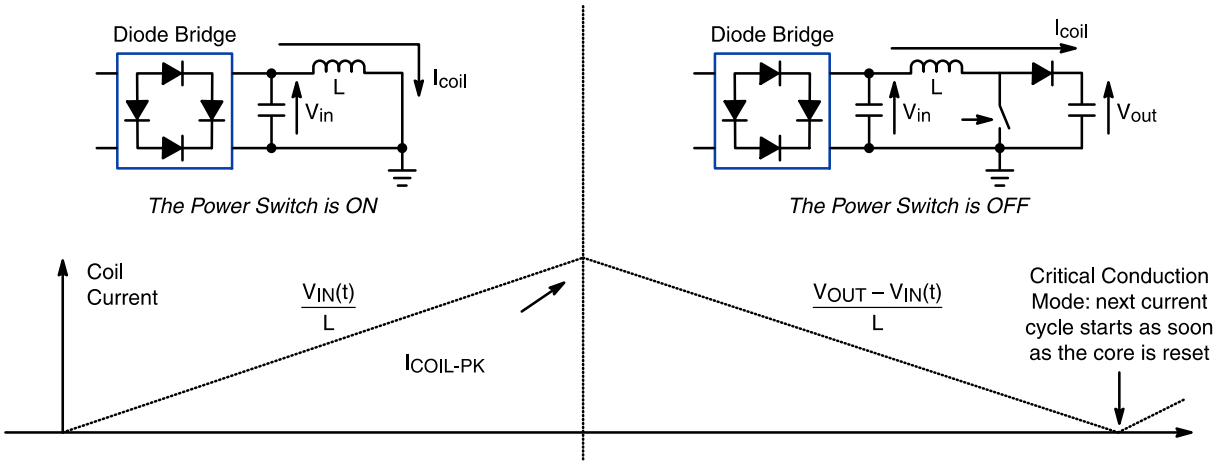


Figure 3−1. States of Operation in Critical Mode Conduction PFC

$$I_{in}(t) = \left\langle I_{coil} \right\rangle_{T\,SW} = \frac{I_{coil,pk}}{2}$$

Where $I_{in}(t)$ is the low (line) frequency instantaneous value of the input current, which is equal to the averaged switching frequency inductor current $<I_{coil}>_{TSW}$. Using this equation and the input voltage and current relationship for unity power factor, it is determined that the on time of the switch is constant for a particular line voltage and load current condition [1]:

$$t_{on} = \frac{2 \cdot P_{in} \cdot L}{Vac^2}$$

As described in chapter 1, this relationship is the basis of the voltage-mode control of the CrM PFC converter. Traditional CrM controllers use current-mode control and industry contains many pin and function compatible, low-cost devices from various semiconductor suppliers. The key common attributes of these controllers are:

- Feedback error processing using a transconductance error amplifier in order to accommodate the overvoltage protection (OVP) function that is critical to PFC operation. Some devices use alternative techniques for OVP detection and managed to retain the use of traditional error amplifier for feedback processing. Pins 1 and 2 are used for this function.
- Multiplier input (Pin 3) that senses the scaled instantaneous input voltage information to create the reference signal for the current waveform.
- Instantaneous current sense input (Pin 4) that is connected to the PWM comparator and protection circuits.
- A zero current detection (ZCD) input (Pin 5) that senses when the inductor current reaches zero and causes the driver to turn on.
- Vcc (Pin 8), Ground (Pin 6) and Driver (Pin 7).

The reasons for success of this function set and pinout are easy to explain, in a very compact package, these features included all the necessary control functionality for the current mode CrM PFC. In addition, the layout is made easy by separation of noise sensitive signals (pins 1−4) and higher noise generation pins (pins 6 and 7). By buffering the driver between Vcc and ground, optimum noise protection is achieved.

NCP1607 – Industry Pin Compatible Voltage Mode CrM Controller

The voltage mode CrM offers certain benefits compared to the current-mode CrM operation, namely:

1. There is no requirement to sense the input voltage through a resistive divider. In addition to reducing component count, it also reduces the power consumption at light or no load conditions. This is a critical feature for compliance with low standby power requirements.
2. The current sense signal is used for protection only and is not used by the PWM comparator. This is beneficial near the input voltage zero crossing where the current sense signal amplitude is low and the possibility of noise injection negatively affecting the circuit performance is high.
3. The lack of a multiplier eliminates a common source of inaccuracies in the circuit.

These benefits make it advantageous to convert from current-mode to voltage-mode control. Due to the popularity and designer familiarity with the traditional CrM controllers, it is important that all the desirable attributes of the current-mode controllers be retained. ON Semiconductor’s NCP1607 and NCP1608 accomplish this objective by retaining the pin out and functionality of the current mode controllers while offering the benefits of the voltage-mode control.

As shown in Figure 3−2, the only change required to convert from current-mode controllers to the NCP1607 or NCP1608 is to modify the components connected to pin 3. The input voltage sense resistors are removed and the multiplier filter capacitor is modified to match the design equation for the timing capacitor for voltage-mode control. All other functionality is retained in the NCP1607 and NCP1608. In many cases, parametric and protection features are enhanced such as the OVP threshold accuracy or the floating pin protection. The NCP1607 incorporates a traditional error amplifier with dynamic OVP sensing based on the feedback path current. The dynamic OVP sensing enables the designer to program the overvoltage threshold. The NCP1608 incorporates a transconductance error amplifier with fixed OVP sensing from the feedback voltage. The advantage of the transconductance error amplifier is that the overvoltage fault is sensed independently of the error amplifier dynamic operation. Both the NCP1607 and NCP1608 offer a low peak current sense threshold (typically 0.5 V) for additional power savings as desired by designers. Additionally, open loop protection (UVP) is provided by both controllers. Finally, the controllers enable the shutdown of the output driver if the FB pin is pulled to ground. The NCP1607 enables the designer to shut down the output driver if the ZCD pin is pulled to ground. More details of the NCP1607 and NCP1608 operation are found in [2] and [3] respectively.

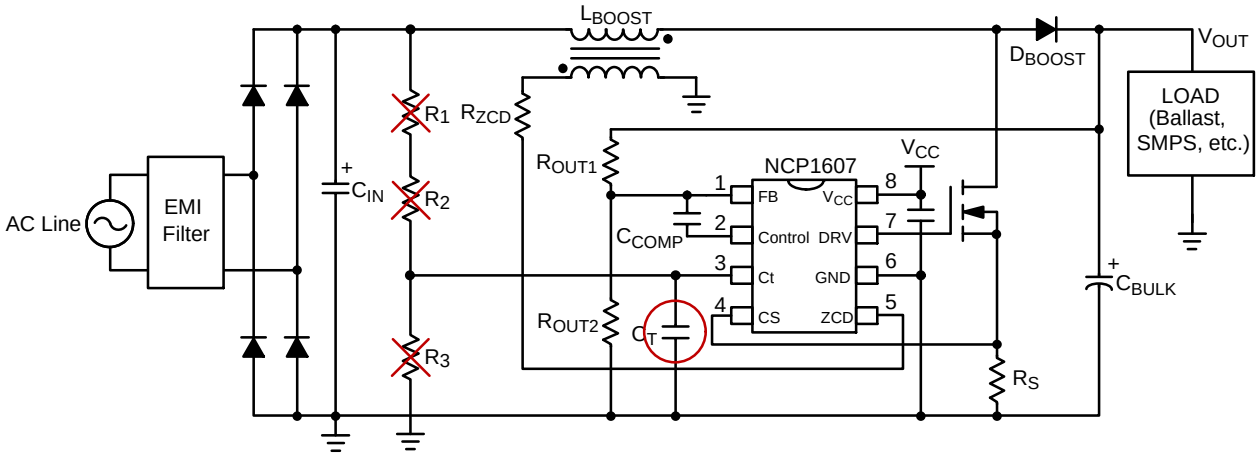


Figure 3−2. Converting from Current-Mode Control to the NCP1607

Design Steps with 270 W Example

The systematic design procedure for CrM PFC using the NCP1607 is performed to illustrate the design of a 270 W CrM PFC converter used as a basis for comparison (design P1 described in Chapter 2).

Step 1: Define the Key Specifications

Equipment used for measurements

Minimum Input voltage (Vac_{LL}): 88 Vac (this is usually 10−12% below the minimum typical voltage, which can be 100 Vac in many countries).

Maximum Input voltage (Vac_{HL}): 264 Vac (this is usually 10% above the maximum typical voltage, which can be 240 Vac in many countries)

Line frequency (f_{LINE}): 50 Hz/60 Hz (This is usually specified in a range of 47−63 Hz and for calculations such as hold-up time, the lowest value specified is used for the calculation)

Output Voltage (V_{out}): 385 V (This value is at least greater than 1.414 • Vac_{HL} and is typically between 385 and 400 V for universal input operation)

Maximum output voltage ($V_{out(max)}$): 415 V (This value is usually 7−10% above the V_{out} value and is determined by the accuracy of the OVP threshold of the PFC controller – conversely, the selection of the PFC controller must be made based on this specification if it is determined by other component stress levels and derating factors).

PFC maximum output power (P_{out}): 270 W (This is the specified output power for the PFC stage. It is important to factor in the follow-on stage efficiency when specifying this parameter – it will always be higher than the specified maximum system output power)

Minimum switching frequency ($f_{sw(min)}$): 40 kHz (This parameter helps set the value of the boost inductor. Choosing it too low increases the inductor size and choosing it too high leads to very high frequency operation near zero crossing and at light loads)

Output voltage ripple ($V_{ripple(p-p)}$): 20 V (This parameter is often specified in percentage of output voltage, ±5% is a very typical specification)

Hold-up time ($t_{hold-up}$): 16 ms (This parameter specifies the amount of time the output remains within a specified limit during line drop-out. One line cycle is typically specified. For PFC alone, this spec is not applicable, but the PFC output capacitor is the single largest determinant of the hold-up time)

Estimated efficiency (η): 93% (This parameter is an initial estimate that is used to size the power stage components. A high level of accuracy is not needed for the design procedure).

Step 2: Design the Boost Inductor (PFC Coil)

The (maximum) peak inductor current is calculated using:

$$I_{coil,pk(\max)} = \frac{2 \cdot \sqrt{2} \cdot P_{out}}{\eta \cdot Vac_{LL}} = \frac{2 \cdot \sqrt{2} \cdot 270}{0.93 \cdot 88} = 9.33A$$

The rms current is calculated using:

$$I_{coil,rms(\max)} = \frac{I_{coil,pk(\max)}}{\sqrt{6}} = \frac{9.33}{2.45} = 3.81A$$

The boost inductor design is calculated using the equation below (generally low line presents the worst case situation, but the following equation should also be applied for the high line condition) :

$$L \geq \frac{\eta \cdot Vac_{LL}^{2} \cdot (\frac{V_{out}}{\sqrt{2}} - Vac_{LL})}{\sqrt{2} \cdot V_{out} \cdot P_{out} \cdot f_{sw(\min)}} = \frac{0.93 \cdot 88^{2} \cdot (\frac{385}{\sqrt{2}} - 88)}{\sqrt{2} \cdot 400 \cdot 270 \cdot 40000} = 225\,\mu\text{H}$$

For this design a 250 μH inductor is chosen, which results in a minimum frequency of 36 kHz. This design uses a Ferrite core (PQ3230, PC40 material) in order to reduce the core losses and litz wire (0.1ϕ • 80) to reduce the skin effect (where current flows only in the periphery of the conductor) and hence the conduction losses.

When designing the inductor, the flux density has to be taken into account. The first point is to keep the flux density low to prevent core from saturation. The ferrite cores have low saturation flux density, 0.25 to 0.5 T, which is temperature dependent. The second point is to get a trade-off point between the usage of flux density and the hysteresis power loss. Based on the lab experience, targeting the peak flux density around 0.25 T seems reasonable:

$$B = \frac{I_{coil,pl(\max)} L}{A_e N} \cdot 10^{4} = \frac{9.33A \cdot 250\mu}{1.67cm^{2} \cdot N} \cdot 10^{4} \leq 0.25T$$

$$N \geq 55.86$$

For this design, a 56-turn winding is implemented using Litz wire as indicated above. The inductor includes a secondary winding to sense the zero current detection (ZCD). The turns ratio for this winding is calculated in Step 4.

Step 3: Select the Timing Capacitor

The voltage mode CrM circuit (NCP1607) operates by setting a fixed on time over the line cycle. This on time changes with the line and load conditions. The on time will be at its maximum value at low line and full load (as that is the time maximum energy has to be transferred to the output). The timing capacitor connected to pin 3 adjusts the maximum on time. The equation for the maximum on time is:

$$T_{ON(\max)} = \frac{2 \cdot L \cdot P_{out}}{\eta \cdot Vac_{LL}^{2}} = \frac{2 \cdot 225 \cdot 10^{-6} \cdot 270}{0.93 \cdot 88^{2}} = 16.87\,\mu\text{s}$$

Next, the value of Ct is calculated using following equation:

$$Ct > \frac{I_{charge} \cdot T_{ON(\max)}}{V_{EA(diff)}} = \frac{297 \cdot 10^{-6} \cdot 16.87 \cdot 10^{-6}}{2.9} = 1.727\ \text{nF}$$

Where I_{charge} and $V_{EA(diff)}$ are the datasheet specified values for the Ct charge current and the error amplifier peak and valley voltages respectively. To ensure that the desired maximum on time can be delivered, the specified maximum and minimum values are used for the numerator and denominator respectively. Based on above calculations, a standard value of 1.8 nF is used in the present design.

Step 4: ZCD Network Design

During the switch off condition, a voltage of (V_{out}-V_{in}) is across the boost inductor. As the current reaches zero, this voltage starts collapsing and ZCD winding senses this event. In order to ensure fail-safe operation, the turns ratio of ZCD winding is selected such that the reflected (V_{out}-V_{in}) voltage is above the ZCD threshold under all conditions as shown in the equation:

$$\frac{N_B}{N_{ZCD}} < \frac{(V_{out} - \sqrt{2} \cdot Vac_{HL})}{V_{ZCDH}} = \frac{(385 - 1.414 \cdot 264)}{2.3} = 5.06$$

The resistor R_{ZCD} (R125) is selected to limit the current into the ZCD pin. If it is selected too low, the current may trigger the ZCD shutdown feature. So, the value of R_{ZCD} is given by:

$$R_{ZCD} \geq \frac{\sqrt{2} \cdot Vac_{HL}}{I_{CL\_NEG}} \cdot \frac{N_{ZCD}}{N_B} = \frac{1.414 \cdot 264}{2.5 \cdot 10^{-3}} \cdot 0.2 = 29.5\,\text{k}\Omega$$

In the design, a 56 kΩ resistor is used. The value of R_{ZCD} is finalized empirically to get the lowest switching losses. The resistor and parasitic (or real) capacitance on the ZCD pin create a short delay circuit that allows the drain voltage of the FET to fall after ZCD condition is reached. If the switch turn-on condition matches the valley of the drain voltage, the switching losses are minimized.

Step 5: Set FB, OVP, and UVP Voltages

The design of the feedback components R_{FB1} and R_{FB2} determine the nominal output voltage, the undervoltage protection threshold, and the overvoltage protection threshold. R_{FB1} sets the overvoltage protection by the following equation:

$$R_{FB1} = \frac{V_{out(\max)} - V_{out}}{I_{OVP}} = \frac{415 - 385}{1 \cdot 10^{-5}} = 3\,\text{M}\Omega$$

R_{FB1} is selected as three 1 MΩ resistors (R130, R131, and R132) due to the high output voltage.

The NCP1607 includes Floating Pin Protection (FPP) that protects the system if the FB pin is floating. FPP is implemented with a pull-down resistor (R_{FB} shown the NCP1607 datasheet). The inclusion of R_{FB} is compensated by adjusting R_{FB2}. The parallel combination of R_{FB} and R_{FB2} form an equivalent resistor R_{EQ} that is calculated using:

$$R_{EQ} = \frac{2.5 \cdot R_{FB1}}{V_{out} - 2.5} = \frac{2.5 \cdot 3 \cdot 10^6}{385 - 2.5} = 19.61\,\text{k}\Omega$$

$$R_{FB2} = \frac{R_{EQ} \cdot R_{FB}}{R_{FB} - R_{EQ}} = \frac{19.61 \cdot 4700}{4700 - 19.61} = 19.7\,\text{k}\Omega$$

R_{FB2} is selected as a standard value of 19.6 kΩ (R134).

Finally, the UVP threshold is given by:

$$V_{out(UV)} = \frac{R_{FB1} + R_{EQ}}{R_{EQ}} \cdot V_{UVP} = \frac{3000 + 19.61}{19.61} \cdot 0.3 = 46\,\text{V}$$

The NCP1607 detects an undervoltage fault when the output voltage is less than $V_{out(UV)}$ and disables the output driver. This feature also protects against open feedback path conditions (missing R_{FB1}).

Step 6: Power Stage Components (MOSFET, Diode, and Current Sense Resistor)

The power stage components are designed based on their current and voltage ratings. The inductor design is covered in step 2. The MOSFET is selected based on peak voltage stress ($V_{out(max)}$ + margin) and rms current stress:

$$I_{M(rms)} = \frac{2 \cdot P_{out}}{\sqrt{3} \cdot \eta \cdot Vac_{LL}} \cdot \sqrt{1 - \frac{8 \cdot \sqrt{2} \cdot Vac_{LL}}{3 \cdot \pi \cdot V_{out}}} = \frac{2 \cdot 270}{\sqrt{3} \cdot 0.93 \cdot 88} \sqrt{1 - \frac{8 \cdot \sqrt{2} \cdot 88}{3 \cdot \pi \cdot 385}} = 3.24\ \text{A}$$

Using a 600 V, 0.19 Ω MOSFET and assuming that $R_{ds(on)}$ increases by 80% due to temperature effects, the conduction losses are:

$$P_{cond} = I_{M(rms)}{}^2 \cdot R_{ds(on)} = 3.24^2 \cdot 0.19 \cdot 1.8 = 3.6\ \text{W}$$

While switching losses are difficult to predict without the details of switching waveforms and diode recovery characteristics, it is assumed that for a CrM PFC, the switching losses are less than the conduction losses. One component of the switching losses that is easily predicted is the capacitive turn-on losses:

$$P_{sw,cap} = \frac{2}{3} \cdot Coss_{25} \cdot \sqrt{25} \cdot V_{on}^{1.5} \cdot f = 0.666 \cdot 780 \cdot 10^{-12} \cdot 5 \cdot (385)^{1.5} \cdot 36000 = 0.71\,\text{W}$$

The nonlinear nature of the capacitance is accounted for in the equation above. As mentioned in step 4, the ZCD network design in reducing the V_{on} from the nominal voltage of 385 V to a much lower value and reduce the losses even more. For CrM operation, the conduction losses dominate. The lowest economically feasible $R_{ds(on)}$ MOSFET is chosen. For this design, the 20 A, 600 V FET with 0.19 ohm $R_{ds(on)}$ was chosen.

The boost diode is a simple selection for CrM since there are no reverse recovery issues. The goal is to choose the correct voltage rating ($V_{out(max)}$ + margin) and lowest forward voltage drop available. The average diode current is the same as the output current ($I_d = P_{out}/V_{out} = 270/385 = 0.7$ A). The losses are simply $I_d * V_f$. The peak current of the diode is equal to the inductor peak current (9.33 A). The chosen diode is the MUR860, which is an ultrafast rectifier with 8 A average and 16 A repetitive peak current rating and 600 V reverse voltage rating.

The current sense resistor is calculated using the peak current and the current sense voltage threshold.

$$R_{sense} = \frac{V_{ILIM}}{I_{coil,pk}} = \frac{0.5}{9.33} = 0.0536\,\Omega$$

In this design, R_{sense} (R100) is selected as 0.04 Ω, which provides 33% margin over the maximum peak current. The dissipation in the sense resistor is calculated using:

$$P_{Rsesnse} = I_{M(rms)}^2 \cdot R_{sense} = 3.24^2 \cdot 0.04 = 0.42\,\text{W}$$

Step 7: Output Capacitor Design

The output capacitor is designed considering three factors: output voltage ripple, output current ripple, and the hold-up time. The output voltage ripple is calculated using:

$$V_{ripple(p-p)} = \frac{P_{out}}{2 \cdot \pi \cdot f_{line} \cdot C_{out} \cdot V_{out}}$$

The capacitor rms current is calculated using:

$$I_{Cout(rms)} = \sqrt{\frac{32 \cdot \sqrt{2} \cdot P_{out}^2}{9 \cdot \pi \cdot Vac_{LL} \cdot V_{out} \cdot \eta^2} - \left(\frac{P_{out}}{V_{out}}\right)^2}$$

However, it is common to size the value of the capacitor based on the hold-up time that is calculated using:

$$t_{hold-up} = \frac{C_{out} \cdot (V_{out}^2 - V_{\min}^2)}{2 \cdot P_{out}}$$

In this case, a 220 μF capacitor is selected to satisfy the conditions above. The peak-peak ripple is 10 V, the rms current is 1.87 A, and the hold-up time is 18.6 ms (for V_{min} = 320 V).

These major design steps enable the functional prototype to be built and tested. In addition to these steps, other common steps such as Vcc generation, feedback compensation, and inrush limiting are required to complete the design. These steps are not covered here as they follow conventional methods.

Circuit Schematic and Bill of Materials

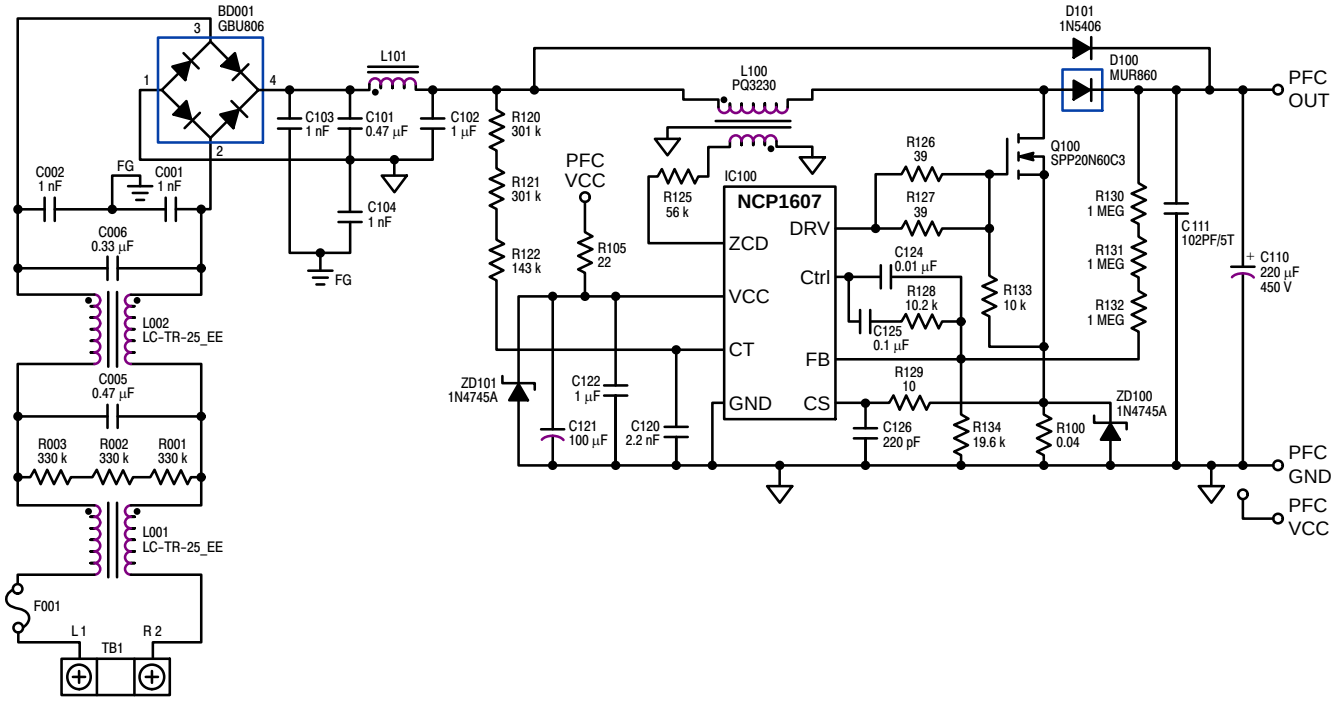


Figure 3−3. Schematic of NCP1607 Based PFC Converter

Table 3−1. Bill of Materials for CrM Board

Reference	Quanity	Part
BD001	1	GBU806
C001, C002, C103, C104	4	1nF
C005, C101	2	0.47μF
C006	1	0.33μF
C102, C122	2	1μF
C110	1	220μF
C111	1	102PF/5T
C120	1	2.2nF
C121	1	100μF
C124	1	0.01μF
C125	1	0.1μF
C126	1	220pF
D100	1	MUR860
D101	1	1N5406
F001	1	FUSE 5*20 (Axial Lead)
IC100	1	NCP1607
L001, L002	2	CHOKE (EMI Choke)
L100	1	PQ3230
L101	1	CHOKE (Power Choke)
Q100	1	SPP20N60C3
R001, R002, R003	3	330k
R100	1	0.04
R105	1	22
R120, R121	2	30k
R122	1	143k
R125	1	56k
R126, R127	2	39
R128	1	10.2k
R129	1	10
R130, R131, R132	3	1MEG
R133	1	10k
R134	1	19.6k
TB1	1	AC inlet
ZD100	1	1N4733A
ZD101	1	1N4745A

Results and Analysis

The results for the 270 W design based on the NCP1607 are shown in Table 3−2 below.

Table 3−2. Performance Results for the 270 W PFC Based on NCP1607

Vin (Vac)	Pin (W)	Vo (V)	Io (A)	Output Power (W)	Po	Efficiency	PF	THD
100	28.91	386.97	0.071	27.43	10%	94.88%	0.954	18.2
	42.24	387.04	0.104	40.40	15%	95.63%	0.971	14.4
	56.93	387.10	0.141	54.59	20%	95.89%	0.970	11.7
	141.59	387.24	0.350	135.60	50%	95.77%	0.996	5.9
	287.10	387.30	0.704	272.53	100%	94.93%	0.998	3.7
115	28.57	386.88	0.070	27.06	10%	94.72%	0.927	23.1
	41.96	386.97	0.104	40.20	15%	95.80%	0.960	15.8
	56.62	387.02	0.141	54.49	20%	96.24%	0.972	14.4
	140.57	387.16	0.350	135.56	50%	96.44%	0.993	8.0
	283.52	387.28	0.700	271.19	100%	95.65%	0.998	4.0
230	28.63	387.21	0.071	27.57	10%	96.29%	0.533	100.0
	42.18	387.04	0.105	40.82	15%	96.78%	0.642	100.0
	55.64	387.07	0.140	54.10	20%	97.23%	0.762	74.1
	137.85	386.89	0.349	135.00	50%	97.93%	0.892	30.5
	275.48	387.06	0.699	270.63	100%	98.24%	0.970	12.3

As shown in Table 3−2 the efficiency of the circuit is nearly 95% at 100 Vac and full load. The efficiency is comfortably higher than 95% for all other line conditions between 15% and 100% load. The wide load range where the efficiency is high is attributable to low switching losses for the CrM operation. The THD at high line and full load is measured to be 12.3% with a PF of 0.97. This is within the allowable range of the IEC61000-3-2 harmonics requirements as depicted in Figure 3−4. The PF and THD performance at light load and high line is not that great for this board. The reasons for this are the distortions applied by the propagation delays.

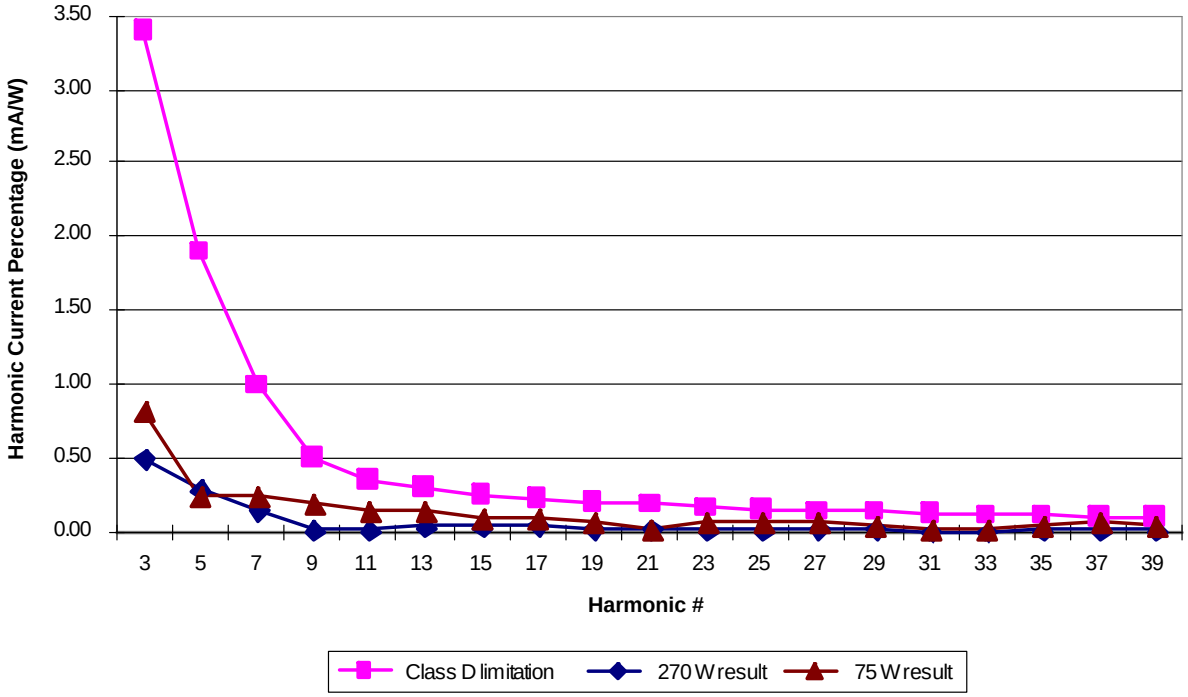


Figure 3−4. Harmonic Content of NCP1607 Based PFC Converter at Full Load and 75 W

The no load power consumption of the circuit is given in Table 3−3. As shown, the no load losses are higher at low line. The no load losses are greater at low line because of the large difference between the input and output voltages. The large difference between the input and output voltages requires increased switching to boost the input voltage up to the output voltage..

Table 3−3. No Load Power Consumption

Vin	Pin (W)
100 Vac	1.084
115 Vac	0.974
230 Vac	0.526

The efficiency optimization involves component tuning. For example, the diode and the MOSFET selections are made using different combinations and the results are compared. For this design, two types of diodes are evaluated. The MUR550, which is a diode designed for CrM and FCCrM applications and MUR860, which is a standard 600 V ultrafast rectifier. In addition, the MOSFET was changed from 20 A to 15 A and its effect was observed. The results are shown in Table 3−4.

Table 3−4. Efficiency Change as a Result of Major Component Changes

100 Vac			115 Vac		
100% load	15 A FET	20 A FET	100% load	15 A FET	20 A FET
5 A diode (MUR550)	93.5%	94.4%	5 A diode (MUR550)	95.1%	95.6%
8 A diode (MUR860)		94.9%	8 A diode (MUR860)		95.7%
20% load	15 A FET	20 A FET	20% load	15 A FET	20 A FET
5 A diode (MUR550)	95.0%	95.7%	5 A diode (MUR550)	95.7%	96.1%
8 A diode (MUR860)		95.9%	8 A diode (MUR860)		96.2%

From Table 3−4, it is clear that the combination of the 8 A diode and 20 A FET provides the highest efficiency results. However, at 115 Vac, the difference between performance results is not large. The impact of the FET on efficiency performance is easy to explain. The conduction losses scale with $R_{ds(on)}$ and increase significantly as the FET $R_{ds(on)}$ increases. By contrast, the efficiency difference between the MUR550 and the MUR860 is not easy to explain.

The relevant operating waveforms of the circuit at full load and 115 Vac input are shown in Figure 3−5. Here, Ch1 is the input voltage (the captured waveform is taken at the peak of the input votlage), Ch2 is the inductor current, which shows the CrM nature of the circuit, Ch3 is the Vds of the main FET, and Ch4 is the Vgs.

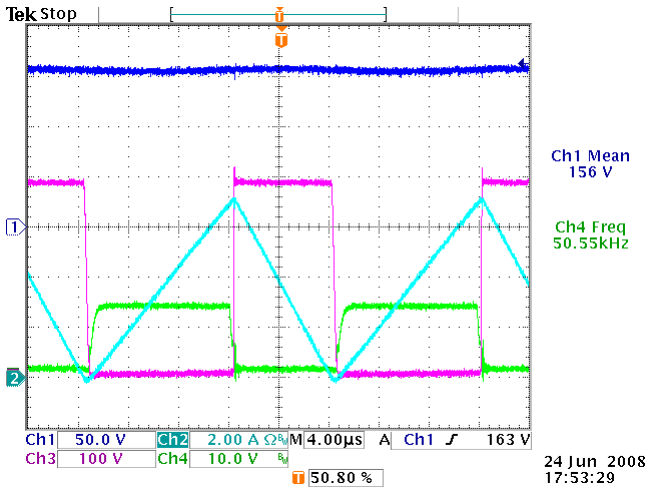


Figure 3−5. Operating Waveforms at Full Load, 115 Vac

The switching frequency of the CrM varies over a wide range with line, load, and the phase angle. Figure 3−6 shows these variations at the peak of the line voltage for low line and high line operations. Also included in the figure are the measured values at some corners. As shown there, the theoretical low line frequency range is 36 kHz to 360 kHz from full load to 10% load. The measured full load frequency matches the theoretical value closely. However, the measured frequency at light load and low line is much lower than the theoretical value. This difference can be ascribed to the internal propagation delays and forward drops which make the actual values different from idealized values used in calculations. The actual frequency being much lower than calculated value is good news from the viewpoint of EMI and light load efficiency. However, the propagation delays also lead to higher distortion in the input current waveform which reduces the PF and increases THD.

Similar results are plotted for the zero crossing instances in Figure 3−7. The difference in the calculated and measured values is apparent and is attributed to the same factors described above. One interesting difference between the two plots is that for zero crossing, the low line frequencies are lower compared to the high line values, while the sinusoid peak shows exactly opposite behavior. At high line, the peak is higher, so the frequency range from zero crossing to sinusoid peak will be wider. Thus, even starting from a smaller number at the peak, it goes to much higher peak during one-half line cycle.

In general, the zero crossing distortion is increased for CrM operation at high line. This is because the theoretical frequency is never reached due to inherent circuit propagation delays. The result is that the PF decreases and THD is increases.

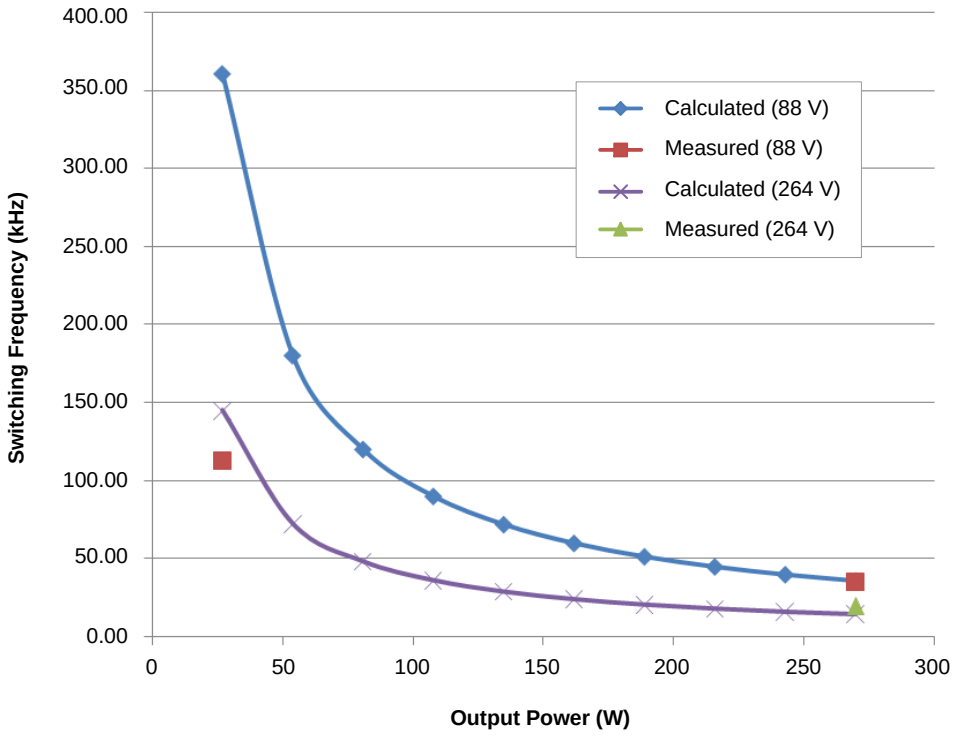


Figure 3−6. Frequency Variation at the Peak of the Sinusoid in CrM PFC

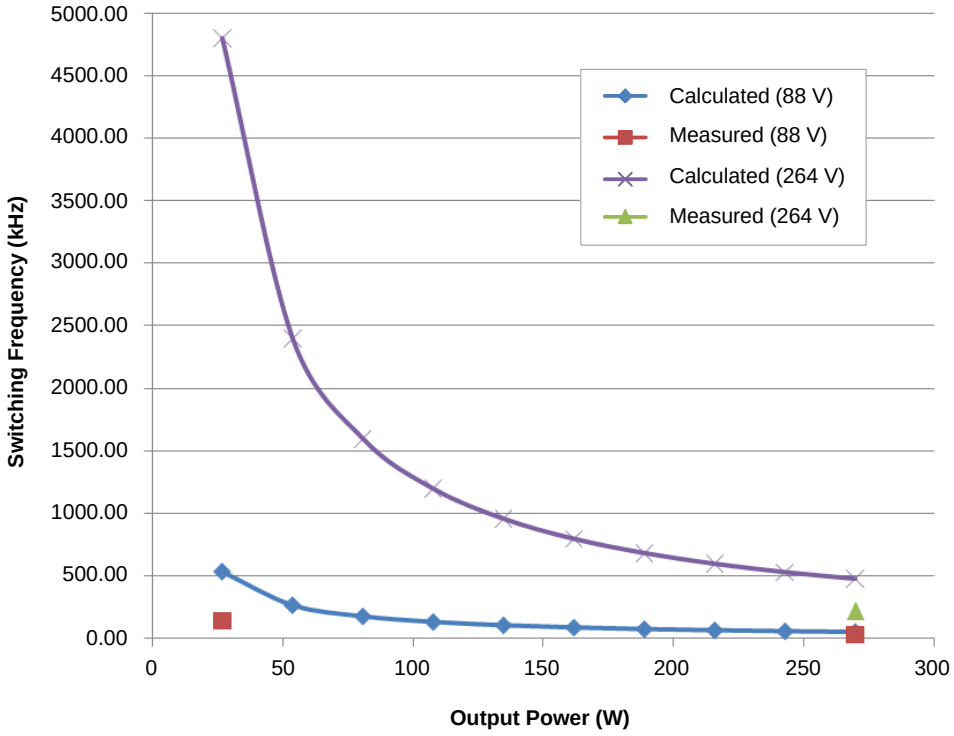


Figure 3−7. Frequency Variation at Zero Crossing in CrM PFC

Following figures provide the graphical representation of the data shown in Table 3−2.

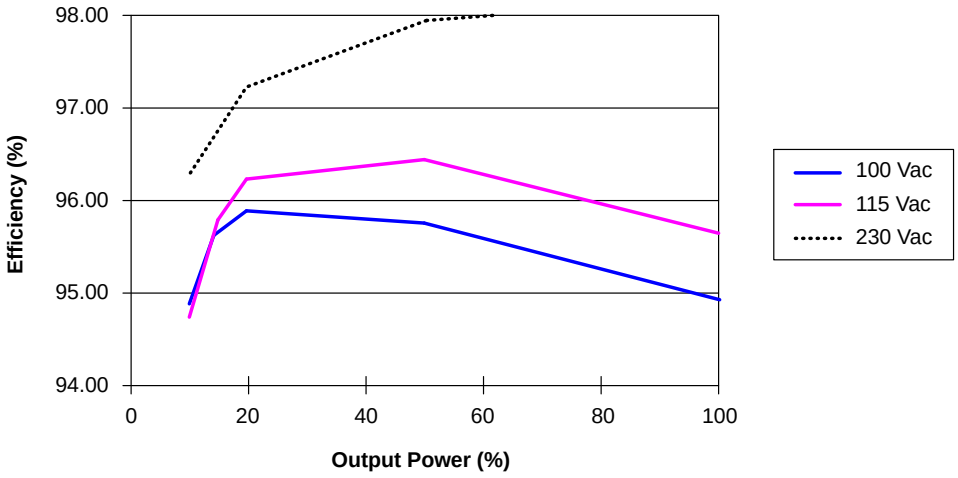


Figure 3−8. Efficiency Performance Over Line and Load

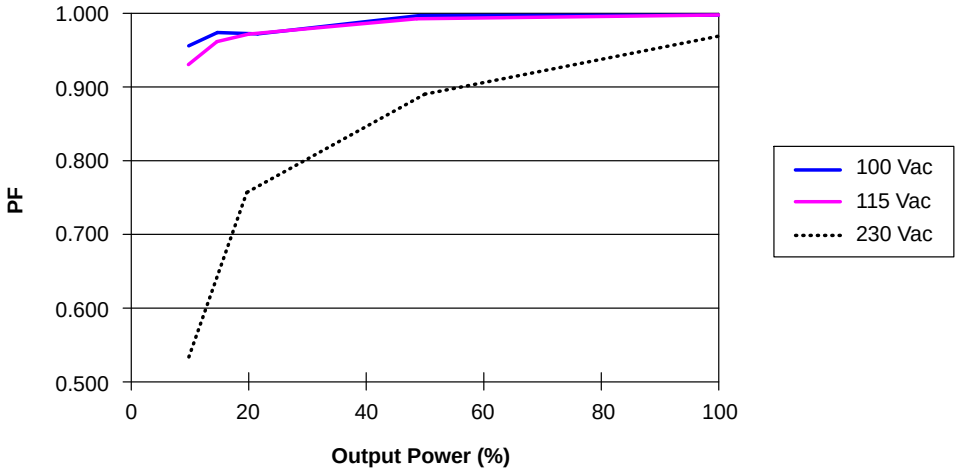


Figure 3−9. Power Factor Performance Over Line and Load

References

[1] “Power Factor Correction Stages Operating in Critical Conduction Mode”, AND8123/D, ON Semiconductor. http://www.onsemi.com/pub_link/Collateral/AND8123−D.PDF
[2] “Implementing Cost Effective and Robust Power Factor Correction with the NCP1607”, AND8353/D, ON Semiconductor. http://www.onsemi.com/pub/Collateral/AND8353−D.PDF
[3] “Implementing Power Factor Correction with the NCP1608”, AND8396/D, ON Semiconductor. http://www.onsemi.com/pub/Collateral/AND8396−D.PDF

CHAPTER 4

Frequency Clamped Critical Conduction Mode (FCCrM) PFC

Introduction

The Critical Conduction Mode (CrM) described in Chapter 3 offers many advantages, especially for low power applications. However, the results and the characteristics also showed some limitations of the approach at light load conditions. The prominent limitation was that the frequency range of the converter varies significantly over line and load conditions. In the design example used in Chapter 3, at high line and full load, the frequency will go from 14.5 kHz at the peak of the sinusoid to 480 kHz near the zero crossing. At lighter loads, this frequency range gets even wider. Theoretically, the frequency has to go to a few MHz to achieve the PFC under light load and high line conditions. However, in practice, the inherent delays within the controllers and in surrounding circuits limit the switching frequency (also, some CrM controllers such as the NCP1605 offer frequency clamp mechanisms to limit the frequency excursion). Limiting of the switching frequency helps limit the EMI generation and also cuts down the magnetic core losses and filter requirements. However, they come at a price of distortion in the power factor, especially near the zero crossings, where the frequency tends to get to its highest level. Thus, a designer always faces a trade-off between keeping the maximum frequency too low and letting it go high.

This difficulty has led to development of a new control approach called the Frequency Clamped Critical Conduction Mode (FCCrM).

Basics of FCCrM Operation

The overview of the FCCrM operation was already provided in Chapter 1. Here, let us take a more detailed view of the basic operation. Since the key differentiation between the CrM and FCCrM is when the converter operates in fixed frequency mode (DCM), we will examine that in detail. The operation in the CrM follows what was described in Chapter 3. There are three fundamental states of operation in DCM – Boost Switch ON state, OFF state with current conduction and OFF state with no current conduction. Figure 4−1 provides the idealized circuit waveforms for these states. A few key equations for the understanding the operation of the DCM mode can be derived next. The first relationship was derived from the nature of the inductor (coil) current waveform in Chapter 1:

$$I_{in(t)} = \frac{V_{in(t)}}{2 \cdot L} \cdot \left(t_{on} \cdot \frac{t_{cycle}}{T_{SW}} \right)$$

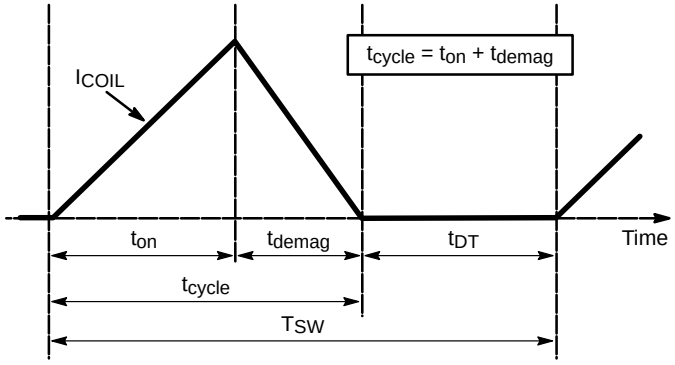


Figure 4−1. States of Operation in Discontinuous Conduction Mode PFC

This relationship between the input current and input voltage points to a PFC control algorithm that can be implemented to make the quantity (t_{on} • t_{cycle}/T_{SW}) constant over a line cycle (for a given set of line and load conditions). This is achieved by including a switched amplifier block as shown in Figure 4−2 that integrates two different values to equal the error amplifier input voltage. This results in:

$$V_{ton} = \frac{T_{sw} \cdot V_{control}}{t_{cycle}}$$

Where $V_{control}$ is the voltage at the error amplifier output which represents the line and load conditions and V_{ton} is the voltage presented to the timing comparator that sets the on time. Since the timing comparator controls the on time such that it is proportional to V_{ton}, we get:

$t_{on} \propto V_{ton}$ and $\frac{t_{on} \cdot t_{cycle}}{T_{sw}} \propto V_{control}$ which is constant over a line cycle.

This yields the desired power factor algorithm. This algorithm is patented and incorporated in two of ON Semiconductor's offerings – NCP1605 and NCP1631. The NCP1605 is an advanced feature set controller. NCP1631 is an interleaved FCCrM PFC controller, which will be depicted in Chapter 7. In this design, the advance feature set of NCP1605 was used and it is described in the next section.

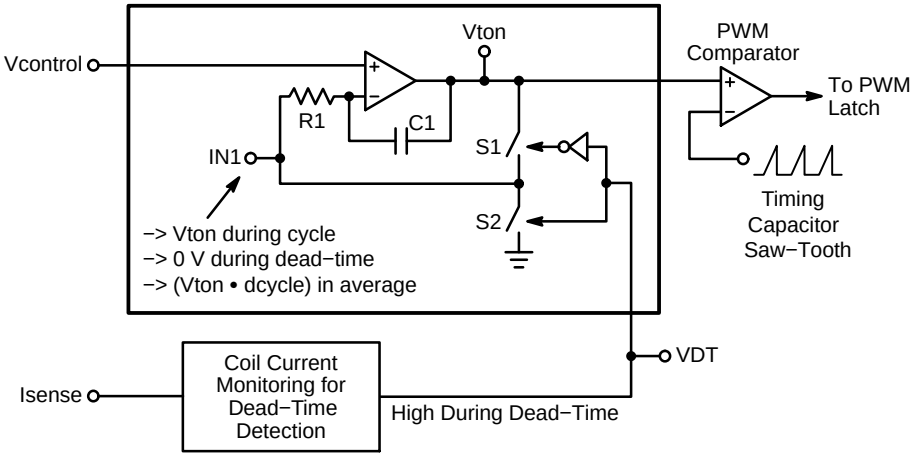


Figure 4−2. DCM PFC Algorithm to Modulate on Time

NCP1605 – Advanced Feature Set FCCrM Controller

Figure 4−3 shows the block diagram of the NPC1605 PFC controller. It has many features to ease and optimize the implementation of PFC in the system.

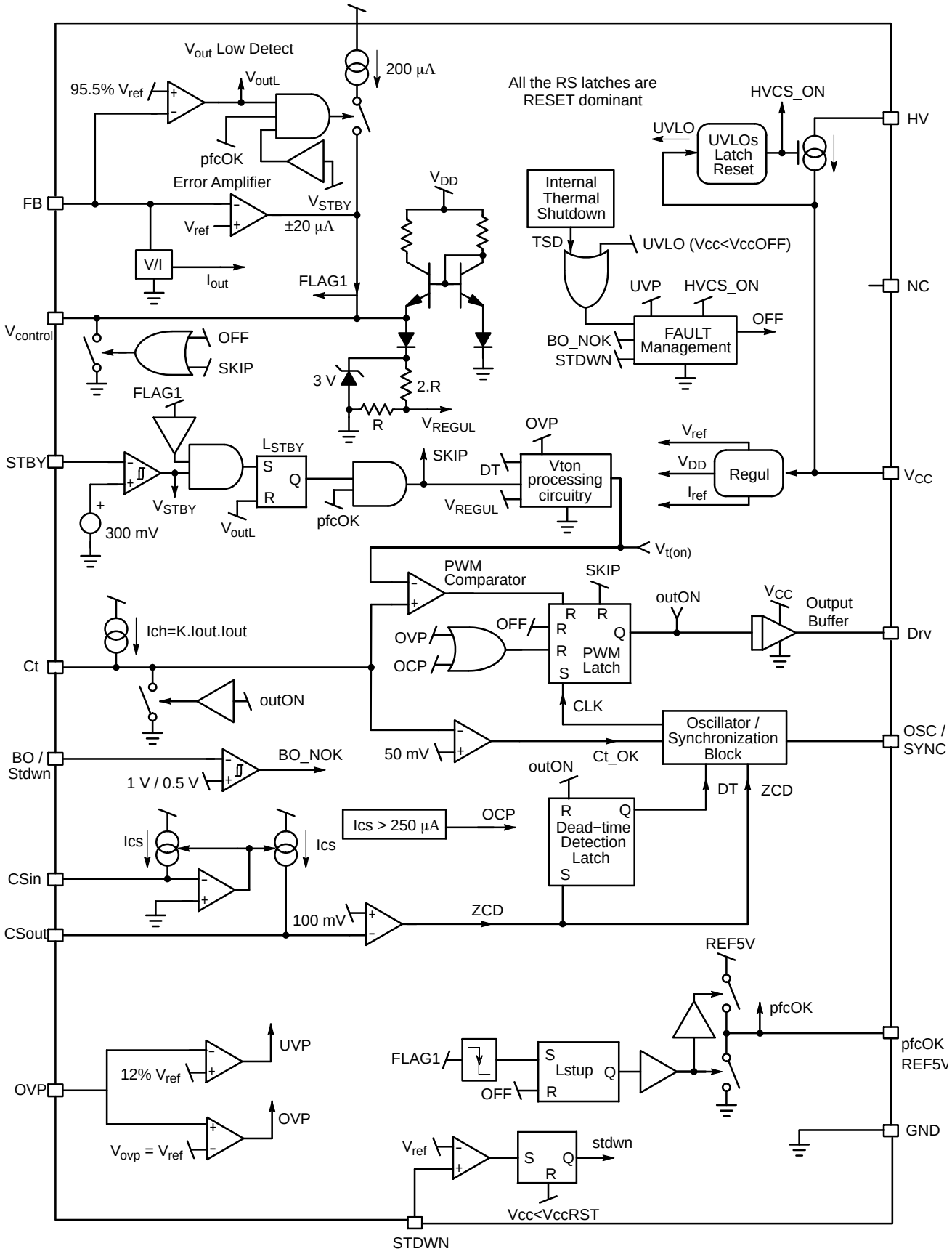


Figure 4−3. Block Diagram

The block diagram helps identify key functional improvements of the NCP1605 which are described below.

- The high voltage input (pin 16) which allows Vcc to be derived directly from the PFC bulk output by charging the Vcc capacitor through an internal current source. [Not used in this design]
- A separate OVP/UVP pin (pin 14) that allows independent protection feature desired in some applications.
- A latched shutdown input (pin 13) that can be used to protect against catastrophic faults. [Not used in this design]
- A PFCOK/reference output (pin 12) that can be used for sequencing the second stage to start after PFC is operational. [Not used in this design]
- An Oscillator/Sync input that helps set the maximum switching frequency. When the coil current has not reached zero, the switching period is automatically extended to enable CrM.
- The current sense resistor is put in the return path to sense the true inductor current. Hence the ZCD winding is not required.
- The light load operation is improved by including a cycle-skip function driven by input on pin 1. [Not used in this design]
- Window comparators to speed up the transient response when output voltage goes outside specified limits.
- Brown-out detection (pin 2) to turn-off the circuit when input voltage is too low.

Design Steps with 270 W Example

The step-by-step design procedure for FCCrM PFC using the NCP1605 is applied next to illustrate the design of a 270 W FCCrM PFC used as a basis for comparison (design P2 described in Chapter 2).

Step 1: Define the Key Specifications

Minimum Input voltage (Vac_{LL}): 88 Vac (this is usually 10−12% below the minimum typical voltage which could be 100 Vac in many countries).

Maximum Input voltage (Vac_{HL}): 264 Vac (this is usually 10% above the maximum typical voltage which could be 240 Vac in many countries)

Line frequency (f_{LINE}): 50 Hz/60 Hz (This is often specified in a range of 47−63 Hz and for calculations such as hold-up time, one has to factor in the lowest value specified)

Output Voltage (V_{out}): 385 V (This value has to be above 1.414 • Vac_{HL} and is typically between 385 and 400 V for universal input operation)

Maximum output voltage ($V_{out(max)}$): 415 V (This value is usually 7−10% above the V_{out} value and is determined by the accuracy of the OVP level of the PFC controller – conversely, the selection of the PFC controller has to be made based on this specification if it is determined by other component stress levels and derating factors).

PFC maximum output power (P_{out}): 270 W (This is the specified output power for the PFC stage. It is important to factor in the follow-on stage efficiency when specifying this parameter – it will always be higher than the specified maximum system output power)

Minimum switching frequency ($f_{sw(min)}$): 40 kHz (This parameter helps set the value of the boost inductor. Choosing it too low increases the inductor size and choosing it too high leads to very high frequency operation near zero crossing and at light loads)

Maximum switching frequency ($f_{sw(max)}$): 65 kHz (This parameter helps set the value of the oscillator capacitor and whenever CrM frequency tries to go above this value, the converter enters the DCM mode.

Output voltage ripple ($V_{ripple(p-p)}$): 20 V (This parameter is often specified in percentage of output voltage, ±5% is a very typical specification)

Hold-up time ($t_{hold-up}$): 16 ms (This parameter specifies the amount of time the output will remain valid during line drop-out. One line cycle is typically specified. For PFC alone, this spec is not applicable, but the PFC output capacitor is the single largest determinant of the hold-up time)

Estimated efficiency (η): 93% (This parameter is an initial estimate that is used to size the power stage components – high level of accuracy is not needed for the design procedure).

Step 2: Design the Boost Inductor (PFC Coil)

The (maximum) peak inductor current is the same as the CrM, since the converter operates in CrM for the most stressful condition (low line, full load). This current is given by:

$$I_{coil,pk(\max)} = \frac{2 \cdot \sqrt{2} \cdot P_{out}}{\eta \cdot Vac_{LL}} = \frac{2 \cdot \sqrt{2} \cdot 270}{0.93 \cdot 88} = 9.33A$$

The rms current is given by:

$$I_{coil,rms(\max)} = \frac{I_{coil,pk(\max)}}{\sqrt{6}} = \frac{9.33}{2.45} = 3.81A$$

The boost inductor design (which is also similar to the CrM design) is given by the equation below (generally low line presents the worst case situation, but the following equation should also be applied for the high line condition) :

$$L \geq \frac{\eta \cdot Vac_{LL}^{2} \cdot (\frac{V_{out}}{\sqrt{2}} - Vac_{LL})}{\sqrt{2} \cdot V_{out} \cdot P_{out} \cdot f_{sw(\min)}} = \frac{0.93 \cdot 88^{2} \cdot (\frac{385}{\sqrt{2}} - 88)}{\sqrt{2} \cdot 385 \cdot 270 \cdot 40000} = 225\,\mu\text{H}$$

In the design under consideration, a 250-μH inductor was chosen, resulting in a minimum frequency of 36 kHz. In order to facilitate direct comparison with CrM, an identical inductor was chosen and used for both CrM (Chapter 3) and FCCrM (Chapter 4).

In the absence of a need to make a direct comparison such as in this handbook, it would have been advisable to push the minimum frequency higher for a FCCrM application. The benefit of this would be smaller inductor requirement as indicated in the equation above. In a normal CrM operation, this would have created a very high maximum frequency, but because of frequency clamping, this situation is averted in the FCCrM operation. Other point to note is that with CrM and FCCrM, the turn-on switching losses are averted, so the switching loss penalty of increasing the switching frequency is not that severe. However, the inductor still has core losses which are function of switching frequency and these should be kept in mind while increasing the switching frequency.

Step 3: Select the Oscillator Capacitor

The oscillator capacitor sets the maximum frequency. In this case, the maximum frequency is chosen to be 65 kHz. Choosing a maximum frequency very close to the minimum frequency calculated in the above step lets the converter operate in CrM for only a brief operating range. All other times, the converter will operate in DCM. In this case, this choice was made intentionally for two reasons. First, it demonstrates the functionality of the FCCrM in the widest range of operating condition and second, it allows the FCCrM circuit to operate as close in frequency to the CCM solution to make the comparisons between the two modes more relevant.

The value of C_{osc} is derived using following equation:

$$Cosc = \frac{I_{charge}}{2 \cdot \Delta V \cdot f_{sw(\max)}} - 20 \cdot 10^{-12} = \frac{100 \cdot 10^{-6}}{2 \cdot 1 \cdot 65000} - 20 \cdot 10^{-12} = 750\,\text{pF}$$

Where I_{charge} and ΔV are the datasheet specified values for the C_{osc} charge current and the oscillator voltage swing respectively. Based on above calculations, 2 capacitors (270 pF and 470 pF) in parallel are used in the present design to have the required capacitance.

Step 4: Current Sense and ZCD Design

The current sense signal across the sense resistor is actually a negative voltage. However, insertion of a resistor between R_{sense} and pin 5 of the NCP1605 allows that signal to be converted into a current. The value of R_{sense} is chosen to minimize its impact on efficiency at low line, full load (here, 0.1 Ω is chosen). The equation for R_{ocp} is given by:

$$R_{ocp} = \frac{I_{coil,pk} \cdot R_{sense}}{I_{pin5(\max)}} = \frac{9.33 \cdot 0.1}{250 \cdot 10^{-6}} = 3.6\,\text{k}\Omega$$

The ZCD design in the NCP1605 is eased because the inductor current is sensed through pin 5. The current into pin 5 is reflected and sourced out of pin 6 through termination resistor R_{ZCD}. The value of R_{ZCD} should be about 3 times the value of R_{ocp}. A natural hysteresis is provided by the offset resistor that is tied to the DRV pin (R_{DRV}). This resistor should be about 3 times the value of R_{ZCD}. The final component values are:

R_{ZCD} = 12 kΩ, R_{DRV} = 33 kΩ

If a further optimized efficiency is preferred, a ZCD circuit that is similar as the one in NCP1607 application schematic would be useful. This circuit is to add the ZCD winding on PFC choke (N_{ZCD}), and insert one diode (e.g. 1N4148) and one resistor (R_{ZCD1}) between the ZCD winding and pin 6. During the switch off condition, a voltage of (V_{out}-V_{in}) is across the boost inductor. As the current reaches zero, this voltage starts collapsing and ZCD winding senses this event. The turns ratio of ZCD winding is selected such that the reflected (V_{out}-V_{in}) voltage is above the ZCD threshold under all conditions as shown in the equation:

$$\left[(V_{out}-\sqrt{2}\cdot Vac_{HL})\cdot\frac{N_{ZCD}}{N_B}-V_f\right]\cdot\frac{R_{ZCD}}{R_{ZCD}+R_{ZCD1}}>V_{ZCDH}$$

Assume R_{ZCD1} has 2 times higher resistance of R_{ZCD}.

$$\frac{N_B}{N_{ZCD}}<\frac{(V_{out}-\sqrt{2}\cdot Vac_{HL})}{V_{ZCDH}\cdot\frac{R_{ZCD}+R_{ZCD1}}{R_{ZCD}}+V_f}=\frac{(385-1.414\cdot 264)}{0.1\cdot 3+0.3}=19.5$$

The N_{ZCD} would be then above 56 turns / 19.5 = 2.87 turns. Choose 3 turns as N_{ZCD}.

The resistance of R_{ZCD1} and parasitic capacitance on the pin 6 create a short delay circuit which allows the drain voltage of the FET to fall after ZCD condition is reached. If the switch turn-on condition matches the valley of the drain voltage, the switching losses are minimized. The final component value of R_{ZCD1} is:

R_{ZCD1} = 24 kΩ

Step 5: Set FB, OVP and UVP Levels

The NCP1605 provides 2 separate pins for the feedback and OVP/UVP functions. Using a single feedback chain consisting of R_{OUT1}, R_{OUT2} and R_{OUT3}, these functions can be accomplished. The equations are given by:

$$V_{out}=\frac{R_{OUT1}+R_{OUT2}+R_{OUT3}}{R_{OUT2}+R_{OUT3}}\cdot V_{ref}\ \text{and}\ V_{out(\max)}=\frac{R_{OUT1}+R_{OUT2}+R_{OUT3}}{R_{OUT2}}\cdot V_{ref}$$

Since there are only two equations and three unknown quantities, we have the freedom to choose the impedances to achieve the right trade-off between noise susceptibility when very high impedances are chosen and high standby current when low impedances are chosen. In this case, R_{OUT2} is chosen as 24.3 kΩ and from there, the R_{OUT1} and R_{OUT3} are calculated to be 4.0 MΩ and 1.82 kΩ respectively.

Finally, the UVP level is given by:

$$V_{out(UV)}=0.12\cdot V_{out(\max)}=0.12\cdot 415=49.8\ \text{V}$$

This is the output voltage below which the NCP1605 will enter under-voltage protection and shut down output pulses. This feature also protects against an open feedback path.

Step 6: Select the On-time Capacitor (C_t) and Offset Circuit

The C_t capacitor on pin 7 can offer multiple functionalities in NCP1605. By dimensioning it correctly, the follower boost operation can be programmed to take effect at a given power level. However, in this particular case, the follower boost function is not desired, so the C_t capacitor is sized to provide full power at low line. The equation for required capacitance for no follower boost is:

$$C_t = \frac{120\mu \cdot V_{ref}^2 \cdot L \cdot P_{out}}{\eta \cdot Vac_{LL}^2} = \frac{120 \cdot 10^{-6} \cdot 2.5^2 \cdot 250 \cdot 10^{-6} \cdot 270}{0.93 \cdot 88^2} = 7.03\,\text{nF}$$

Where V_{ref} is the NCP1605 internal reference (2.5 V) and 120 μ represents the internal constant of NCP1605 when the C_t charge current is made proportional to the feedback voltage squared.

A known issue with any fixed on-time circuit is that the on-time at high line (especially at light loads) is extremely small − in the 200-500 ns range. Such small on-times are susceptible to propagation delay changes and circuit variations. Additionally, it presents a unique problem to the NCP1605, since there is an intervening circuit that is used to create the Vton that corresponds to the on-time. The accuracy of this circuit suffers when on-time is small. A trick is to add an intentional offset on the on-time to change its functional range. This offset is externally introduced by inserting a resistor Roffset between C_t pin and ground and tying a resistor Rdrv2 from the gate drive output to the junction of C_t and R4. To achieve accurate V_{out}, the resistive divider of Rdrv2 and Roffset should form an offset of 400-500 mV when the switch is on. On the other hand, since NCP1605 implements the skip mode feature, a lower offset could be trimmed depending on the required accuracy of V_{out}. In the present design, with choice of Rdrv2 = 4.7 kΩ and Roffset = 56 Ω, the offset is 0.18 V for 15 V Vcc.

Once the offset is applied to the C_t pin, its effective range becomes narrow. Without offset, it is full 1 V, but the offset reduces it by 0.18 V in this case. As a result, in order to achieve the same on-time, the C_t value has to be revised up by same ratio. Hence, the new C_t value is given by:

$$C_t(offset) = \frac{C_t(nom)}{1 - V_{offset}} = \frac{7.03}{1 - 0.18} = 8.57\,\text{nF}$$

For ensuring no follower boost operation, a higher value of C_t (10 nF) is used in this application.

Step 7: Power Stage components (MOSFET, Diode and sense resistor)

The power stage components are designed based on their current and voltage ratings. The inductor design is already covered in step 2. The MOSFET is selected based on peak voltage stress ($V_{out(max)}$+margin) and rms current stress:

$$I_{M(rms)} = \frac{2 \cdot P_{out}}{\sqrt{3} \cdot \eta \cdot Vac_{LL}} \cdot \sqrt{1 - \frac{8 \cdot \sqrt{2} \cdot Vac_{LL}}{3 \cdot \pi \cdot V_{out}}} = \frac{2 \cdot 270}{\sqrt{3} \cdot 0.93 \cdot 88} \sqrt{1 - \frac{8 \cdot \sqrt{2} \cdot 88}{3 \cdot \pi \cdot 385}} = 3.24\,\text{A}$$

Using a 600 V, 0.19 ohm FET, will give conduction losses of (assuming that $R_{ds(on)}$ increases by 80% due to temperature effects):

$$P_{cond} = I_{M(rms)}^2 \cdot R_{ds(on)} = 3.24^2 \cdot 0.19 \cdot 1.8 = 3.6\,\text{W}$$

While switching losses are harder to predict without getting into the details of switching waveforms and diode recovery characteristics, etc., it can be assumed that for a FCCrM PFC, the switching losses will be lower than the conduction losses. One component of the switching losses that can be predicted is the capacitive turn-on losses.

$$P_{sw,cap} = \frac{2}{3} \cdot Coss_{25} \cdot \sqrt{25} \cdot V_{on}^{1.5} \cdot f = 0.666 \cdot 780 \cdot 10^{-12} \cdot 5 \cdot (385)^{1.5} \cdot 36000 = 0.71\,\text{W}$$

Here, the nonlinear nature of the capacitance is taken into account. However, as mentioned in step 4, the ZCD network design can help in reducing the V_{on} from the nominal voltage of 385 V to a much lower value and reduce the losses even more. For the CrM, the conduction losses dominate, hence, lowest economically feasible $R_{ds(on)}$ MOSFET is chosen. In this design, the 20 A, 600 V FET with 0.19 ohm $R_{ds(on)}$ was chosen.

The boost diode is a simple selection for FCCrM since there are no reverse recovery issues to worry about. The goal is to choose the correct voltage rating ($V_{out(max)}$ + margin) and lowest forward drop available. The average diode current is the same as the output current ($I_d = P_{out}/V_{out} = 270/385 = 0.7$ A). So, the losses are just $I_d \bullet V_f$. The peak current seen by the diode will be the same as the inductor peak current. The diode chosen here is the MUR550 which offers lower forward drop by trading off on the reverse recovery characteristics.

Step 8: Output Capacitor Design

The output capacitor is designed considering 3 factors: output voltage ripple, output current ripple and the hold-up time. The output voltage ripple is given by:

$$V_{ripple(p-p)} = \frac{P_{out\cdot}}{2 \cdot \pi \cdot f_{line} \cdot C_{out} \cdot V_{out}}$$

The capacitor rms current is given by:

$$I_{Cout(rms)} = \sqrt{\frac{32 \cdot \sqrt{2} \cdot P_{out}^2}{9 \cdot \pi \cdot Vac_{LL} \cdot V_{out} \cdot \eta^2} - (\frac{P_{out}}{V_{out}})^2}$$

However, almost always, the size and the value of the capacitor is determined by the hold-up time which is given by:

$$t_{hold-up} = \frac{C_{out} \cdot (V_{out}^2 - V_{\min}^2)}{2 \cdot P_{out}}$$

In this case, a 220-μF capacitor was chosen that satisfies the conditions above. The peak-peak ripple is 10 V, the rms current is 1.87 A and the hold-up time is 18.6 ms (for a 320 V V_{min}).

These major design steps allow the functional prototype to be built and tested. In addition to these steps, other common steps such as Vcc generation, brown-out detection, feedback compensation and inrush limiting are also needed to complete the design. These steps are not covered here as they follow conventional methods.

Circuit Schematic and Bill of Materials

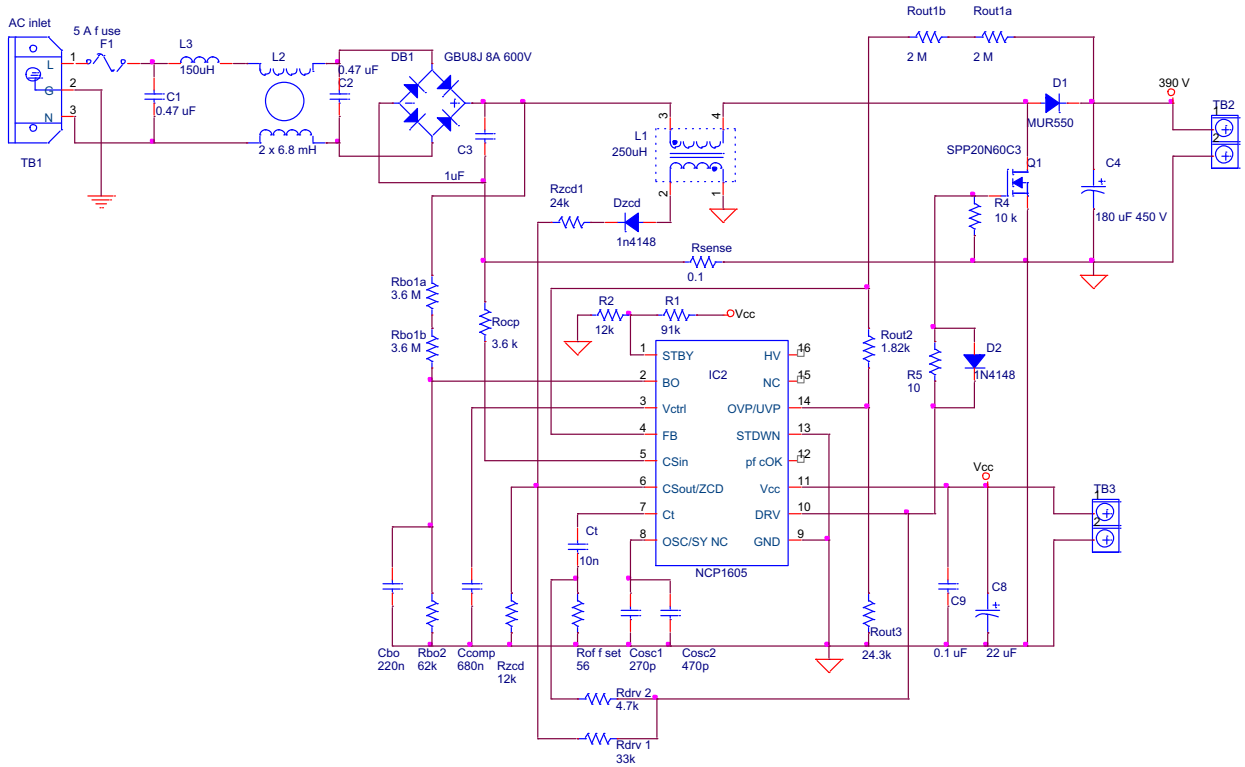


Figure 4−4. Circuit Schematic of NCP1605 Based PFC Converter

Table 4−1. Bill of Materials for the NCP1605 based PFC Converter

Quantity	Reference	Description	Part Number	Manufacturer
1	C1	0.47 μF / 275 V type X2	F1772-447-2000	VISHAY
1	C2	0.47 μF / 275 V type X2	F1772-447-2000	VISHAY
1	C3	1 μ, 400 V, High Ripple, Polypropylene Cap	ECWF4105JL	Matsushita
1	C4	180 μF 450 V	2222 159 47181	BC Components
1	Cbo	0.22 μF / 50V	K224K20X7RF53H5	VISHAY
1	Ccomp	0.68 μF / 50V	K684K20X7RF53H5	VISHAY
1	Cosc1	270 pF / 50 V	K271K15X7RF53H5	VISHAY
1	Cosc2	470 pF / 50 V	K471K15X7RF53H5	VISHAY
1	Ct	10 nF / 50 V	K103K15X7RF53H5	VISHAY
1	C9	0.1 μF / 50 V	K104K15X7RF53H5	VISHAY
1	C8	22 μF / 25 V	2222 013 36229	BC Components
1	DB1	600 V, 8.0 A bridge diode	GBU8J	VISHAY
1	D1	5.0 A, 520 V	MUR550PF	ON Semiconductor
2	D2	1N4148	1N4148	VISHAY
	Dzcd	1N4148	1N4148	VISHAY
1	F1	5 A fuse, Time Delay Fuse (FST 5x20)	0034.3124	SCHURTER
1	IC1	FCCrM PFC controller	NCP1605	ON Semiconductor
1	L1	250 μH (56 turns to 3 turns)		
1	L2	4 A, 2 x 6.8 mH, CM choke	B82725-J2402-N20	EPCOS
1	L3	150 μH, 5 A, WE-FI series, DM choke	7447055	Wurth Elektronik
1	Q1	20 A 600 V MOSFET	SPP20N60C3	Infineon
2	Rbo1a	Resistor, Axial Lead, 3.6 M, 1/4 W, 1%	CCF503M60FKE36	VISHAY
	Rbo1b	Resistor, Axial Lead, 3.6 M, 1/4 W, 1%	CCF503M60FKE36	VISHAY
1	Rbo2	Resistor, Axial Lead, 62 k, 1/4 W, 1%	CCF5062K0FKE36	VISHAY
1	Rdrv1	Resistor, Axial Lead, 33 k, 1/4 W, 1%	CCF5033K0FKE36	VISHAY
1	Rdrv2	Resistor, Axial Lead, 4.7 k, 1/4 W, 1%	CCF504K70FKE36	VISHAY
1	Rocp	Resistor, Axial Lead, 3.6 k, 1/4 W, 1%	CCF503K60FKE36	VISHAY
1	Rdrv2	Resistor, Axial Lead, 56, 1/4 W, 1%	CCF5056R0FKE36	VISHAY
2	Rout1a	Resistor, Axial Lead, 2 M, 1/4 W, 1%	CCF502M00FKE36	VISHAY
	Rout1b	Resistor, Axial Lead, 2 M, 1/4 W, 1%	CCF502M00FKE36	VISHAY
1	Rout2	Resistor, Axial Lead, 1.82 k, 1/4 W, 1%	CCF501K82FKE36	VISHAY
1	Rout3	Resistor, Axial Lead, 24.3 k, 1/4 W, 1%	CCF5024K3FKE36	VISHAY
1	Rsense	Resistor, Axial Lead, 0.1, 3 W, 1% LVR3 series	LVR03 R1000 F E12	VISHAY
2	Rzcd	Resistor, Axial Lead, 12 k, 1/4 W, 1%	CCF5012K0FKE36	VISHAY
	R2	Resistor, Axial Lead, 12 k, 1/4 W	CCF5012K0FKE36	VISHAY
1	Rzcd1	Resistor, Axial Lead, 24 k, 1/4 W, 1%	CCF5024K0FKE36	VISHAY
1	R1	Resistor, Axial Lead, 91 k, 1/4 W	CCF5091K0FKE36	VISHAY
1	R4	Resistor, Axial Lead, 10 k, 1/4 W	CCF5010K0FKE36	VISHAY
1	R5	Resistor, Axial Lead, 10, 1/4 W	CCF5010R0FKE36	VISHAY
1	TB1	AC inlet connector	GSF1.1201.31	SCHURTER
1	TB2	DC output plug socket	20.101/2 (order code 3044531)	IMO
1	TB3	Vcc connector plug socket	PM5.08/2/90. (order code 5015571)	WEIDMULLER
1	HS1	Heatsink (2.9 °C/W)	SK481 100mm	Fischer elektronik
2	Q1	Isolator TO220	3223-07FR-43	BERGQUIST
	D1	Isolator TO220	3223-07FR-43	BERGQUIST
3	DB1	Clip for heatsink (TO220)	THFU 1	Fischer elektronik
	Q1	Clip for heatsink (TO220)	THFU 1	Fischer elektronik
	D1	Clip for heatsink (TO220)	THFU 1	Fischer elektronik

Results and Performance Curves

The results of the NCP1605 based design described above are shown below.

Table 4−2. Performance Results of the 270 W NCP1605 PFC

Vin (Vac)	Pin (W)	Vo (V)	Io (A)	Output Power (W)	Pout	Efficiency	PF	THD
100	28.63	388.24	0.070	27.21 W	10%	95.05%	0.972	4.6
	42.52	388.19	0.105	40.77 W	15%	95.89%	0.987	4.3
	56.41	388.17	0.140	54.32 W	20%	96.29%	0.992	4.3
	140.88	387.96	0.350	135.84 W	50%	96.43%	0.998	2.9
	284.04	387.64	0.700	271.40 W	100%	95.55%	0.996	7.5
115	28.58	388.28	0.070	27.21 W	10%	95.21%	0.956	6.2
	42.40	388.23	0.105	40.77 W	15%	96.15%	0.977	3.9
	56.25	388.19	0.140	54.32 W	20%	96.56%	0.987	3.4
	140.29	388.04	0.350	135.87 W	50%	96.85%	0.997	2.7
	281.60	387.77	0.700	271.44 W	100%	96.39%	0.997	6.1
230	29.26	400.11	0.070	28.06 W	10%	95.90%	0.734	18.6
	42.35	389.76	0.105	41.05 W	15%	96.94%	0.825	13.6
	55.77	388.58	0.140	54.37 W	20%	97.49%	0.877	9.6
	138.25	388.19	0.350	135.91 W	50%	98.30%	0.969	6.7
	276.11	388.07	0.700	271.61 W	100%	98.37%	0.988	7.2

As shown in Table 4−2 the full load efficiency of the circuit at 100 Vac input is comfortably above 95%. The efficiency shows even better performance at light load (96.29% at 20% load). These are derived from the low switching losses and frequency clamping associated with FCCrM approach. The PF and THD at high line, full load are 0.988 and 7.2% respectively – which are quite good. At lighter load, the PF does go down, but not very significantly. Another interesting result to note is that the high line full load efficiency crosses 98%.

The harmonic analysis shown in Figure 4−5 shows that the converter passes class D limits easily. The data for the 75 W input condition were captured as shown in Figure 4−6 also show positive result.

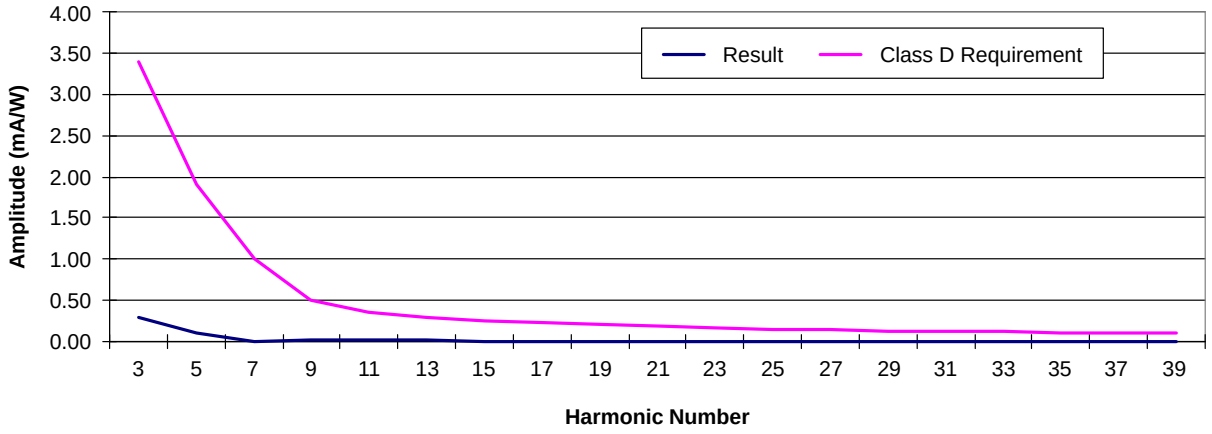


Figure 4−5. Harmonic Spectrum of 270 W FCCrM Converter at Full Load

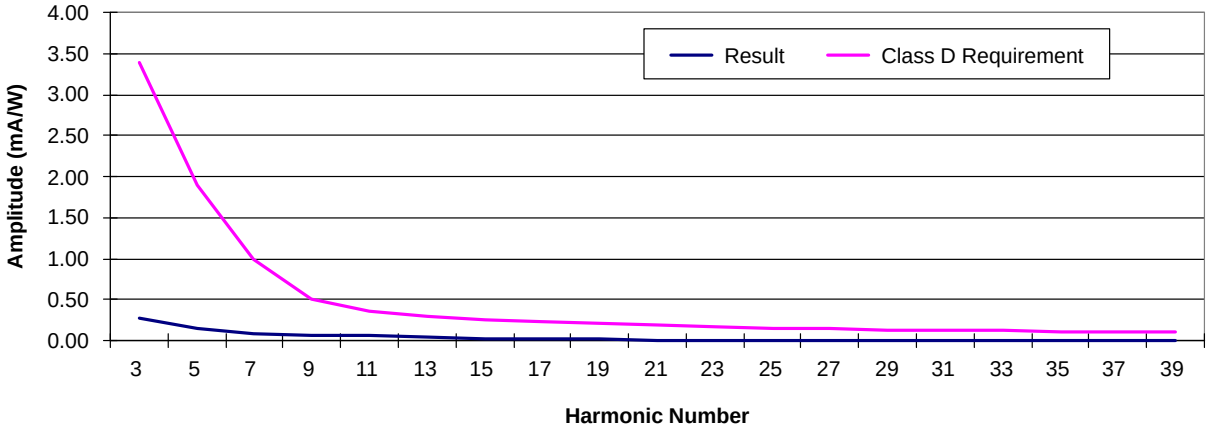


Figure 4−6. Harmonic Spectrum of 270 W FCCrM Converter at 75 W Load

Another key attribute to measure is the no load power drawn from the line at various input conditions. Table 4−3 shows these measurements. These measurements indicate that the no load input power is quite low for the FCCrM due to the frequency clamping and is also independent of the input voltage level.

Table 4−3. No Load Power Consumption

Vin	Pin (W)
100 Vac	0.125
115 Vac	0.118
230 Vac	0.131

The other areas of optimization for FCCrM investigated included the choice of optimal boost diode and also the optimization of the ZCD feature to get valley switching and minimize turn-on losses. It should be remembered that the relatively high rms current means that the trade-off of Rds on vs. switching loss is not an option and hence the 20 A MOSFET was not modified. By changing the boost diode from the 8 A, 600 V ultrafast diode (optimized for CCM) to 5 A, 520 V diode (MUR 550, optimized for CrM/FCCrM), the efficiency improvement at 100 Vac and full load was 0.22%. Next, by fine tuning the ZCD circuit to achieve precise valley switching, another efficiency improvement of 0.56% at 100 Vac and full load was achieved. The final results shown in Table 4−2 incorporate these enhancements. Figure 4−7 depicts the effects of the ZCD optimization effect. In the left figure, the switch turns on prior to Vds going to its valley and hard turn-on results in higher switching losses. By adding the ZCD delay (N_{ZCD} = 3 turns, R_{ZCD1} = 24 kΩ, and D_{ZCD} = 1N4148), the Vds can be brought to near zero as shown in the right waveform and the efficiency is improved. Here, Ch1 is the input voltage, Ch2 is the inductor current, Ch3 is the Vds waveform and Ch4 is the gate drive waveform.

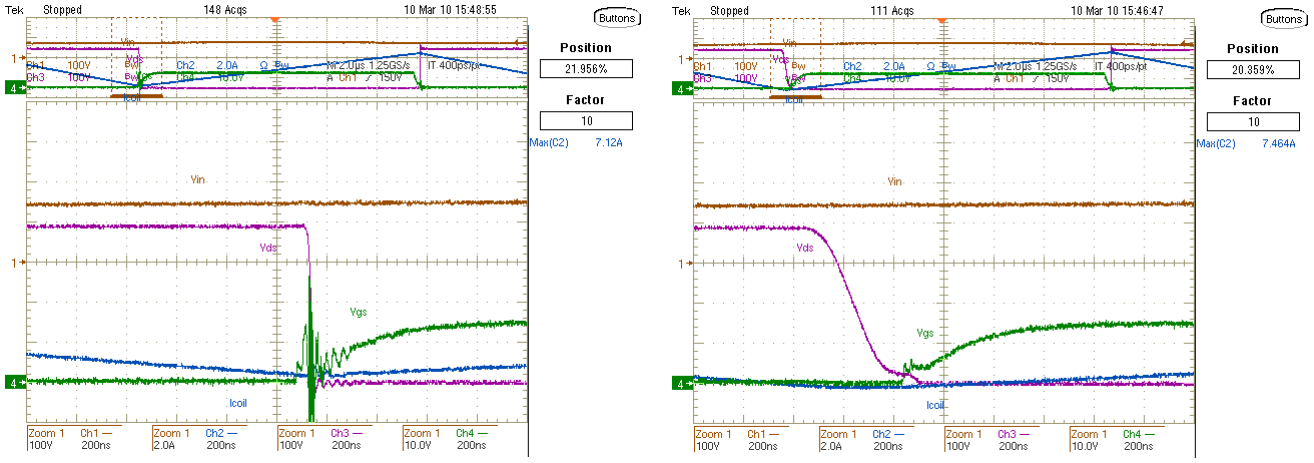


Figure 4−7. Turn-On Waveforms with (Left) No ZCD Delay and (Right) Optimized ZCD Delay

The Figure 4−8 shows the switching waveforms of the converter at full load and 115 Vac input. Here, Ch1 is the input voltage, Ch2 is the inductor current, Ch3 is the Vds waveform and Ch4 is the gate drive waveform. As seen here, the switching frequency is about 47 kHz.

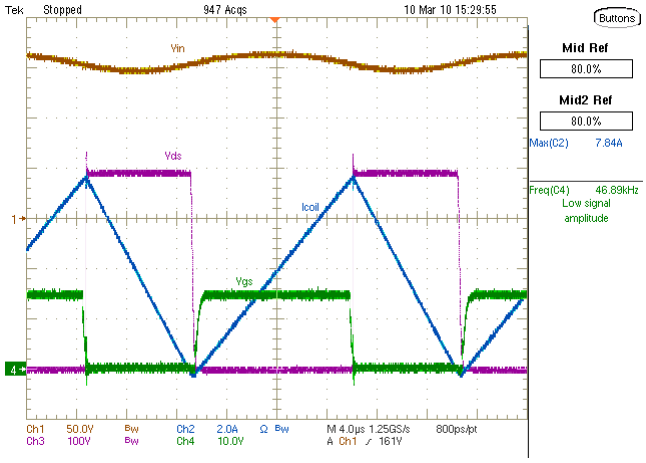


Figure 4−8. Switching Waveforms at Full Load, 115 Vac Input

Another critical contribution of the FCCrM circuit is the frequency clamping. As indicated in step 3, the maximum frequency chosen is 65 kHz. So, the frequency variation is limited compared to pure CrM operation shown in Chapter 3. As shown in Table 4−4, the frequency stays clamped at 62 kHz (close to the designed value). As a result, the light load operation is always in fixed frequency mode. Even at high line, full load and zero crossing, the frequency clamping comes into place. However, at other full load conditions, the converter operates in the CrM mode, keeping the peak currents in check. The frequency at peak and zero crossing appears to be the same for low line and full load conditions. This may be attributable to measurement error margins. Typically, the low line frequency variation between the peak and the zero crossing is not that much, so the measurement errors make them look the same.

Table 4−4. Frequency Variation in FCCrM Application

	Full load (0.7 A)		10 % load (0.07 A)	
	Peak Vin (kHz)	Zero Cross (kHz)	Peak Vin (kHz)	Zero Cross (kHz)
88 Vac	35.2	37.6	59.8	61.9
264 Vac	25.3	62.2	618	62.5

The results from Table 4−2 are plotted in graph form in figures below.

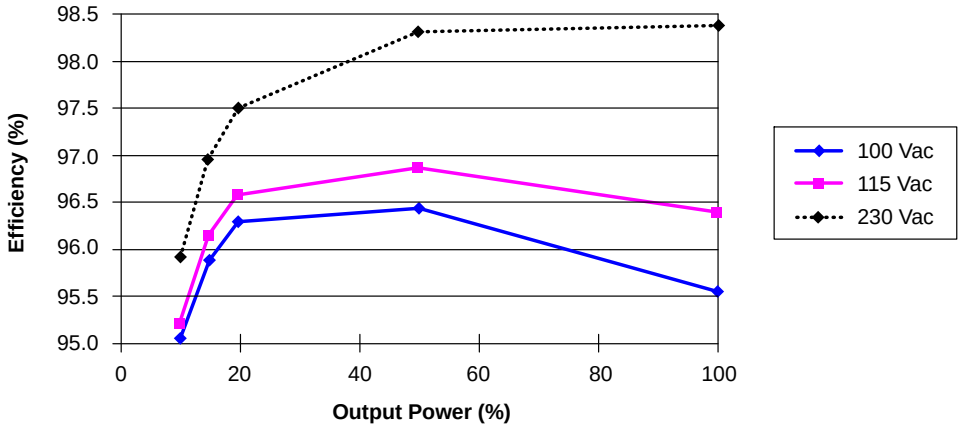


Figure 4−9. Efficiency Plot for FCCrM PFC

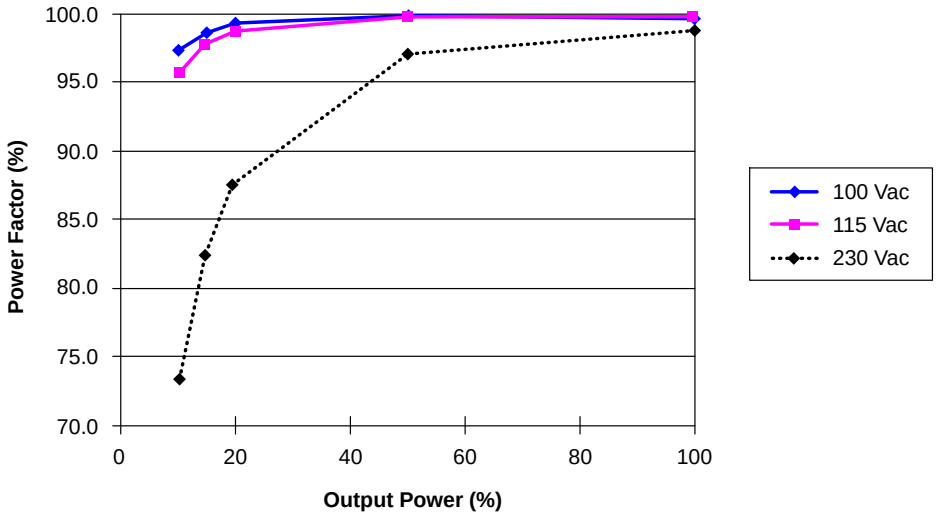


Figure 4−10. Power Factor Plot for FCCrM PFC

References

[1] “Implementing the NCP1605 to drive the PFC stage of a 19 V/8 A Power Supply”, AND8281/D, ON Semiconductor. http://www.onsemi.com/pub_link/Collateral/AND8281-D.PDF

CHAPTER 5

Current-Controlled and Valley-Switching Frequency Foldback Modes

Introduction

In general, power supplies do not permanently operate at the maximum power they are designed for but only for short periods of time. Hence, specifying the full-load performance is not sufficient for effective power savings. Instead, “green requirements” like the 80 PLUS® initiative [1] address the actual operating conditions by also dictating minimum levels for either the averaged efficiency or for the efficiency ratios at different loading situations: for example 10%, 20%, 50% and 100% of nominal power.

As a result, medium and light-load efficiency ratios have become critical points to address. Reducing the switching frequency is a popular option to improve efficiency under these conditions. Extremely efficient at very low power, this solution must be carefully implemented at intermediate power levels. The Current-Controlled and Valley-Switching Frequency Foldback techniques are emerging techniques that optimally control the operating frequency for maximized efficiency performance across a range of loads.

Why New Schemes?

It has been seen that Frequency Clamped Critical Conduction Mode (FCCrM) circuits improve the averaged efficiency by limiting the switching frequency that otherwise runs away at light load. Current-Controlled and Valley-Switching Frequency Foldback approaches do not only contain the switching frequency but further reduce it to values as low as 30 kHz when switching losses are dominant, for a further optimized efficiency.

As detailed in [2], a reduced frequency leads to less switching losses but increases conduction losses. More specifically,

$$(P_{cond})_{DCM} = (P_{cond})_{CrM} \cdot \sqrt{\alpha}$$

Where for a given operating point:

- $(P_{cond})_{DCM}$ are the conduction losses with the reduced frequency (DCM operation)
- $(P_{cond})_{CrM}$ are the conduction losses exhibited in CrM operation
- $\alpha = \frac{f_{SW.CrM}}{f_{SW.DCM}}$ is the ratio between the CrM frequency by the (reduced) DCM frequency

Hence, reducing the switching the frequency can be counterproductive if done when the rms current flowing within the PFC stage is too high. Also, frequency reduction must be well controlled. If not, an excessive reduction would degrade efficiency. Practically, it is interesting to reduce switching frequency when, in CrM, switching and conduction losses are substantially equal, with an optimal benefit when α nearly equals the following α_{max} term:

$$\alpha_{max} = \frac{(P_{SW})_{CrM}}{(P_{cond})_{CrM}}$$

Where $(P_{SW})_{CrM}$ designates CrM switching losses.

Regarding the frequency reduction impact, losses analysis and experimental data further show [2] that:

- When conduction losses are higher or in the same range as the switching losses, frequency foldback increases losses. This is what happens when large rms currents circulate through the converter like in heavy load, low line conditions of a PFC stage.
- When conduction losses are slightly smaller compared to switching losses, a limited reduction of the frequency is desired. It must remain limited however. Otherwise the benefits on the switching losses is totally cancelled or cannot compensate for the increase of conduction losses. This case corresponds to line and load conditions leading to a medium current within the converter...

- When conduction losses are very low compared to switching losses, frequency reduction dramatically lowers overall losses. The switching frequency must then be reduced when the line current is small.

In other words, frequency foldback is preferred when conduction losses are small compared to switching losses, that is, when the line current is low. More specifically, the lower the current is, the lower the optimal frequency.

The line current is hence an information of choice to detect when and how much the switching frequency is to be reduced. Based on this, Current-Controlled Frequency Foldback (CCFF) targets this optimal frequency control by forcing the DCM operation and by adjusting the dead-time as a function of either the instantaneous line current or an averaged form of it. Valley-Switching Frequency Foldback (VSFF) is a simplified version where the only line current magnitude is considered for frequency control.

It is worth noting that both CCFF and VSFF offer valley switching in all operating modes.

Next chapters will detail how these two options operate.

Current-Controlled Frequency Foldback (CCFF)

Targeting light-load efficiency requirements, ON Semiconductor has released the NCP1611 and NCP1612 PFC boost controllers which operate in a so-called ***C***urrent ***C***ontrolled ***F***requency ***F***old-back (***CCFF***) mode. In this mode, the PFC stage operates in traditional ***Cr***itical conduction ***M***ode (***CrM***) when the line current exceeds a programmable value. Conversely, when the current is below this preset level, the switching frequency decays down towards about 20 kHz as the line current reduces to zero [3] - [4].

Practically, these controllers monitor the line voltage and an internal computation generates a current. This current is pined out to a FFcontrol pin which, together with an external resistor, builds a signal representative of the line current. When this voltage ($V_{FFcontrol}$) exceeds the internal 2.5-V internal reference (V_{REF}), the circuit operates in critical conduction mode. The external resistor hence controls the minimal line current for CrM operation. Conversely, if the FFcontrol pin voltage ($V_{FFcontrol}$) is below 2.5 V, a dead-time is generated that approximately equals ($66\ \mu s \cdot (1 - (V_{FFcontrol} / V_{REF}))$). By this means, the circuit forces a longer dead-time when the line current is small and a shorter one as the line current is larger. In addition, the circuit skips cycles whenever the FFcontrol pin is below 0.65 V to prevent the PFC stage from operating near the line zero crossing where the power transfer is particularly inefficient.

The CCFF operation is summarized by Figure 5−1.

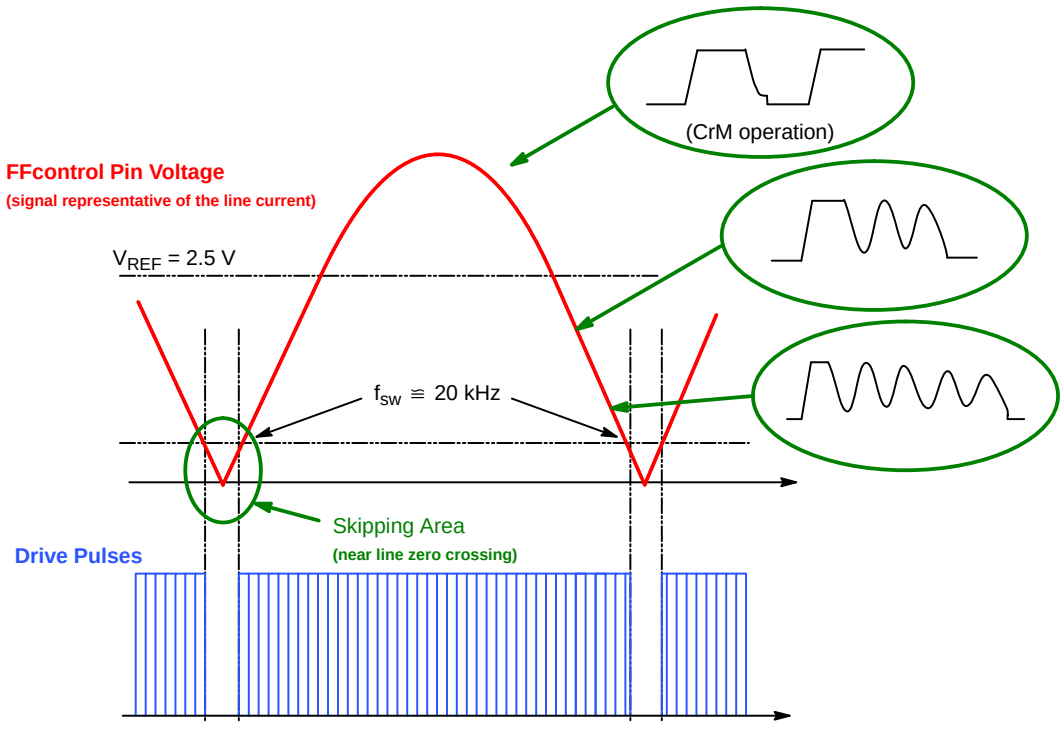


Figure 5−1. Current-Controlled Frequency Fold-back

Clamping the switching frequency of a CrM PFC boost normally leads to a distorted line current since traditional current shaping schemes assume a critical conduction mode operation. This traditional limitation is solved in the NCP1611 and the NCP1612 in the same way as in Frequency Clamped Critical conduction Mode (FCCrM) circuits from ON Semiconductor (NCP1605 for instance): a circuitry (designated V_{TON} processing block) is integrated and modulates the on time to compensate for the presence of dead-times. This block is based on an integrator (see data sheet for more details) whose time constant is nearly 100 μs for a proper switching ripple filtering.

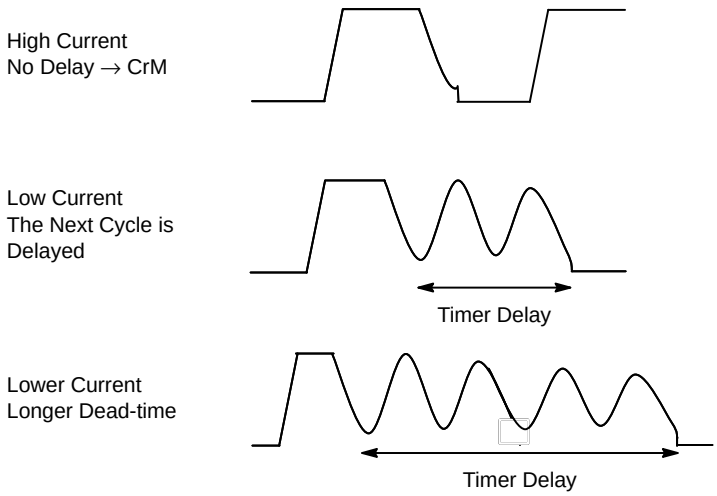


Figure 5−2. CCFF Operation

As illustrated in Figure 5−2 and Figure 5−3, under heavy line current conditions, a CCFF boost stage is intended to operate in CrM. When the line current reduces, the controller enters discontinuous conduction mode operation. By the way, even in DCM, the MOSFET turn-on is stretched until its drain-source voltage is at its valley for an optimal power saving.

The CCFF technique further leads to a stable operation without hesitation between valleys.

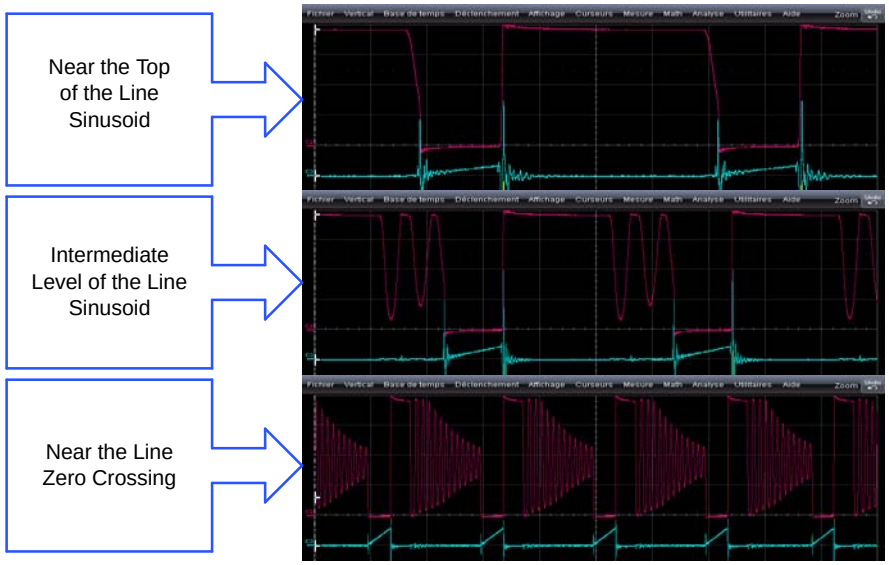


Figure 5−3. Operation @ 230 V, 160 W Near the Line Zero Crossing of the NCP1612 Evaluation Board. The MOSFET Drain-source Voltage is in Red, the Blue Trace Showing the MOSFET Current.

CCFF Flattens the Efficiency Over Load Characteristics

Tests have been carried on the NCP1611 evaluation board [5]. This is the slim (< 13 mm) PFC stage designed to provide 160 W from a wide mains line shown in Figure 5−4.

Figure 5−4. Wide Mains, 160 W PFC Stage

This board is designed to run in CCFF. However, it can be easily operated in CrM by forcing the line current representative signal above 2.5 V. It has the effect to disable the CCFF frequency foldback characteristic. Also, the skip-cycle capability inherent to CCFF operation can be disabled by preventing the line current representative signal from dropping below 0.65 V. Finally, this versability allows for testing three modes: CrM, CCFF and non-skipping CCFF, allowing perfect apples-to-apples comparison performed on the same application schematic with similar external power components.

A fair comparison also requires avoiding configurations which exagerate the affects in one mode when a better tailored solution is possible. This board is designed to be either self-powered or powered by an external voltage source. For efficiency measurements, the second option is preferred because the consumption of the charge pump implemented to feed V_{CC} in the self-powered option is proportional to the switching frequency. Keeping it would dramatically affect the light-load CrM efficiency. For instance, it was measured at high line, 20% of the load, that this charge pump would contribute a 1% efficiency loss in CrM while it did not significantly affect CCFF performance.

A large current charges the bulk capacitor when the PFC stage is plugged in. The board keeps the in-rush current under control with the help of a NTC. This NTC has been shorted for efficiency measurements.

Figure 5−5 reports efficiency ratios measured at low and high line over a large power range (from 5% to 100% of full load). The right-hand side of the CCFF efficiency curves resembles that of a traditional CrM PFC stage. In the left-hand side, the efficiency normally drops because of switching losses until an inflection point where it rises up again as a result of the CCFF operation. As previously detailed, CCFF makes the switching frequency decay linearly as a function of the instantaneous line current when it goes below a preset level. The CCFF threshold was set to about 20% of the line maximum current at low line, to nearly 45% at high line as confirmed by the aforementioned inflection points observed in Figure 5−5.

Recall that CCFF works as a function of the instantaneous line current: when the signal representative of the line current (generated by the FFcontrol pin) is lower than 2.5 V, the circuit reduces the switching frequency. This is the case near the line zero crossing whatever the load is. Hence, switching frequency reduces at the lowest values of the line sinusoid even in heavy load conditions. That is why efficiency is also improved when the load is high, at least at high line where CCFF has a higher impact since the line current is less.

When the instantaneous line current tends to be very low (below about 5% of its maximum level in our application – refer to [3]), the circuit enters a skip-cycle mode. In another words, the circuit stops operating at a moment when the power transfer is particularly inefficient. Compared to the skip-free CCFF operation, skip-cycle mode further improves the efficiency in light load (2% increase at high line and 5% of the full load).

More generally, Figure 5−5 illustrates that CCFF significantly improves efficiency below 20% of the load at low line while more dramatic benefits start to occur below 50% of the load at 230 V.

It should be noted that the total harmonic distortion is affected by the skip-cycle mode function. Even if it remains relatively low, skip mode should be inhibited when superior THD performance are targeted. Refer to the NCP1611/2 evaluation board for PF and THD data.

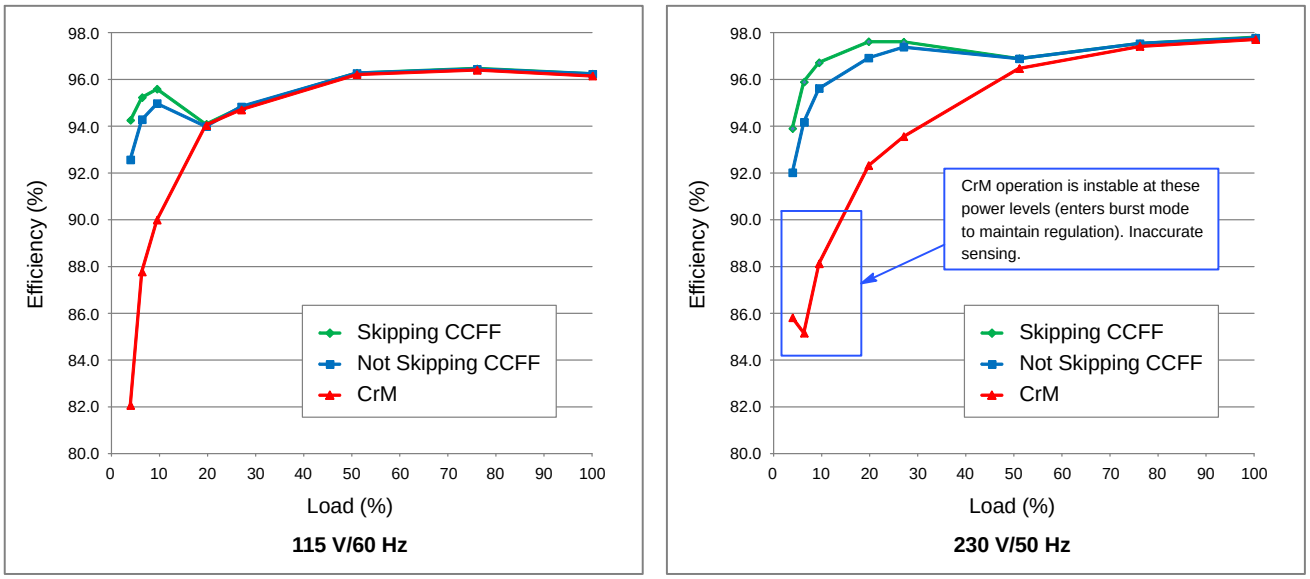


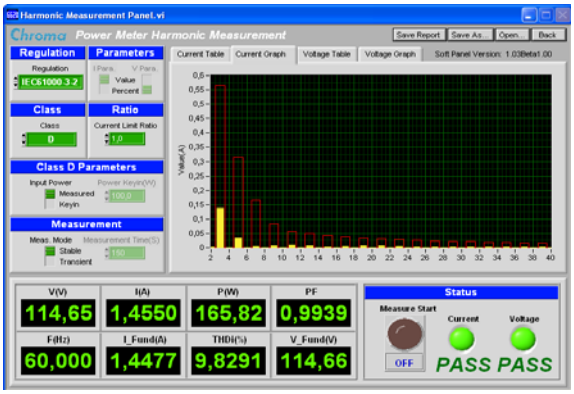
Figure 5−5. Efficiency Over the Load Range at Low- and High-line Conditions

Finally, these data confirm that CCFF maintains high efficiency ratios over an extended power range, in both low and high-line conditions. More specifically, for loadings ranging from 5% to 100%, efficiency remains above 94% if skip-cycle mode is enabled while the efficiency floor (obtained at 5% of the load) drops to 92% when skip-cycle mode is disabled.

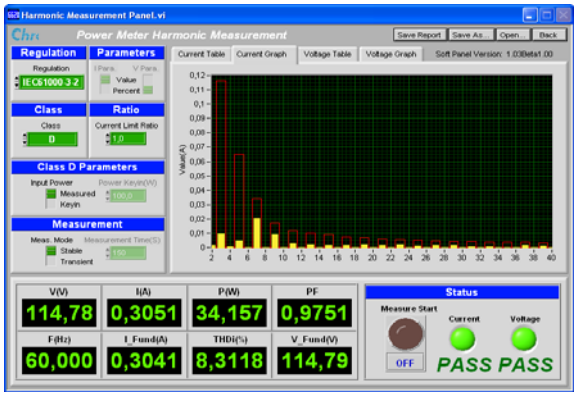
It is well known that CrM systems generally fail to operate continuously at high line, light load because of the high operating switching frequency. Instead, they enter burst mode. This often occurs in the range and below 20% of the load when operating at the highest line levels. Figure 5−5 illustrates that reducing switching frequency solves this limitation. Thus, it should be noted that CCFF further offers the possibility to have a stable operation down to extremely low power levels.

CCFF PF and THD Performance

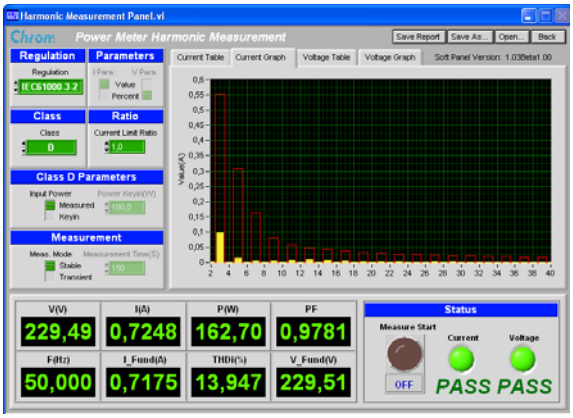
As mentioned before, CCFF NCP1611 and NCP1612 controllers modulate the on-time to compensate for the presence of dead-times. Such a circuitry is already embedded in Frequency Clamped Critical conduction Mode (FCCrM) controllers from ON Semiconductor (NCP1605 for instance). It provides a proper current shaping over the whole load range, whether the circuit operates in CrM or DCM. High performance can be obtained even in light load as illustrated by Figure 5−6 which reports the performance of the wide-mains, 160 W NCP1612 evaluation board ([6]) at 100% and 20% load for low- and high-line.



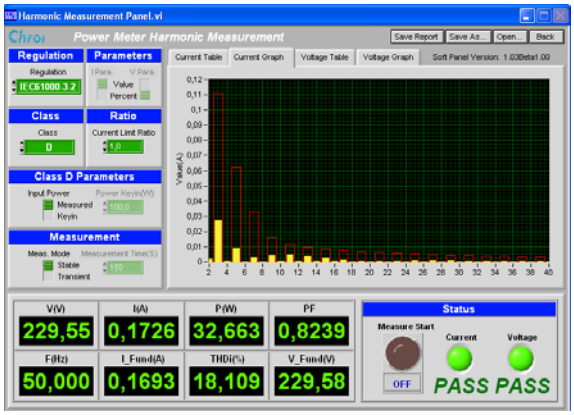
115 V/60 Hz, Full Load



115 V/60 Hz, 20% Load



230 V/50 Hz, Full Load



230 V/50 Hz, 20% Load

Figure 5−6. NCP1612 Evaluation Board − Performance with Respect to IEC61000−3−2 Class D Specification

Valley-Switching Frequency Foldback (VSFF)

VSFF is a CCFF simplified version where switching frequency characteristic is controlled by the line current magnitude rather than by its instantaneous value or an averaged form of it. No signal representative of the rectified line current is generated. Instead, the line is sensed and the monitored signal is fed-forward to make the control signal proportional to the line current magnitude.

More specifically, the line current of a traditional PFC boost converter is dependent on the line voltage:

$$i_{line}(t) = k_0 \cdot V_{control} \cdot v_{line}(t)$$

Where:

- $i_{line}(t)$ is the instantaneous line current
- $v_{line}(t)$ is the instantaneous line voltage
- k_0 is a constant accounting for the circuitry managing the duty-ratio control (for instance, the inductor value, the timing ramp and PWM constants for a voltage mode controller)
- $V_{control}$ is the control signal provided by the error amplifier.

Integrating over the line period, it comes:

$$I_{line,rms} = k_0 \cdot V_{control} \cdot V_{line,rms} \qquad (*)$$

Feedforward can consist in making the k_0 factor inversely proportional to the squared line rms voltage:

$$k_0 = \frac{k_1}{\left(V_{line,rms}\right)^2}$$

Doing so, the power expression becomes independent of the line magnitude for an eased loop compensation, the open loop being constant over the line range:

$$P_{in,avg} = k_1 \cdot V_{control}$$

A “first-order” feedforward can also be performed where k_0 factor is simply made inversely proportional to the line rms voltage:

$$k_0 = \frac{k_2}{V_{line,rms}} \qquad (**)$$

This feedforward approach limits the open-loop variations over the line range. In addition, substitution of equation (*) into equation (**) leads to:

$$V_{control} = \frac{I_{line,rms}}{k_2}$$

The control signal is then representative of the line current magnitude. This signal is hence used to control the dead-time. Finally, the major difference between CCFF and VSFF is the signal used to control the frequency. For the rest, the operation is same.

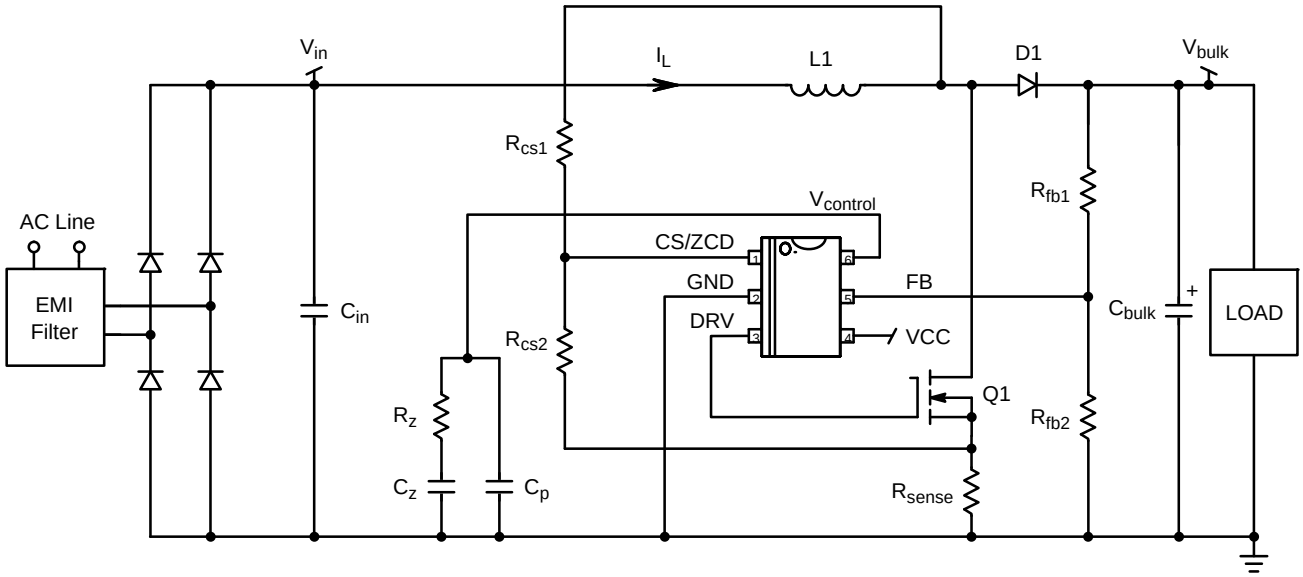


Figure 5−7. Generic Application Schematic for the NCP1602 6-pin Controller that Embeds the VSFF Technique

The NCP1602 from ON Semiconductor incorporates this architecture. Extremely compact, this 6-pin circuit does not exactly perform the “first-order” feedforward here above described. It simply detects two line ranges (low-line and high-line) and changes k_0 of equation (*) accordingly. This 2-step feedforward automatically sets an optimal gain at low-line and another at high-line for both compensation and VSFF operation ([7]). As a result, there is a $V_{control}$ threshold and at low-line and another one at high-line.

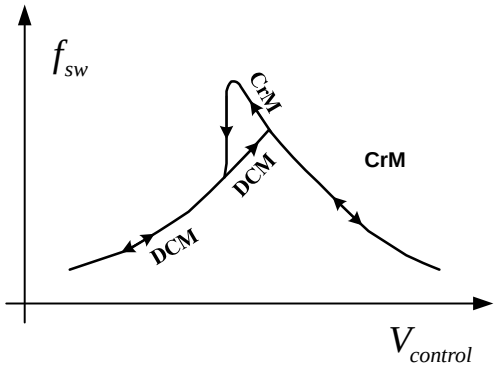


Figure 5−8. The System Enters and Leaves DCM in Accordance with the $V_{control}$ Level

When the line current drops below the $V_{control}$ threshold, the switching frequency starts to decrease as illustrated by Figure 5−8. This characteristic is in-built in such a way that the frequency does not exceed 150 kHz at the nominal low- and high-line voltage levels to help pass EMI specification (frequencies below 150 kHz are generally not considered by the most common standards).

As sketched by Figure 5−8, an hysteresis prevents the system from “hesitating” between DCM and CrM when the line current is near the DCM/CrM threshold. The frequency characteristic is further designed so that the system operates at frequency just above the audible range when in very light load.

Details of operation can be found in [7].

Design Procedure with a 160 W Example

Figure 5−9 presents the generic application schematic of a CCFF PFC stage. The step-by-step design procedure of a CCFF PFC stage is for instance detailed in [8] and will not be described here. Actually, power components selection is very much the same as for a Frequency Clamped CrM solutions, since the switching frequency spread is under control. In addition, the CCFF must be programmed by selecting the current level below which the frequency is reduced. Equations and an Excel spreadsheet exist and let the designer make this setting relatively easily.

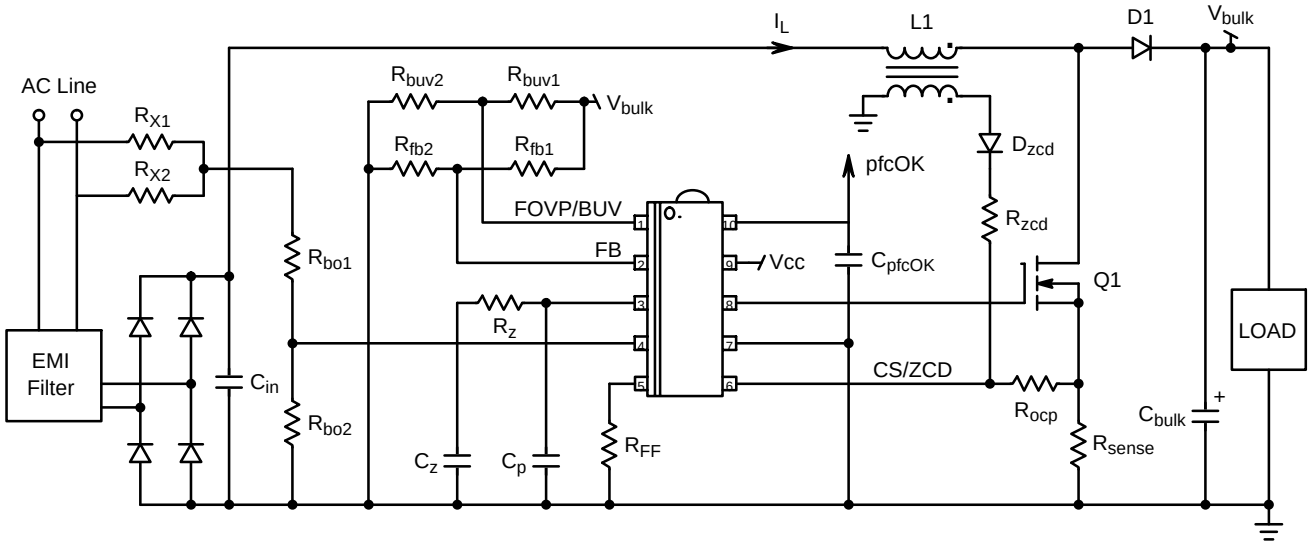


Figure 5−9. Generic Application Schematic

Same statement is valid for VSFF designs. Even, with the NCP1602 as the controller, the dimensioning is particularly straightforward. Most of the functions are inbuilt to optimally cope with a large variety of applications, including the current level below which the frequency starts to reduce. Design work is hence reduced to a minimum.

Conclusion

Frequency foldback is necessary to optimize the efficiency and the THD performance of a PFC stage over the load range. However, the operating point below which frequency reduction occurs and the frequency span must be carefully selected to maintain efficiency in spite of increased conduction losses. Based on this, both CCFF and VSFF architectures were designed to optimally manage the frequency foldback operation. CCFF mode is more flexible by offering a precise setting of the frequency foldback characteristic. More compact, VSFF automatically offers a frequency control to efficiently drive most applications.

CCFF and VCFF solutions are recommended for applications ranging from 0 to 500 W.

Following Figure 5−10 and Figure 5−11 give an overview of the CCFF and VSFF frequency characteristic with respect to that obtained with the traditional critical conduction mode. Practically, these plots illustrate the frequency variation over one half-line cycle at 115 V rms, for three load levels (20%, 50% and 100% of the full power) of a 160 W PFC stage.

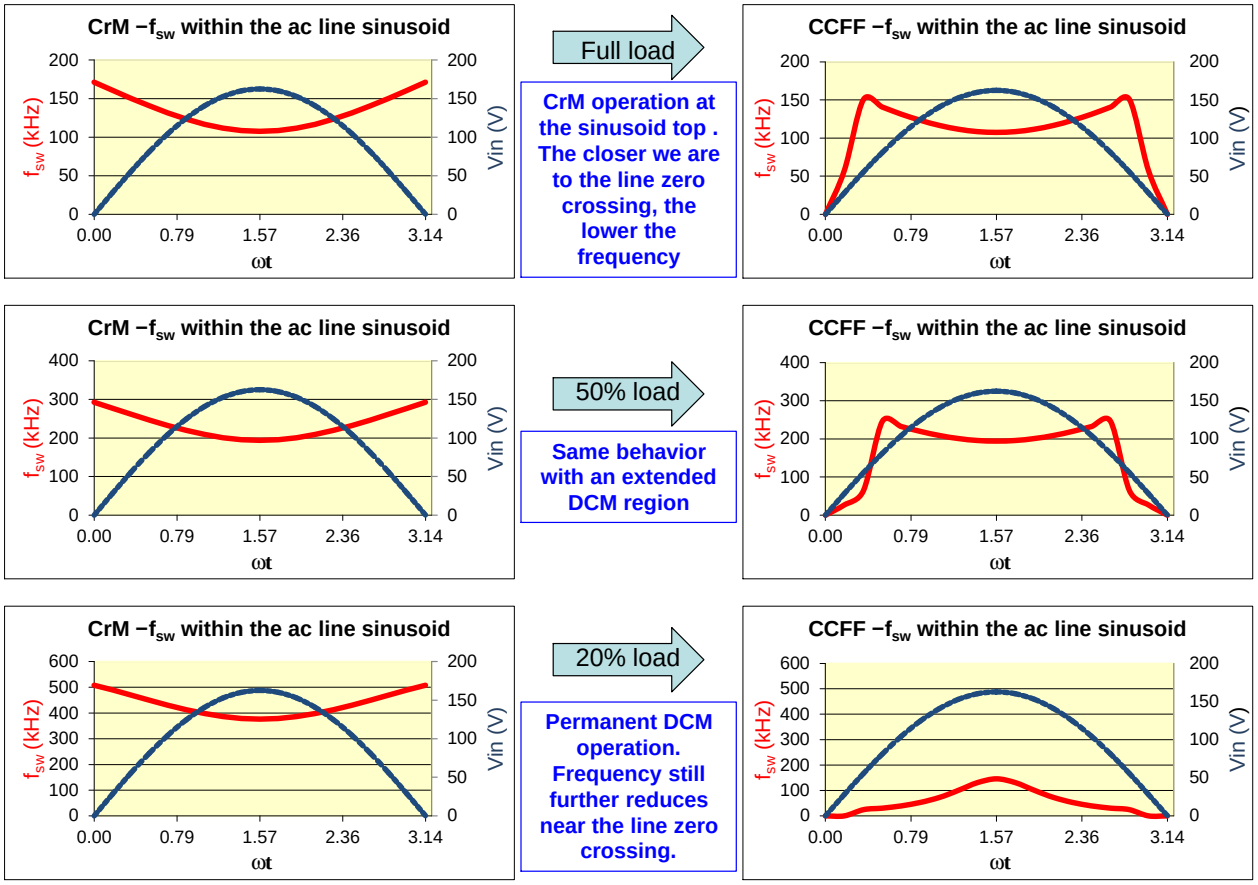


Figure 5−10. CCFF with Respect to CrM at Three Different Load Levels

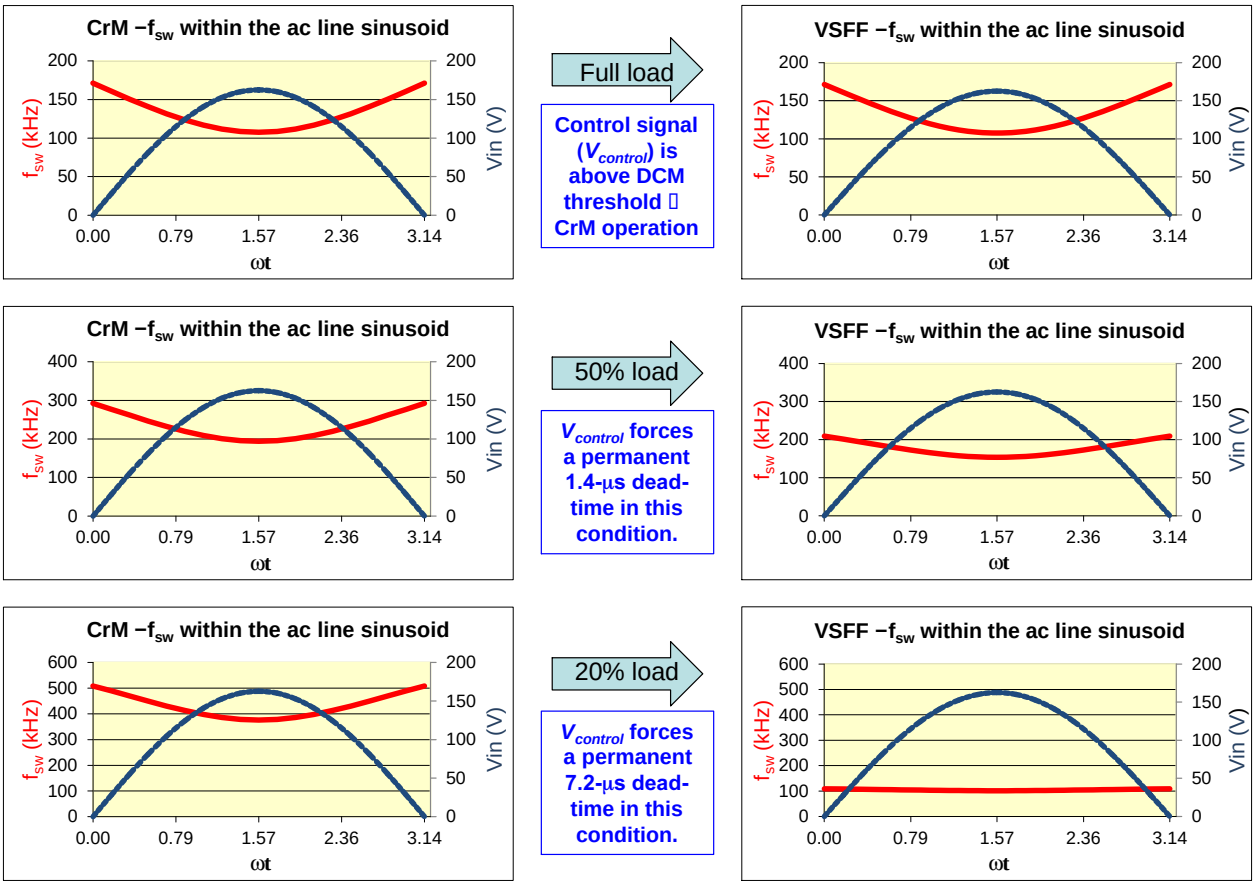


Figure 5−11. VSFF with Respect to CrM at Three Different Load Levels

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[2] Joel Turchi: “Frequency-Foldback Technique Optimizes PFC Efficiency Over The Full Load Range”, How2Power Today Magazine, October 2012 issue, http://www.how2power.com/newsletters/1210/articles/H2PToday1210_design_ONSemiconductor.pdf
[3] NCP1611 data sheet and application notes, http://www.onsemi.com/PowerSolutions/product.do?id=NCP1611
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[7] NCP1602 data sheet and application notes, http://www.onsemi.com/PowerSolutions/product.do?id=NCP1602
[8] Joel Turchi, Application notes “5 key steps to design a compact, high efficiency PFC stage using the NCP1612”, http://www.onsemi.com/pub_link/Collateral/AND9065-D.PDF

CHAPTER 6

Continuous Conduction Mode (CCM) PFC

The continuous conduction mode (CCM) PFC has been around for many years and as indicated in [1], average current mode control is the most convenient way of achieving CCM PFC. The traditional average current mode controllers and their improvements have been described before [2]. More recently, predictive CCM PFC controllers have been introduced as described in Chapter 1. This section walks the reader through the design of a continuous conduction mode boost PFC circuit utilizing the NCP1654 predictive PFC controller, which has 65 kHz, 133 kHz, and 200 kHz operating frequency versions. The description here is restricted to major design choices and their analyses. More in-detail designs are provided in the products' datasheets and application notes.

CCM Introduction

The CCM operation is more popular at higher power levels as it has minimal peak and rms currents. In comparison with the CrM operation, the peak currents can be 50% lower and rms currents can be 25% lower. This reduces the stress in power FET, diode and inductor. In addition, the filtering is easier as the current through the boost inductor is more continuous. Finally, the switching frequency remains constant for the CCM operation, so the boost inductor design and EMI filter design are easier.

However, traditional control algorithms and circuitry for CCM PFC have always been more complex and 16-pin controllers with significant number of external components were common in the CCM applications for a long time. In recent years, the predictive control method has resulted in a simplified approach being available and NCP1653 and NCP1654 are examples of such simple methodology for CCM PFC.

NCP1654 – Simplified CCM PFC Controller

Housed in a DIP8 or SO8 package, the NCP1654 minimizes the number of external components and drastically simplifies the PFC implementation. It also integrates high safety protection features that make the NCP1654 a driver for robust and compact PFC stages (e.g. input power runaway clamping circuitry). Following features make the NCP1654 a unique solution:

- Flexibility to operate in traditional or follower boost mode
- Low power consumption and shutdown capability
- Key safety and protection features including:
- Maximum current limit – directly applicable to the inductor current
- Feedback network failure protection (Under voltage protection/shutdown)
- Brown-out detection and shutdown to prevent thermal overheating
- Output overvoltage protection
- Overpower protection and shutdown
- Thermal shutdown
- Improved output voltage regulation accuracy (compared to NCP1653)

The block diagram of NCP1654 is shown in Figure 6−1.

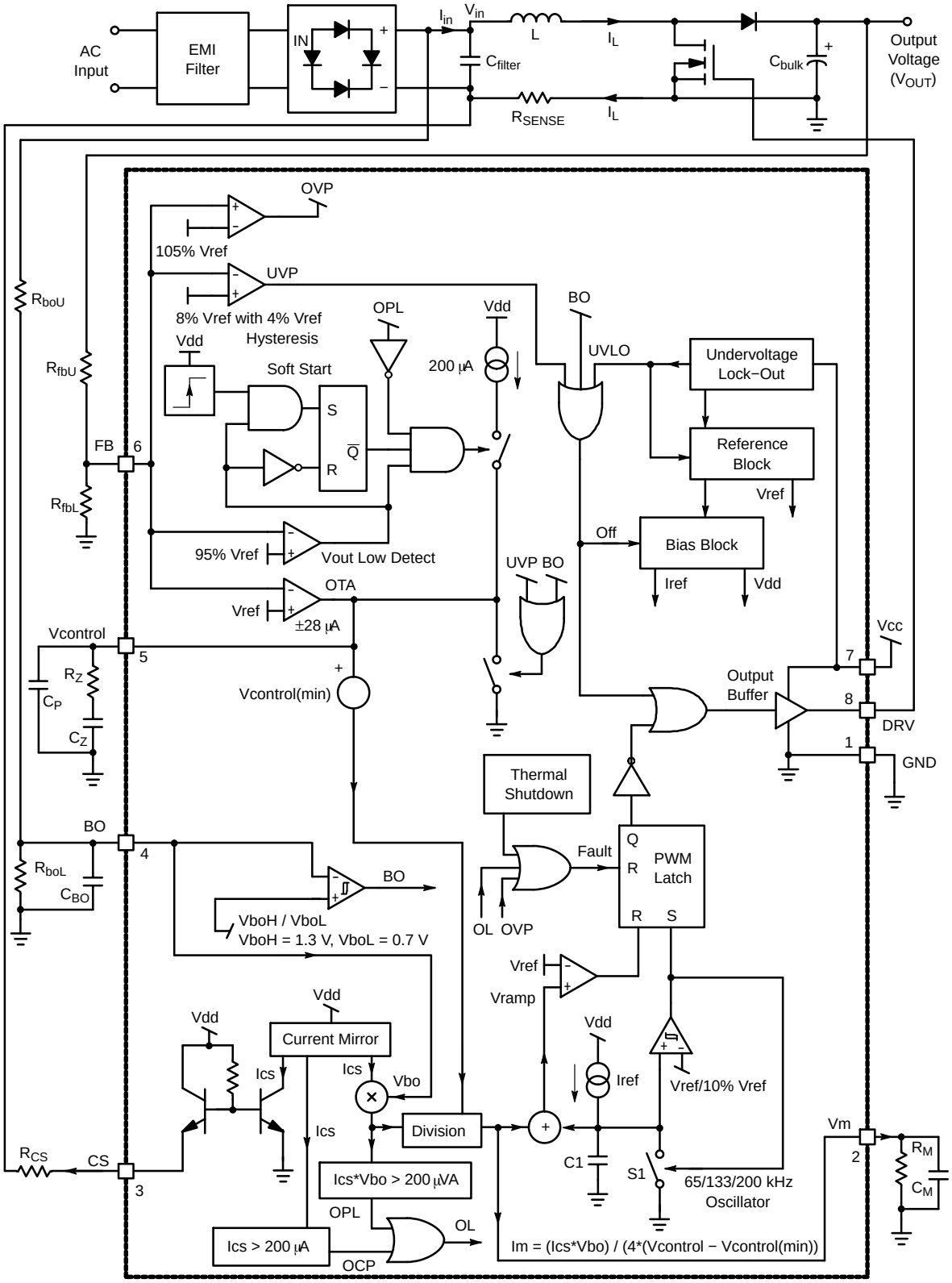

Figure 6−1. NCP1654 Block Diagram

Design Steps with 270 W Example

The step-by-step design procedure for CCM PFC using the NCP1654 is applied next to illustrate the design of a 270 W CCM PFC used as a basis for comparison (design P3 described in Chapter 2).

Step 1: Define the Key Specifications

Minimum Input voltage (Vac_{LL}): 88 Vac (this is usually 10−12% below the minimum typical voltage which could be 100 Vac in many countries).

Maximum Input voltage (Vac_{HL}): 264 Vac (this is usually 10% above the maximum typical voltage which could be 240 Vac in many countries)

Line frequency (f_{LINE}): 50 Hz/60 Hz (This is often specified in a range of 47−63 Hz and for calculations such as hold-up time, one has to factor in the lowest value specified)

Output Voltage (V_{out}): 385 V (This value has to be above 1.414 • Vac_{HL} and is typically between 385 and 400 V for universal input operation)

Maximum output voltage ($V_{out(max)}$): 415 V (This value is usually 7−10% above the V_{out} value and is determined by the accuracy of the OVP level of the PFC controller – conversely, the selection of the PFC controller has to be made based on this specification if it is determined by other component stress levels and derating factors).

PFC maximum output power (P_{out}): 270 W (This is the specified output power for the PFC stage. It is important to factor in the follow-on stage efficiency when specifying this parameter – it will always be higher than the specified maximum system output power)

Switching frequency (f_{sw}): 65 kHz (This parameter helps set the value of the boost inductor). For the NCP1654, the frequency is set internally with 3 options, which are 65 kHz, 133 kHz, and 200 kHz. The 65 kHz is the common choice for easier EMI compliance, while 133 kHz and 200 kHz are chosen for applications needing lower profile or smaller inductor.

Output voltage ripple ($V_{ripple(p-p)}$): 20 V (This parameter is often specified in percentage of output voltage, ±5% is a very typical specification)

Hold-up time ($t_{hold-up}$): 16 ms (This parameter specifies the amount of time the output will remain valid during line drop-out. One line cycle is typically specified. For PFC alone, this spec is not applicable, but the PFC output capacitor is the single largest determinant of the hold-up time)

Estimated efficiency (η): 93% (This parameter is an initial estimate that is used to size the power stage components – high level of accuracy is not needed for the design procedure).

Step 2: Design the Boost Inductor (PFC Coil)

The (maximum) peak inductor current is the about half the value of the corresponding value in CrM and FCCrM. This does not take into account the peak to peak ripple due to non-infinite inductor value. This current is given by:

$$I_{coil,pk(\max)} = \frac{\sqrt{2} \cdot P_{out}}{\eta \cdot Vac_{LL}} = \frac{\sqrt{2} \cdot 270}{0.93 \cdot 88} = 4.67A$$

Similarly, ignoring the contribution of the p-p ripple (which can be shown to contribute less than 10% to the rms value for most selections), the rms current in the inductor is given by:

$$I_{coil,rms} = \frac{P_{out}}{\eta \cdot Vac_{LL}} = \frac{270}{0.93 \cdot 88} = 3.3A$$

Unlike the CrM and FCCrM topologies, there is no minimum or maximum inductance value equation for the CCM PFC (except that to maintain the CCM operation, the ripple should be less than 100% p-p). The inductor value selection is somewhat iterative and is determined based on the peak current, ripple current, output ripple voltage, components stress and losses, as well as board space. Typically, higher inductance value will reduce ripple and stress levels, but use up significant board space. In contrast, lower inductance value will increase the ripple and peak currents, but will have benefits of smaller size and lower current at diode turn-off – as will be shown in the results section, this lower diode turn-off current results in significant improvement of diode switching characteristics and efficiency.

A first approximation of the inductor value L can be obtained with the following equation:

$$L = \frac{{Vac_{LL}}^2}{2 \cdot I\% \cdot f_{SW} \cdot P_{out} \cdot \eta} \cdot \left[1 - \left(\frac{\sqrt{2} \cdot Vac_{LL}}{V_{out}}\right)\right]$$

Where:

- L = inductance value
- I% = ratio of allowable pk-pk ripple current to peak current in the inductor (25−45% typical)

The following chart helps in defining a range of inductances based on the allowable ripple current. It is recommended to use a value of inductance that falls within the 25−45 % range of input current ripple. In this particular design, p-p ripple value applied was 45% and it resulted in the inductor value of 650 μH. The resultant modified peak current is 22.5% above the calculated value above (4.67 • 1.225 = 5.72 A).

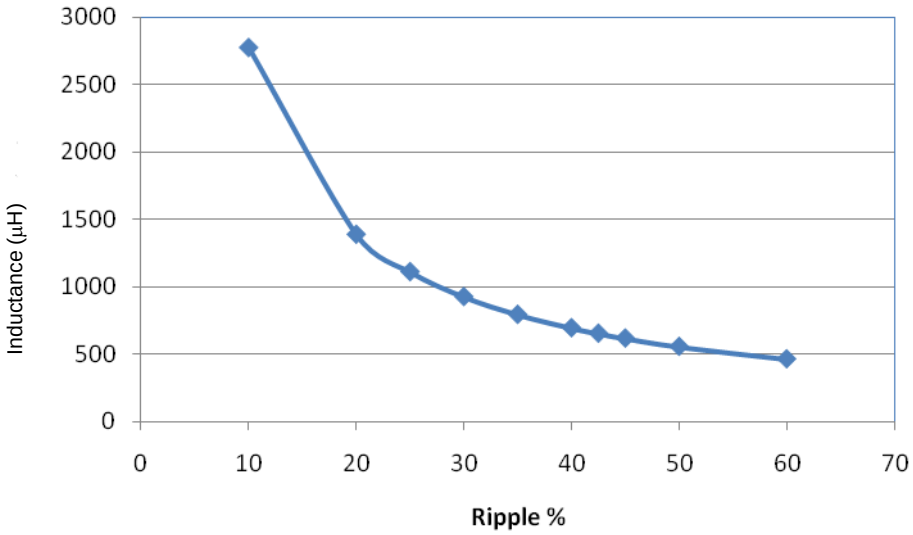

Figure 6−2. CCM Inductance Value as a Function of p−p Ripple

Step 3: Design the Power Stage Components

The power stage components are designed based on their current and voltage ratings. The inductor design is already covered in step 2. The bridge diode should be selected based on peak inductor current rating and will have the power dissipation given by:

$$P_{bridge} = \frac{4\sqrt{2}}{\pi} \cdot \frac{V_f}{Vac_{LL}} \cdot \frac{P_{out}}{\eta} \approx 1.8 \frac{V_f}{Vac_{LL}} \cdot \frac{P_{out}}{\eta}$$

The MOSFET is selected based on peak voltage stress ($V_{out(max)}$ + margin) and rms current stress:

$$I_{M(rms)} = \frac{P_{out}}{\eta \cdot Vac_{LL}} \cdot \sqrt{1 - \frac{8 \cdot \sqrt{2} \cdot Vac_{LL}}{3 \cdot \pi \cdot V_{out}}} = \frac{270}{0.93 \cdot 88} \sqrt{1 - \frac{8 \cdot \sqrt{2} \cdot 88}{3 \cdot \pi \cdot 385}} = 2.81\,\text{A}$$

Using a 600 V, 0.19 ohm FET, will give conduction losses of (assuming that $R_{ds(on)}$ increases by 80% due to temperature effects):

$$P_{cond} = {I_{M(rms)}}^2 \cdot R_{ds(on)} = 2.81^2 \cdot 0.19 \cdot 1.8 = 2.7\ \text{W}$$

While switching losses are harder to predict without getting into the details of switching waveforms and diode recovery characteristics, etc., one component of the switching losses that can be predicted is the capacitive turn-on losses.

$$P_{sw,cap} = \frac{2}{3} \cdot Coss_{25} \cdot \sqrt{25} \cdot V_{on}^{1.5} \cdot f = 0.666 \cdot 780 \cdot 10^{-12} \cdot 5 \cdot (385)^{1.5} \cdot 36000 = 0.71\,\text{W}$$

Here, the nonlinear nature of the capacitance is taken into account. The other switching losses of the FET are dependent on the choice of boost diode, switching speeds and the choice of snubbers in the circuit. In the CCM circuit, the diode recovery losses often dominate the switching losses and hence, the choice of FET is less critical in this application.

The choice of boost diode is more critical in the CCM applications. As mentioned before, the diode current at its turn-off is non-zero unlike the CrM application. As a result, there is significant reverse recovery phenomenon that leads to dissipation in the diode and the FET. One option is to use advanced rectifiers such as SiC diodes and such. However, they are expensive and their higher forward drop offsets some of the gains of reduced switching losses. For this application, a soft recovery boost rectifier (LQA08TC600) was used and it worked well due to its softer recovery characteristics and additional snubbers were not necessary. The average diode current is the same as the output current ($I_d = P_{out}/V_{out} = 270/385 = 0.7$ A). So, the diode conduction losses are $I_d \bullet V_f$ (generally less than 1 W). The peak current seen by the diode will be the same as the inductor peak current (4.67 A).

Step 4: Output Capacitor Design

The output capacitor is designed considering 3 factors: output voltage ripple, output current ripple and the hold-up time. The output voltage ripple is given by:

$$V_{ripple(p-p)} = \frac{P_{out\cdot}}{2 \cdot \pi \cdot f_{line} \cdot C_{out} \cdot V_{out}}$$

The capacitor rms current is given by (assuming a resistive load):

$$I_{Cout(rms)} = \sqrt{\frac{32 \cdot \sqrt{2} \cdot P_{out}^2}{9 \cdot \pi \cdot Vac_{LL} \cdot V_{out} \cdot \eta^2} - (\frac{P_{out}}{V_{out}})^2}$$

However, almost always, the size and the value of the capacitor are determined by the hold-up time which is given by:

$$t_{hold-up} = \frac{C_{out} \cdot (V_{out}^2 - V_{\min}^2)}{2 \cdot P_{out}}$$

In this case, a 220 μF capacitor was chosen that satisfies the conditions above. The peak-peak ripple is 10 V, the rms current is 1.83 A and the hold-up time is 20.82 ms (for a 330 V V_{min}).

Step 5: Set FB, OVP and UVP Levels

The OVP level in the NCP1654 is set at 5% above the nominal V_{out} given by

$$V_{out,OVP} = 105\% \cdot V_{out,nom}$$

As the nominal output voltage is set at 385 V. The OVP level is:

$$V_{out,OVP} = 105\% \cdot 385 = 404\,V$$

The choice of feedback resistors does not play a critical role in setting the OVP level. As a result, the feedback divider values are selected as follows.

First, choose the value of the lower resistor, R_{fbL}. There is a trade-off between the noise immunity and the power losses when choosing R_{fbL}. In this application, we select 23.2 kΩ as R_{fbL} that leads a 108 μA feedback current and 42 mW losses. The value of upper resistor R_{fbU} is then given by:

$$R_{fbU} = \frac{V_{out} - V_{REF}}{V_{REF}} \cdot R_{fbL}$$

Where:

- V_{REF} is the internal reference voltage for V_{out} feedback (2.5 V typical).
- $R_{fbU} = R_{fbU1} + R_{fbU2}$ is the total feedback resistor placed between V_{out} and FB pin.

In this case, V_{out} is 385 V and R_{fbL} is 23.2 kΩ, one must then select the following R_{fbU} resistance:

$$R_{fbU} = \frac{385 - 2.5}{2.5} \cdot 23.2\,k\Omega = 3.549\,M\Omega$$

The feedback string is implemented using two equal resistors $R_{fbU1} = R_{fbU2} = 1.8$ MΩ.

The Under-Voltage Protection (UVP) function has 2 purposes.

- Open Loop Protection - Protect the power stage from damage at feedback loop abnormal, such as V_{fb} is shorted to ground, the feedback resistor R_{fbU} is open, or the FB pin is left open.
- Shutdown mode - Disables the PFC stage and forces a low consumption mode. This feature helps to meet stringent stand-by specifications. Power Factor being not necessary in stand-by, the PFC stage is generally inhibited to save the pre-converter losses. To further improve the stand-by performance, the PFC controller should consume minimum current in this mode.

The UVP level in the NCP1654 is set when V_{fb} is below 8% of V_{REF}, the device is shut down. The device automatically starts operation when the output voltage goes above 12% of V_{REF}. In normal situation of boost converter configuration, V_{fb} has to be greater than 12 % of V_{REF} to enable the NCP1654 to operate. For this case, the UVP level is set at:

$$V_{out,UVP} = 12\% \cdot V_{out,nom} = 12\% \cdot 385 = 46V$$

It is around 32 Vac input, which is much lower than the minimum input voltage, i.e. 85 Vac, and is ok for start-up.

Step 6: Input Voltage Sensing

The NCP1654 monitors the input voltage, V_{in}, which is the rectified AC line sinusoid for brown-out, over-power limitation (OPL), and PFC duty cycle modulation. This sensing circuit consists of:

R_{boU} and R_{boL} are dimensioned to adjust the threshold of brown out protection. Because of the safety consideration, it is recommended to split this upper side brown out resistor into 2 or more resistors.

C_{BO} that forms a low pass filtering together with R_{boL} to get the average value of input signal. A time constant in the range of around 5 times the V_{in} period should be targeted to make V_{bo} substantially constant and proportional to the mean input voltage as the rule of thumb:

$$V_{bo} = \frac{R_{boL}}{R_{boL} + R_{boU}} \langle V_{in} \rangle$$

The NCP1654 starts to operate as V_{bo} exceeds 1.3 V and keeps operating until V_{bo} goes below 0.7 V. The 600 mV hysteresis prevents the system from oscillating.

$R_{boU} + R_{boL}$ should be relatively high impedance to limit the current drawn and the associated losses. Please note however that given the bias current of the brown-out comparator (0.5 μA maximum), it is recommended to set the current flowing through R_{boU} and R_{boL} to be in the range or higher than 5 μA at low line. In this application, we use 82.5 kΩ for R_{boL}, which leads to a bias current of:

$$0.7V \big/ 82.5k = 8.5\,\mu A$$

Second, select R_{boU} according to $V_{ac,on}$, the minimum AC input voltage to start PFC, which comes from:

$$R_{boU} = \frac{\sqrt{2}V_{ac,on} - V_{BOH}}{V_{BOH}} R_{boL}$$

In this application, 75 Vac is targeted as $V_{ac,on}$. Hence,

$$R_{boU} = \frac{\sqrt{2} \cdot 75V - 1.3V}{1.3V} \cdot 82.5\,k\Omega \approx 6.65\,M\Omega$$

Here R_{boU} is split into 2 parts, R_{boU1} and R_{boU2} both equal to 3.3 MΩ for a total of 6.6 MΩ resistance.

Third, select C_{BO} to make the time constant be around 5 times T_{Vin}, the cycle time of V_{in} by

$$C_{BO} \approx \frac{5 \cdot T_{Vin}}{R_{boL}}$$

In this application, T_{Vin} is 10 ms since the ac input line is 50 Hz. So. Here 0.47 μF is selected because it is the closest normalized value.

$$C_{BO} \approx \frac{5 \cdot 10ms}{82.5k\Omega} = 0.6\,\mu F$$

Fourth, check Vac_{off}, the PFC brown-out off threshold of AC input voltage.

$$V_{ac,off} = \frac{V_{BOL}}{K_{BO} \cdot \frac{2\sqrt{2}}{\pi} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}}\right)}$$

Where K_{BO} is the scaling factor formed by R_{boU} and R_{boL} and f_{BO} is the corner frequency of the BO filter.

In this application,

$$V_{ac,off} = \frac{0.7}{0.0123 \cdot \frac{2\sqrt{2}}{\pi} \cdot \left(1 - \frac{4.2Hz}{3 \cdot 50Hz}\right)} = 64.8\,Vac$$

which seems acceptable. By reducing CBO, one can increase this level and vice versa. Note that this calculation result is just a reference since it doesn't include the voltage drop on the current loop, i.e. EMI filter and bridge diode etc.

Step 7: Current Sense Circuit

The current sense signal across the sense resistor is actually a negative voltage. However, insertion of a resistor between R_{sense} and pin 3 of the NCP1654 allows that signal to be converted into a current. The value of R_{sense} is chosen to minimize its impact on efficiency at low line, full load (here, 0.1 Ω is chosen). The equation for R_{cs} is given by:

$$R_{cs} = \frac{I_{coil,pk} \cdot R_{sense}}{I_{pin3(\min)}} = \frac{4.67 \cdot 0.1}{185 \cdot 10^{-6}} = 2.52\,\text{k}\Omega$$

R_M adjusts the maximum power the PFC stage can supply given the chosen output voltage level. By choosing R_M high enough, you can force the “Follower Boost Operation”. Use the following equation to select R_M:

$$R_M = 70\% \cdot \eta \frac{2\pi R_{CS} \cdot \Delta V_{CONTROL} \cdot V_{REF}}{\sqrt{2} \cdot R_{sense} \cdot K_{BO} \cdot V_{outLL} \cdot P_{out,max}} \cdot Vac_{LL} = 45.4k\Omega$$

In this example, follower boost is not utilized, so the V_{outLL} value is same as V_{out} and plugging in the other values results in a R_M value of 45.4 kΩ - a 47 kΩ value is used. The value of C_M is chosen so that the $R_M.C_M$ time constant is at least 5 times the switching period. Based on this, the C_M value is calculated to be 1 nF.

Additional design steps such as feedback compensation, Vcc generation follow conventional methods and are not covered here.

Circuit Schematics and Bill of Materials

The circuit schematic of the CCM PFC converter described in the design steps above is provided in Figure 6−3. The Bill of Materials follows in Table 6−1.

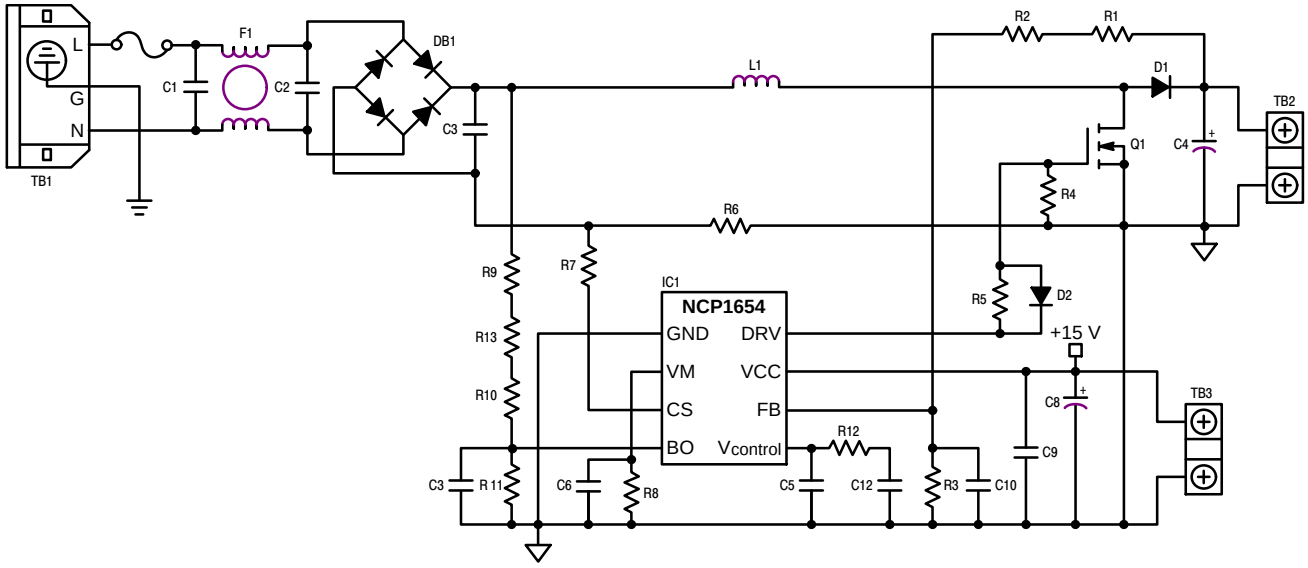

Figure 6−3. Circuit Schematic of the CCM PFC Circuit Based on NCP1654

Table 6−1. Bill of Materials for CCM PFC Circuit Based on the NCP1654

Quantity	Reference	Description	Part Number	Manufacturer
1	C1	0.47 μF / 275 V type X2	F1772-447-2000	VISHAY
1	C2	0.47 μF / 275 V type X2	F1772-447-2000	VISHAY
1	C3	0.1 μ, 400 V, High Ripple, Polypropylene Cap	ECWF4104JL	Matsushita
1	C4	180 μF 450 V	2222 159 47181	BC Components
1	C5	0.22 μF / 50V	K224K20X7RF53H5	VISHAY
1	C7	0.47 μF / 50V	K474K20X7RF53H5	VISHAY
1	C9	0.1 μF / 50V	K104K15X7RF53H5	VISHAY
1	C6	1 nF / 50 V	K102K15X7RF53H5	VISHAY
1	C10	100 pF / 50 V	K101K15X7RF53H5	VISHAY
1	C8	22 μF / 25 V	2222 013 36229	BC Components
1	C12	2.2 μF / 50 V	B32529D5225J	EPCOS
1	DB1	600 V, 8.0 A bridge diode	GBU8J	VISHAY
1	D1	8.0 A, 600 V	MSR860G	ON Semiconductor
1	D2	1N4148	1N4148	VISHAY
1	F1	5 A fuse, Time Delay Fuse (FST 5x20)	0034.3124	SCHURTER
1	IC1	CCM PFC controller	NCP1654	ON Semiconductor
1	L1	650 μH	GA3199-AL	CoilCraft
			2702.0010A	Pulse
1	L2	4 A, 2 x 6.8 mH, CM choke	B82725-J2402-N20	EPCOS
1	L3	150 μH, 5A, WE-FI series, DM choke	7447055	Wurth Elektronik
1	Q1	20 A 600 V MOSFET	SPP20N60C3	Infineon
2	R1	Resistor, Axial Lead, 1.8 M, 1/4 W, 1%	CCF501M80FKE36	VISHAY
	R2	Resistor, Axial Lead, 1.8 M, 1/4 W, 1%	CCF501M80FKE36	VISHAY
2	R9	Resistor, Axial Lead, 3.3 M, 1/4 W, 1%	CCF503M30FKE36	VISHAY
	R13	Resistor, Axial Lead, 3.3 M, 1/4 W, 1%	CCF503M30FKE36	VISHAY
1	R10	Jumper	Jumper	
1	R3	Resistor, Axial Lead, 23.7 k, 1/4 W, 1%	CCF5023K7FKE36	VISHAY
1	R4	Resistor, Axial Lead, 10 k, 1/4 W	CCF5010K0FKE36	VISHAY
1	R5	Resistor, Axial Lead, 10, 1/4 W	CCF5010R0FKE36	VISHAY
1	R6	Resistor, Axial Lead, 0.1, 3 W, 1% LVR3 series	LVR03 R1000 F E12	VISHAY
1	R7	Resistor, Axial Lead, 3.6 k, 1/4 W 1%	CCF503K60FKE36	VISHAY
1	R8	Resistor, Axial Lead, 47 k, 1/4 W	CCF5047K0FKE36	VISHAY
1	R11	Resistor, Axial Lead, 82.5 k, 1/4 W, 1%	CCF5082K5FKE36	VISHAY
1	R12	Resistor, Axial Lead, 12 k, 1/4 W, 1%	CCF5012K0FKE36	VISHAY
1	TB1	AC inlet connector	GSF1.1201.31	SCHURTER
1	TB2	DC output plug socket	20.101/2 (order code 3044531)	IMO
1	TB3	Vcc connector plug socket	PM5.08/2/90. (order code 5015571)	WEIDMULLER
1	HS1	Heatsink (2.9 °C/W)	SK481 100mm	Fischer elektronik
2	Q1	Isolator TO220	3223-07FR-43	BERGQUIST
	D1	Isolator TO220	3223-07FR-43	BERGQUIST
3	DB1	Clip for heatsink (TO220)	THFU 1	Fischer elektronik
	Q1	Clip for heatsink (TO220)	THFU 1	Fischer elektronik
	D1	Clip for heatsink (TO220)	THFU 1	Fischer elektronik

Results and Performance Curves

The operating results of the NCP1654 based design described above are shown in Table 6−2.

Table 6−2. Results of the 270 W CCM PFC Using NCP1654

Vin (ac)	**Pin** (W)	**Vo** (V)	**Io** (A)	**Output Power** (W)	**Po**	**Efficiency**	**PF**	**THD%**
100	28.44	382.78	0.070	26.97	10%	94.83%	0.975	
	41.56	381.95	0.104	39.80	15%	95.76%	0.984	
	56.07	381.79	0.141	53.88	20%	96.10%	0.991	
	139.59	381.40	0.350	133.65	50%	95.75%	0.996	
	280.91	381.26	0.701	267.10	100%	95.08%	0.998	4.6
115	28.70	383.03	0.072	27.39	10%	95.43%	0.968	
	42.15	382.18	0.105	40.31	15%	95.64%	0.981	
	55.52	381.83	0.140	53.42	20%	96.22%	0.985	
	138.41	381.43	0.349	133.28	50%	96.30%	0.994	
	278.29	381.30	0.700	266.77	100%	95.86%	0.997	4.6
230	27.67	382.63	0.069	26.55	10%	95.97%	0.757	
	42.04	382.31	0.106	40.63	15%	96.65%	0.858	
	55.33	382.13	0.141	53.78	20%	97.21%	0.905	
	136.59	381.64	0.350	133.71	50%	97.89%	0.978	
	272.60	381.36	0.701	267.15	100%	98.00%	0.991	7.2

From the information in Table 6−2, we can confirm that the full load efficiency at 100 Vac is above 95%. In addition, even at 20% load (which is a key performance criterion from regulatory viewpoint), the efficiency is above 96%. These results are achieved with a combination of optimal component choices and careful layout of the PCB. It can also be observed that the power factor remains above 0.9 for high line (230 Vac) at loads down to about 50 W (20%). The THD of the circuit at full load and high line is measured at 7.2% which is quite respectable.

The input harmonic spectrum for 230 Vac and full load is shown in Figure 6−4 against class D limit and it is shown that the circuit comfortably passes the IEC61000-3-2 requirements. Similar result was observed with the load reduced to 75 W.

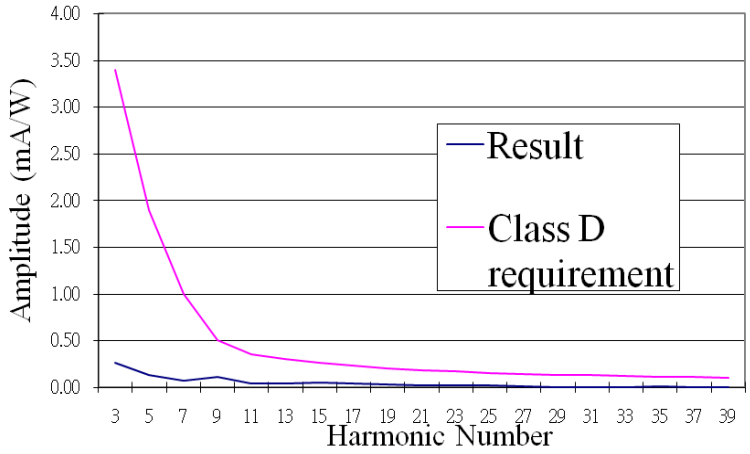

Figure 6−4. Harmonic Spectrum of the 270 W CCM Converter

Some of the design trade-offs involved in component choices are illustrated next using changes in two key components and how they impact the efficiency at critical points. In the above design, the MOSFET used is a 20 A, 600 V (0.19 Ω) and the boost diode is 8 A, 600 V. By experimenting with 15 A, 600 V FET and 3 A, 600 V diode from the same vendors/component class, following result variations are obtained at 100 Vac input. Similar performance changes are observed at the 115 Vac input.

Table 6−3. Impact of Component Variations on Efficiency (100 Vac)

100% load	15 A FET	20 A FET
3 A diode	94.82%	94.99%
8 A diode	94.89%	95.08%
20% load	15 A FET	20 A FET
3 A diode	95.88%	95.91%
8 A diode	96.06%	96.08%

The results of Table 6−3 offer interesting insight into the trade-offs involved in component selection for PFC circuits. First, it is interesting to note that the efficiency change when going from [15 A FET, 3 A diode] combination to [20 A FET, 8 A diode] combination results in about 0.25% efficiency improvement at full load (0.2% at 20% load). This implies that the gains in the conduction losses made by going to bigger FET are offset by the increased switching losses associated with higher Coss. Depending on the costs of the available devices and efficiency targets, Table 6−3 offers an interesting set of options for selecting right components and optimizing the design. In another set of experiments, the boost diode was replaced with a different category of diode (Q series to X series) resulted in efficiency drop of about 0.5% at low line and 20% load.

Finally, a change in the inductor value from 650 μH to 250 μH was tried. Such a drastic reduction in inductor value takes the circuit closer to DCM at lighter loads and the power factor gets worse as shown in Table 6−4. However, since the ripple value gets bigger, the inductor current at the diode turn-off instance is significantly below its peak and average values. The result of this is that the diode recovery effects are not as bad and the efficiency and EMI improve. For a given design requirement, this may be a good trade-off to make. Comparing with Table 2, the efficiency improves by 0.2% at full load and by about 0.33% at 50% load (at 100 Vac). However, the 20% load efficiency reduces by about 0.27% − this is caused by higher ripple in the inductor causing additional core losses.

Table 6−4. Impact of Reducing the Inductor Value in CCM

Vin (ac)	**Pin** (W)	**Vo** (V)	**Io** (A)	**Output Power** (W)	**Po**	**Efficiency**	**PF**	**THD%**
100	28.55	383.71	0.071	27.09	10%	94.90%	0.966	13.6
	41.97	382.58	0.105	40.13	15%	95.62%	0.977	12.2
	56.52	382.06	0.142	54.16	20%	95.83%	0.982	12.2
	139.08	381.53	0.350	133.62	50%	96.08%	0.992	9.3
	280.26	381.31	0.700	267.05	100%	95.29%	0.996	5.9
115	28.97	383.66	0.072	27.54	10%	95.06%	0.969	12.0
	42.29	382.67	0.106	40.54	15%	95.85%	0.972	11.9
	55.75	382.16	0.140	53.60	20%	96.14%	0.978	11.8
	138.42	381.59	0.350	133.48	50%	96.43%	0.989	11.6
	277.90	381.35	0.700	266.93	100%	96.05%	0.996	5.1
230	27.70	382.70	0.070	26.60	10%	96.02%	0.731	23.0
	41.08	382.45	0.104	39.77	15%	96.82%	0.839	15.5
	55.43	382.14	0.141	53.88	20%	97.21%	0.893	12.4
	136.72	381.61	0.351	133.83	50%	97.89%	0.954	15.7
	272.05	380.29	0.701	266.58	100%	97.99%	0.980	13.9

The results from Table 6−2 are plotted in the following figures for understanding performance over line and load.

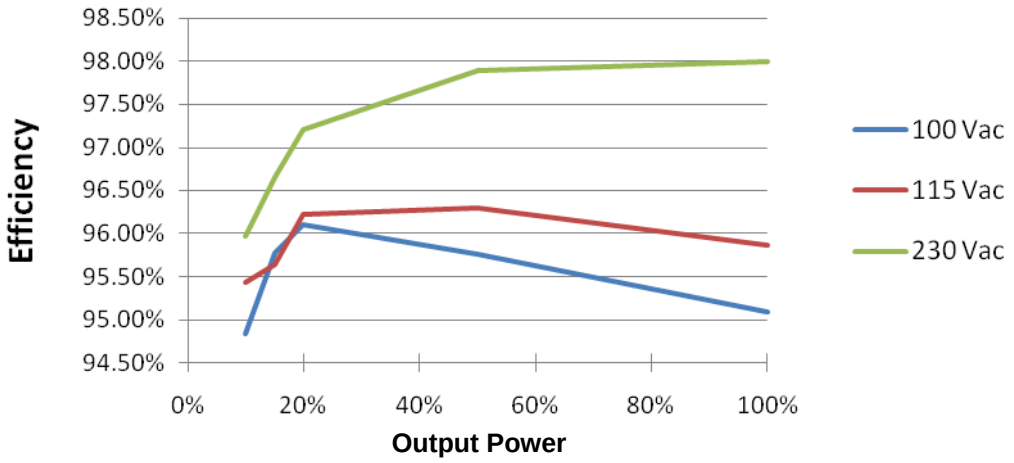

Figure 6−5. Efficiency Performance of the 270 W CCM Design

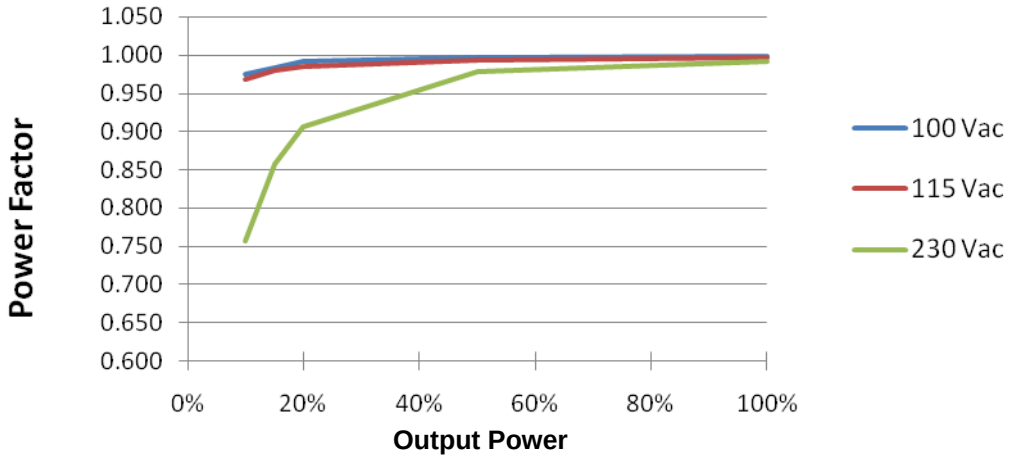

Figure 6−6. Power Factor Performance of the 270 W CCM Design

CHAPTER 7

Interleaved PFC

Interleaved PFC is an emerging solution that becomes particularly popular in applications where a strict form factor has to be met, for instance, in low profile notebook adapters or in LCD TVs. This section will consider the interleaving of two FCCrM PFC stages that efficiently address the 300 W application of our interest. Interleaving CCM PFC stages is also possible. However, this option should be devoted to much higher power applications (above 1 kW) and will not be detailed here.

This section will give an overview of the interleaved PFC characteristics and will deal with the main design steps. Practical results are given as obtained with the NCP1631. More detailed information is available at www.onsemi.com (see references).

Introduction

Interleaving consists in paralleling two “small” stages in lieu of a bigger one, which may be more difficult to design. Practically, two 150 W PFC stages are combined to form our 300 W PFC pre-regulator. This approach has several merits like the ease of implementation, the use of smaller components or better heat distribution.

Also, Interleaving extends the power range of Critical Conduction Mode that is an efficient and cost-effective technique (no need for low t_{rr} diodes). Furthermore, if the two stages are operated out-of-phase, the current ripple is significantly reduced. In particular, the input current looks like a CCM one and the rms current within the bulk capacitor is dramatically reduced.

Interleaving Method

When designing a CrM or FCCrM interleaved PFC, maintaining an out-of phase operation is the main difficulty. This is because the switching frequency is not fixed and a nominal operation requires the MOSFET turn on to be delayed until the very moment the valley is detected. Hence, each phase must beat at its own rhythm and at the same time stay synchronized to the other branch, thus requiring a sophisticated control circuitry.

In the traditional master/slave approach, the master branch operates freely, while the other phase is controlled to follow with a 180° phase shift. The challenge is to drive the slave branch so that it never enters CCM nor exhibits undesired dead-times [1].

The NCP1631 utilizes an interactive-phase option where the two branches operate independently, in CrM, inherently preventing risks of undesired dead-times or continuous conduction mode sequences. Still, the two phases interact with each other for out-of-phase operation. It is worth noting that the NCP1631’s unique interleaving technique (which will be described in this chapter) substantially maintains the wished 180° phase shift between branches in all conditions including start-up, fault or transient sequences.

More generally, the NCP1631 integrates a dual MOSFET driver for interleaved, 2-phase PFC applications. It drives the two branches in so-called ***F**requency **C**lamped **Cr**itical conduction **M**ode* (***FCCrM***) where each phase operates in ***Cr**itical conduction **M**ode* (CrM) in the most stressful conditions and in ***D**iscontinuous **C**onduction **M**ode* (DCM) otherwise, acting as a CrM controller with a frequency clamp (given by the oscillator). According to the conditions, the PFC stage actually transitions from DCM to CrM (and vice versa) with no discontinuity in operation and without degradation of the current shape. Traditional CrM control methods fail to offer this integrity of current shape, even though some of them transition to DCM through use of frequency clamping.

The NCP1631 capitalizes on its FCCrM operation mode to manage the out-of-phase operation by the simple means of an oscillator. As sketched by Figure 7−1, the oscillator voltage swings at twice the frequency of each branch. When it reaches its 4-V lower threshold, the circuit generates a clock signal alternatively for phase 1 or phase 2.

There are two possible cases to consider:

1. The cycle time of the inductor current is shorter than two oscillator periods. When the clock signal is generated, the inductor of the branch corresponding to the clock is demagnetized (the inductor current has already reached zero) and a new cycle can immediately start. We have a fixed frequency DCM operation mode in each branch as depicted by the right side of Figure 7−1. Out-of-phase operation is naturally obtained as the result of the interleaved clock signals.

2. The inductor current is not at zero when the clock signal corresponding to the inductor branch occurs. The circuit would enter Continuous Conduction Mode (CCM) if the MOSFET turned on in that moment. Instead, the next conduction phase is delayed until the core is reset and the inductor current reaches zero. The clock signal remains high for this waiting period and the MOSFET turns on as soon as the coil current has reached zero. In other words, critical conduction mode (CrM) operation is obtained. The oscillator keeps on discharging for the waiting period, reducing the oscillator frequency and delaying the occurrence of the next clock signals. It can be analytically shown that an appropriate selection of the oscillator charge and discharge currents leads to stable out-of-phase operation as depicted by the left side of Figure 7−1.

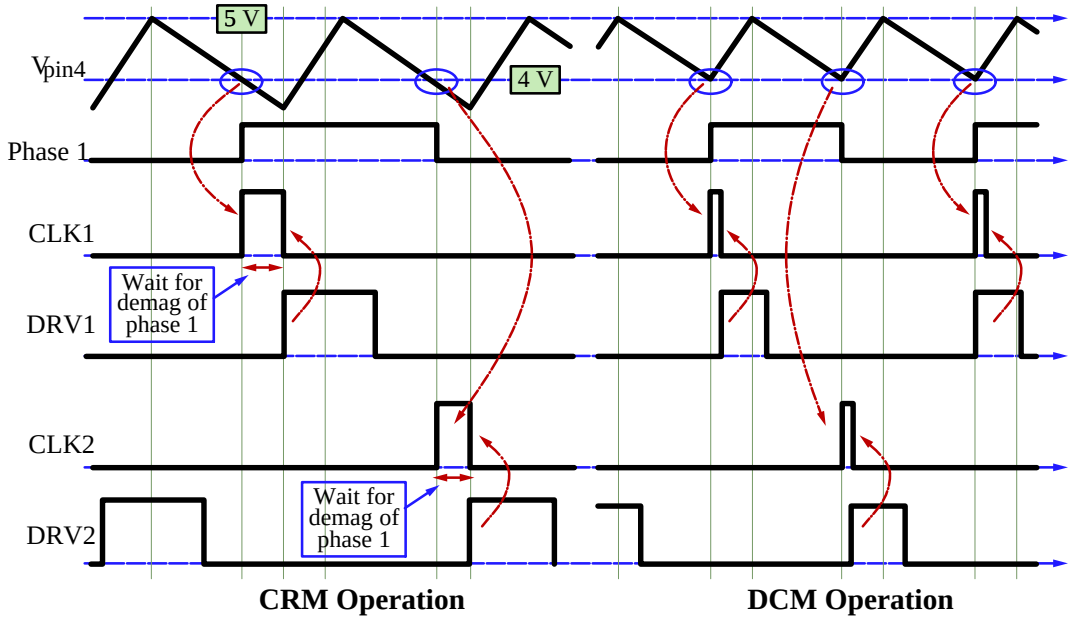

Figure 7−1. Interleaved Clock Generation

As a voltage mode controller, the NCP1631 forces the MOSFET on-time to be identical in both branches. The demagnetization time that only depends on the conduction time and on the line and output voltages is then the same in both branches as well $\left(t_{demag} = t_{on} \cdot \frac{V_{in}}{V_{out} - V_{in}} \right)$. Hence if we neglect the tolerance in the timing circuitry that adjusts the on-time in response to the control signal for each circuit, the current cycle duration is the same in the two branches even if their respective inductors do not have the same inductance.

Finally, the only source of current unbalancing is the inductor tolerance. One can easily show that the current sharing is governed by the following equation:

$$\frac{I_{in(branch1)}}{I_{in(branch2)}} = \frac{L_{branch2}}{L_{branch1}}$$

Where:

- $I_{in(branch1)}$ and $I_{in(branch2)}$ are the averaged input currents drawn by phase 1 and phase 2 respectively
- $L_{branch1}$ and $L_{branch2}$ are the inductance values of phase 1 and phase 2 respectively

Practically, if the inductance dispersion is in the range of ±5%, the possible current imbalance is less than ±10%.

Housed in a SOIC16 package, the NCP1631 also offers many other useful features. In particular, the circuit adapts its frequency clamp to optimize the PFC stage efficiency over the line/load range: below a programmable load level, the frequency linearly decays as a function of the power to maintain high efficiency levels even in very light load (frequency fold-back).

A NCP1631-driven PFC stage also eases the design of the downstream converter by providing it with a narrow range dc voltage. With this goal, the circuit features a “pfcOK” output pin to disable the downstream converter until the bulk capacitor is charged and no fault is detected. In addition, the NCP1631 dramatically reduces the output voltage deviations during abrupt

load or line transients (when the low bandwidth of the PFC loop normally causes large overshoot and undershoot problems) by:

- Dedicating one specific pin for an optimal programming of the Over-Voltage Protection level
- Drastically speeding-up the regulation loop when the output voltage is 4.5% below its desired level (***dynamic response enhancer***).

As a matter of fact, the downstream converter can be optimally designed since the PFC stage provides it with a very narrow voltage range.

Finally, the NCP1631 protections (maximum current limitation, in-rush current detection, under-voltage protection, brown-out detection...) protect the system from most possible over-stresses and make the PFC stage extremely robust and reliable.

Main Merits of Interleaved PFC

The simplified schematic of Figure 7−2 shows the two paralleled channels. The first branch absorbs a current $I_{branch1}$ and provides the output with I_{D1}. The other branch draws $I_{branch2}$ and generates I_{D2}. These currents are similar to those exhibited by a classical one-phase ***FCCrM*** PFC stage. However, we will see that as a result of the out-of-phase operation, the total current absorbed by the interleaved PFC ($I_{in(total)}$ of Figure 7−2) and the total current provided by the boost diodes ($I_{D(total)}$ of Figure 7−2) have a significantly reduced ripple compared to that obtained with conventional one-phase PFC stages.

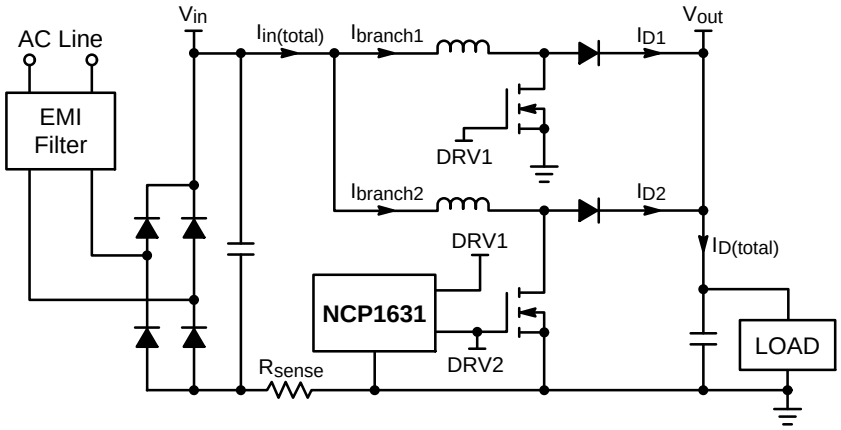

Figure 7−2. Simplified Schematic of an Interleaved PFC Stage

1. The input current ripple is minimized:

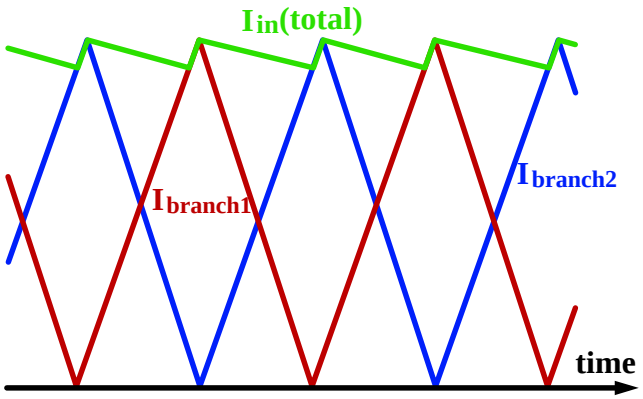

Figure 7−3. The Total Current Exhibits a Reduced Ripple

The inductor current within each branch exhibits a large ripple (CrM operation) but as illustrated by Figure 7−3 and detailed in [2], out-of-phase operation results in a very small ripple on the total current drawn by the PFC stage. In fact, there is no ripple at all when the input voltage is half of the output voltage (the up and down-slopes being the same) and goes to a maximum value (100% of the averaged current − peak to peak) when V_{in} is near zero or close to V_{out} (see Figure 7−4).

More specifically, assuming a permanent CrM operation (no frequency clamp − ([1])) and a 180- phase shift, one can compute the input current ripple as follows:

$$\frac{\Delta I_{in(pk-pk)}}{I_{in}} = \frac{\left(2 \cdot \frac{V_{in}}{V_{out}}\right) - 1}{\frac{V_{in}}{V_{out}}} \qquad if \quad \frac{V_{in}}{V_{out}} > 0.5$$

$$\frac{\Delta I_{in(pk-pk)}}{I_{in}} = \frac{1 - \left(2 \cdot \frac{V_{in}}{V_{out}}\right)}{1 - \frac{V_{in}}{V_{out}}} \qquad if \quad \frac{V_{in}}{V_{out}} < 0.5$$

The following figure summarizes the ripple variations as a function of $\left(\frac{V_{in}}{V_{out}}\right)$.

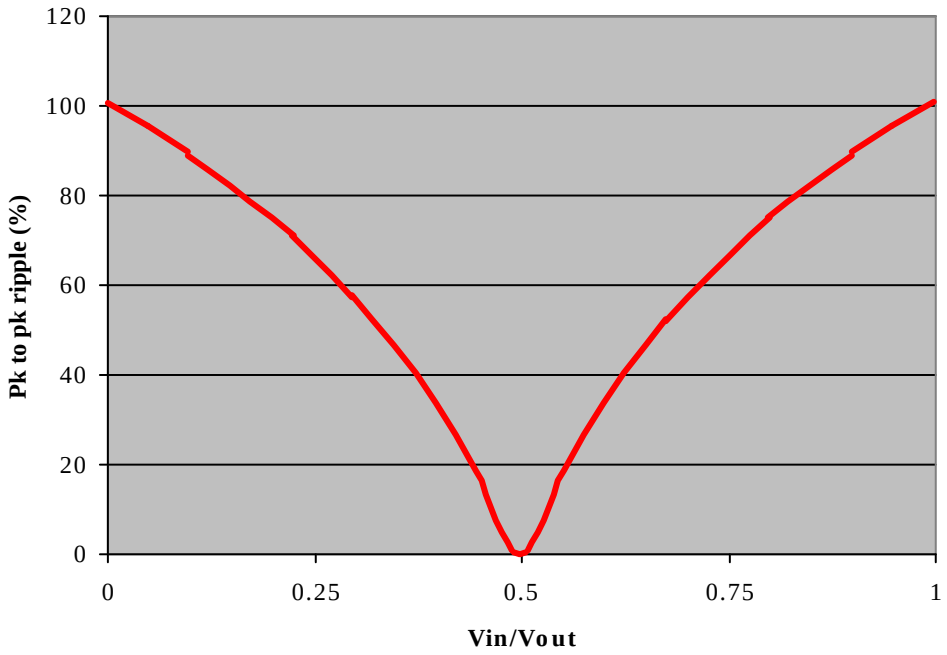

Figure 7−4. Peak-to-Peak Ripple of the Input Current as a Function of the Line Magnitude

As a matter of fact, the input current looks similar to that of a CCM PFC in the sense that the current ripple is small.

2. The ripple of the current that feeds the bulk and the load is minimized:

As shown by Figure 7−5, still assuming a CrM operation, the 180° phase shift reduces the ac content of the total current delivered by the 2 branches to the bulk capacitor and the load ($I_{D(total)}$ of Figure 7−2). This is because the two phases exhibit interleaved refueling sequences. Furthermore, if the input voltage is less than half of the output voltage, there is no overlap at all between the two-branch refueling intervals. This characteristic leads to a dramatically reduced rms current within the bulk capacitor at low line conditions in wide mains applications, for an easier, cheaper and more robust design.

[1] - *The current ripple increases if the PFC stage operates in DCM as a result of the dead-times. However, the PFC stage is designed to operate in CrM in the most severe conditions, the frequency being only clamped when the line current is relatively low. Thus, FCCrM does not alter the benefits in term of input and output current ripple.*

In the wide mains case (no overlap between the refueling times of the two phases), the maximum rms value of the global refueling current can be expressed as follows:

$$I_{D(rms)} = \sqrt{\frac{16 \cdot \sqrt{2} \cdot P_{out}^2}{9 \cdot \pi \cdot V_{acLL} \cdot V_{out} \cdot \eta^2}}$$

The rms current is thus 30% lower (divided by $\sqrt{2}$) when compared to what is obtained in traditional CrM or FCCrM operation.

Similarly, the rms current flowing through the bulk capacitor is also diminished. Assuming a constant load current, we can obtain a good approximation of this current using the following equation:

$$I_{Cout(rms)} = \sqrt{\frac{16 \cdot \sqrt{2} \cdot P_{out}^2}{9 \cdot \pi \cdot V_{acLL} \cdot V_{out} \cdot \eta^2} - \left(\frac{P_{out}}{V_{out}}\right)^2}$$

Whereas, in a traditional CrM or FCCrM PFC, we would have:

$$I_{Cout(rms)} = \sqrt{\frac{32 \cdot \sqrt{2} \cdot P_{out}^2}{9 \cdot \pi \cdot V_{acLL} \cdot V_{out} \cdot \eta^2} - \left(\frac{P_{out}}{V_{out}}\right)^2}$$

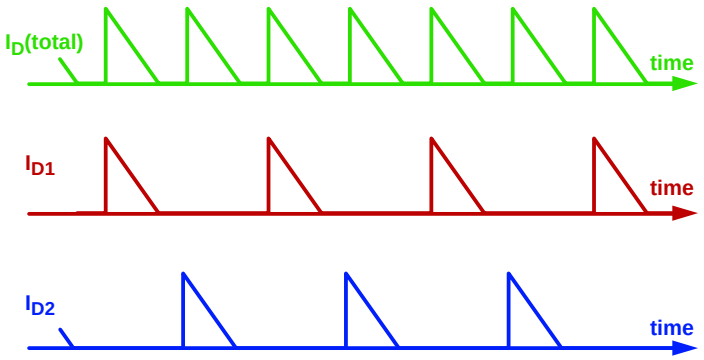

Figure 7−5. Reduction in the AC Content of the Refueling Current as a Result of Interleaving

Design Steps with the 300 W Example

A 300 W interleaved PFC consists of two 150 W parallel CrM (Chapter 3) or FCCrM (Chapter 4) stages. Hence, the main task lies in their dimensioning. As the main steps in designing a CrM or FCCrM PFC boost have already been covered in this handbook, this chapter will mainly focus on the aspects that are specific to interleaving.

Step 1: Define the Key Specifications

Minimum Input voltage (Vac_{LL}): 88 Vac (this is usually 10−12% below the minimum typical voltage which could be 100 Vac in many countries).

Maximum Input voltage (Vac_{HL}): 264 Vac (this is usually 10% above the maximum typical voltage which could be 240 Vac in many countries)

Line frequency (f_{LINE}): 50 Hz/60 Hz (This is often specified in a range of 47−63 Hz and for calculations such as hold-up time, one has to factor in the lowest value specified)

Output Voltage (V_{out}): 390 V (This value has to be above 1.414 • Vac_{HL} and is typically between 385 and 400 V for universal input operation)

Maximum output voltage ($V_{out(max)}$): 415 V (This value is usually 7−10% above the V_{out} value and is determined by the accuracy of the OVP level of the PFC controller).

PFC maximum output power (P_{out}): 300 W (This is the specified output power for the PFC stage. It is important to factor in the follow-on stage efficiency when specifying this parameter − it will always be higher than the specified maximum system output power)

Clamp frequency ($f_{sw(min)}$): 130 kHz per phase leading to a 260-kHz clamp frequency for the interleaved PFC. The clamp frequency is key when dimensioning the boost inductors that must be large enough to force CrM operation in the most severe conditions (full load). The higher $f_{sw(min)}$, the lower the inductance can be.

Output voltage ripple ($V_{ripple(p-p)}$): <27 V (This parameter is often specified in percentage of output voltage, ±3.5% maximum in our case)

Estimated efficiency (η): 94% (This parameter is an initial estimate that is used to size the power stage components − high level of accuracy is not needed for the design procedure).

Step 2: Design the Boost Inductor (for each branch)

As already seen in the CrM and FCCrM sections, the (maximum) peak and rms inductor currents within one branch are:

$$I_{coil,pk(\max)} = \frac{2\sqrt{2}\cdot\left(\frac{P_{out}}{2}\right)}{\eta\cdot Vac_{LL}} = \frac{2\sqrt{2}\cdot 150}{0.94\cdot 88} = 5.13\,A$$

And:

$$I_{coil,rms(\max)} = \frac{I_{coil,pk(\max)}}{\sqrt{6}} \cong \frac{5.13}{\sqrt{6}} \cong 2.09\,A$$

As discussed in chapter 4, the boost inductor design is given by the equation below (where $f_{sw(min)}$ is the clamp frequency):

$$L \geq \frac{\eta\cdot Vac_{LL}{}^2\cdot\left(\frac{V_{out}}{\sqrt{2}}-Vac_{LL}\right)}{\sqrt{2}\cdot V_{out}\cdot\left(\frac{P_{out}}{2}\right)\cdot f_{sw(\min)}} = \frac{0.94\cdot 88^2\cdot\left(\frac{390}{\sqrt{2}}-88\right)}{\sqrt{2}\cdot 390\cdot 150\cdot 130k} \cong 127\ \mu H$$

Finally, a 150-µH / 6-A pk / 2.5-A rms inductor was selected.

Step 3: Design the Power Stage Components

The power stage components are designed based on their current and voltage ratings. The inductor design is already covered in step 2. The bridge diode should be selected based on peak inductor current rating and will have the power dissipation given by:

$$P_{bridge} = \frac{4\sqrt{2}}{\pi}\cdot\frac{V_f}{Vac_{LL}}\cdot\frac{P_{out}}{\eta} \cong 1.8\frac{V_f}{88}\cdot\frac{300}{0.94} \cong 6.5\cdot V_f$$

Assuming a forward voltage of 1 V for each diode ($V_f = 1V$), the bridge approximately dissipates 6.5 W.

For each branch, the MOSFET is selected based on peak voltage stress ($V_{out(max)}$ + margin) and rms current stress:

$$I_{M(rms)} = \frac{2\cdot\left(\frac{P_{out}}{2}\right)}{\sqrt{3}\,\eta\cdot Vac_{LL}}\cdot\sqrt{1-\frac{8\cdot\sqrt{2}\cdot Vac_{LL}}{3\cdot\pi\cdot V_{out}}} = \frac{2\cdot 150}{\sqrt{3}\cdot 0.94\cdot 88}\sqrt{1-\frac{8\cdot\sqrt{2}\cdot 88}{3\cdot\pi\cdot 390}} \cong 1.79\ \text{A}$$

Using a 550-V, 250-mΩ FET, per branch, each MOSFET will give conduction losses of (assuming that $R_{DS(on)}$ increases by 80% due to temperature effects):

$$P_{cond} = I_{M(rms)}{}^2\cdot R_{DS(on)} = 1.79^2\cdot 0.25\cdot 180\% \cong 1.44\ \text{W}$$

One Infineon IPP50R250 MOSFET per branch was used in this design.

Two IPP50R250 placed in parallel would cause the same conduction losses in a conventional CrM or FCCrM PFC stage.

Switching losses are difficult to predict accurately. They are not computed here.

One can simply note that whether a traditional or an interleaved PFC is used, the switching event occurs under the same voltage stress. The only difference is in the current magnitude that is half in one branch of the interleaved PFC compared to that of the conventional PFC. Thus, assuming that the switching times are the same in both cases and remembering that the interleaved PFC consists of two branches:

- If the same MOSFETs are used (one in a traditional PFC, 1 per branch in an interleaved one), the global switching losses would be the same in the two solutions
- In practice, they should be lower in interleaved PFC because of the use of a smaller MOSFET per phase leading to less parasitic capacitance and higher transition speed.

Interleaved PFC requires two boost diodes (one per branch). As explained in the FCCrM chapter, there are no reverse recovery issues to worry about. Simply, they must meet the correct voltage rating ($V_{out(max)}$ + margin) and exhibit a low forward voltage drop. Supposing a perfect current sharing, the average diode current is the half of the load current $\left(I_{d1} = I_{d2} = \frac{I_{d(total)}}{2} = \frac{P_{out}}{2 \cdot V_{out}} \cong 0.38\ A \right)$. So, the losses are just $\left(\frac{I_{d(total)} \cdot V_f}{2} \right)$ per diode. For each phase, the peak current seen by the diode will be the same as the corresponding inductor peak current.

Step 4: Output Capacitor Design

The output capacitor is designed considering 3 factors: output voltage ripple, output current ripple and the hold-up time. The output voltage ripple is given by:

$$V_{ripple(p-p)} = \frac{P_{out} \cdot}{2\pi \cdot f_{line} \cdot C_{out} \cdot V_{out}}$$

The capacitor rms current is given by (assuming a resistive load):

$$I_{Cout(rms)} = \sqrt{\frac{16 \cdot \sqrt{2} \cdot P_{out}^2}{9 \cdot \pi \cdot V_{acLL} \cdot V_{out} \cdot \eta^2} - \left(\frac{P_{out}}{V_{out}} \right)^2}$$

However, almost always, the value of the capacitor is determined by the hold-up time which is approximated by:

$$t_{hold-up} = \frac{C_{out} \cdot (V_{out}^2 - V_{\min}^2)}{2 \cdot P_{out}}$$

The hold-time being not considered here, a 100-μF capacitor was chosen to satisfy the other above conditions. The peak-peak ripple peaks to 24 V_{pp} at full load (50-Hz line) (±3% of V_{out}) and the rms current is 1.34 A.

Step 5: Current Sense Circuit

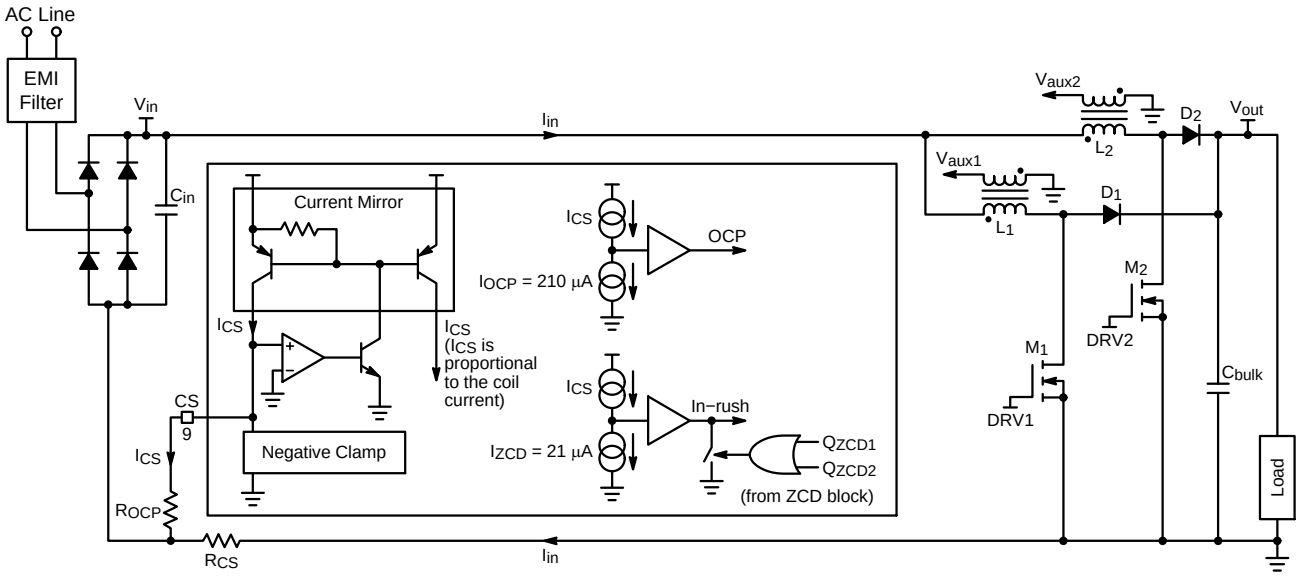

Figure 7−6. Current Sense Block

The NCP1631 is designed to monitor a negative voltage proportional to the inductor current. Practically, a current sense resistor (***R**CS*** of Figure 7−6) is inserted in the return path to generate a negative voltage proportional to the total current absorbed by the two branches. The circuit incorporates an operational amplifier that sources the current necessary to maintain the CS pin voltage null (refer to Figure 7−6). By inserting a resistor ***R**OCP*** between the CS pin and ***R**CS***, we adjust the pin9 current as follows:

$$-\left(R_{CS}\cdot I_{in}\right)+\left(R_{OCP}\cdot I_{CS}\right)=V_{pin9}\cong 0$$

Where ***I**in*** is the total current drawn by the two phases of the interleaved PFC stage.

Finally the current I_{CS} absorbed by pin9 is proportional to the inductor current as shown by the following equation:

$$I_{CS}=I_{pin9}=\frac{R_{CS}}{R_{OCP}}I_{in}$$

The circuit compares ***I**CS*** to an internal 210-μA current reference for a cycle by cycle current limitation. Hence, the Over-Current protection trips when:

$$I_{in,\max}=\frac{R_{OCP}}{R_{CS}}\cdot 210\ \mu A$$

Finally, the ratio (***R**OCP* / *R**CS***) sets the over-current limit in accordance with the following equation:

$$\frac{R_{OCP}}{R_{CS}}=\frac{I_{in,\max}}{210\ \mu A}$$

As we have two external components to set the current limit (***R**OCP*** and ***R**CS***), the current sense resistor can be optimized to have the ***best trade-off between losses and noise immunity***. Following procedure is used to arrive at the trade-off:

Calculate the maximum current drawn by the two branches:

As shown in [2], the following equations give the total current that is absorbed by the interleaved PFC

$$I_{in,\max}=2\sqrt{2}\cdot\frac{\left(P_{in,avg}\right)_{\max}}{\left(V_{in,rms}\right)_{LL}}\cdot\left(1-\frac{V_{out,nom}}{4\cdot\left(V_{out,nom}-\left(\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}\right)\right)}\right)\quad if\ \left(V_{in,rms}\right)_{LL}\le\frac{V_{out,nom}}{2\sqrt{2}}$$

$$I_{in,\max}=2\sqrt{2}\cdot\frac{\left(P_{in,avg}\right)_{\max}}{\left(V_{in,rms}\right)_{LL}}\cdot\left(1-\frac{V_{out,nom}}{4\cdot\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}}\right)\qquad if\ \left(V_{in,rms}\right)_{LL}\ge\frac{V_{out,nom}}{2\sqrt{2}}$$

Where:

- $(V_{in,rms})_{LL}$ is the lowest level of the line rms voltage.
- $(P_{in,avg})_{max}$ is the maximum level of the input power.
- $V_{out,nom}$ is the nominal level of the output voltage (or the output regulation voltage)

In our case, $\left(\left(V_{in,rms}\right)_{LL} = 88 \leq \frac{V_{out,nom}}{2\sqrt{2}} = \frac{390}{2\sqrt{2}} \cong 138 \right)$.

Hence:

$$I_{in,\max} = 2\sqrt{2} \cdot \frac{\left(P_{in,avg}\right)_{\max}}{\left(V_{in,rms}\right)_{LL}} \cdot \left(1 - \frac{V_{out,nom}}{4 \cdot \left(V_{out,nom} - \left(\sqrt{2} \cdot \left(V_{in,rms}\right)_{LL} \right) \right)} \right)$$

Assuming $\left(P_{in,avg}\right)_{\max} = \frac{300}{94\%} \cong 320\ W$ (assuming a 94% minimum efficiency), it comes

$$I_{in,\max} = 2\sqrt{2} \cdot \frac{320}{88} \cdot \left(1 - \frac{390}{4 \cdot \left(390 - \left(\sqrt{2} \cdot 88 \right) \right)} \right) \cong 6.5\ A$$

Selecting R_{OCP} and R_{CS}:

If we neglect the input current ripple, the R_{CS} losses are given by the following simplified equation:

$$p_{R_{CS}} = R_{CS} \cdot \left(\frac{P_{in,avg}}{V_{in,rms}} \right)^2$$

One can choose R_{CS} as a function of its relative impact on the PFC stage efficiency at low line and full power. If α is the relative percentage of the power that can be consumed by R_{CS}, this criterion leads to:

$$\alpha \cdot \left(P_{in,avg}\right)_{\max} = R_{CS} \cdot \left(\frac{\left(P_{in,avg}\right)_{\max}}{\left(V_{in,rms}\right)_{\min}} \right)^2$$

Finally:

$$R_{CS} = \alpha \cdot \frac{\left(V_{in,rms}\right)_{\min}^{\ 2}}{\left(P_{in,avg}\right)_{\max}}$$

And:

$$R_{OCP} = R_{CS} \cdot \frac{I_{in,\max}}{210\ \mu A}$$

Generally ($\alpha = 0.2\%$) gives a good trade-off between losses and noise immunity (0.2% of the power is lost in the R_{CS} at low line). Lower levels can be set when superior efficiency ratios are targeted. In this case, a special attention is to be paid to the PCB layout.

This criterion leads to the following R_{CS} value:

$$R_{CS} = 0.2\% \cdot \frac{88^2}{320} \cong 50\ m\Omega$$

This selection results in the following R_{OCP} resistor:

$$R_{OCP} = 50m \cdot \frac{6.5\ A}{210\ \mu A} \cong 1.54\ k\Omega$$

A 1.8-kΩ resistor is selected for R_{OCP} that gives a 15% margin in the over-current level.

When an over-current event is detected, the NCP1631 decreases the conduction time in both branches as a function of the excess current for a gradual response in case of a moderate over-current and a sharp reaction in a severe situation. This method detailed in the data-sheet [3] avoids risks of discontinuity in the operation because of “normal” transients that would trigger the OCP function.

Application Schematic

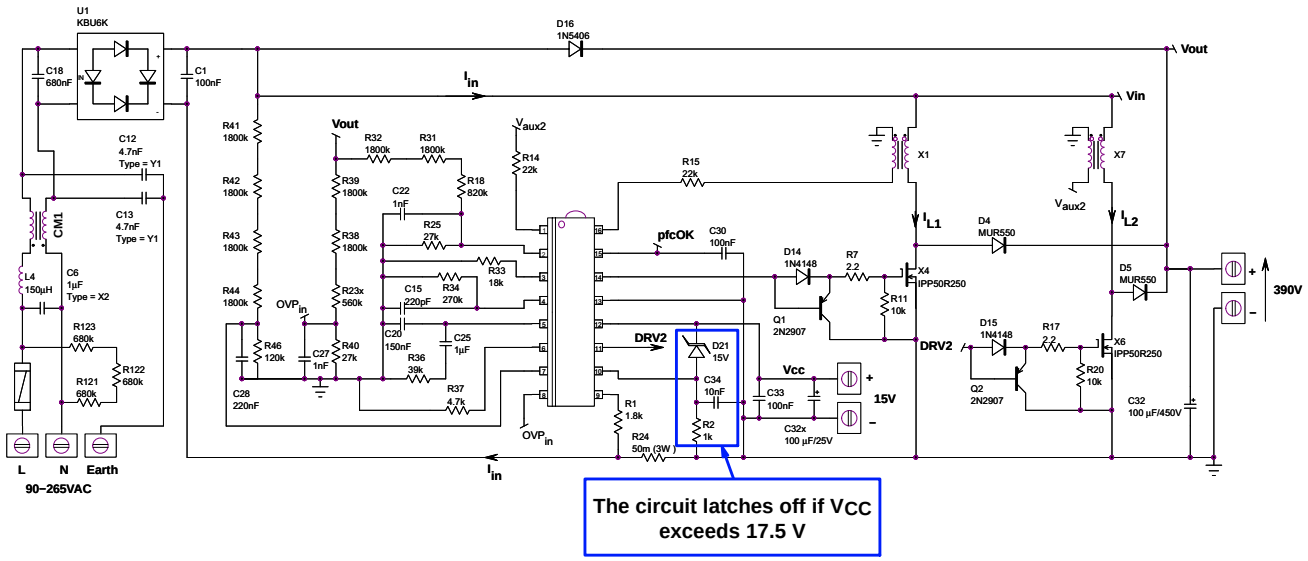

Figure 7−7. Application Schematic

The presented application is that of the NCP1631 demo-board detailed in [4]. It was populated so that it must be fed by a 15-V external power source. However, it is possible to add the elements necessary to have it self-powered: start-up resistors and charge pump.

The boards is equipped with two 150-µH, PQ2620 inductors.

The MOSFETS are IPP50R250 from Infineon.

The boost diodes are axial MUR550 from ON Semiconductor. These Ultra-Fast diodes are specifically designed for CrM or FCCrM PFC.

The latch off capability is highlighted in schematic. Thermal protection could utilize the NCP1631 latch off capability.

Bill of Materials

Table 6−1. Bill of Materials for CCM PFC Circuit Based on the NCP1654

Reference	Qty	Description	Value	Tolerance/ Constraints	Footprint	Manufacturer	Part Number	Substitution Allowed
CM1	1	CM Filter, 4 A	2*6.8 mH	4 A/250 V	Through-hole	EPCOS	B82725-A2402-N1	No
C2	1	Electrolytic Capacitor	100 μF	450 V	Through-hole	BC Components	222.215.937.101	No
C5	1	X2 Capacitor	100 nF	275 V	Through-hole	RIFA	PHE840MB6100MB05R1	No
C6	1	X2 Capacitor	1 μF	275 V	Through-hole	RIFA	PHE840MD7100MD50R0	No
C10, C16	2	Y Capacitor	4.7 nF	275 V	Through-hole	Murata	DE1E3KX472MA5B	No
C15	1	Ceramic Capacitor	220 pF	5%, 50 V	SMD, 1206			Yes
C18	1	X2 Capacitor	680 nF	275 V	Through-hole	EPCOS	B32923A2684M	No
C20	1	Ceramic Capacitor	150 nF	10%, 50 V	SMD, 1206			Yes
C22, C27	2	Ceramic Capacitor	1 nF	10%, 50 V	SMD, 1206			Yes
C25	1	Ceramic Capacitor	1 μF	10%, 50 V	SMD, 1206			Yes
C28	1	Ceramic Capacitor	220 nF	10%, 50 V	SMD, 1206			Yes
C30, C33	2	Ceramic Capacitor	100 nF	10%, 50 V	SMD, 1206			Yes
C32	1	Electrolytic Capacitor	100 μF	25 V	Through-hole			Yes
C34	1	Ceramic Capacitor	100 nF	10%, 50 V	SMD, 1206			Yes
D6, D14, D15	3	Diode	D1N4148		Through-hole	Philips	1N4148	Yes
D3	1	LED 3 mm	2.4 V/2 mA		Through-hole	Vishay	TLLG4400	Yes
D4, D5	2	Boost Diode	MUR550	5 A, 500 V	Axial	ON Semiconductor	MUR550APFG	No
D16	1	Standard Recovery Diode, 600 V	1N5406	3 A, 600 V	Axial	ON Semiconductor	1N5406G	No
D21	1	Zener Diode, 18 V	18 V		Through-hole	NXP	BZX79-C18	No
HS1	1	Heatsink, 2.9°C/W	2.9°C/W			AAVID THERMALLOY	437479	No
L4	1	DM Choke, WI-FI Series	150 μH/5 A	20%, 5 A	Through-hole	Wurth Electronics	7447076	No
Q1, Q2	2	PNP Transistor	2N2907		TO92	ON Semiconductor	P2N2907AG	No
R2, R6	2	Axial Resistor, 1/4 W	1 kΩ	1%	Through-hole			Yes
R1	1	Axial Resistor, 1/4 W	1.8 kΩ	1%	Through-hole			Yes
R7, R17	2	Axial Resistor, 1/4 W	2.2 Ω	1%	Through-hole			Yes
R11, R20	2	SMD Resistor, 1206, 1/4 W	10 kΩ	1%	SMD, 1206			Yes
R14, R15	2	SMD Resistor, 1206, 1/4 W	22 kΩ	1%	SMD, 1206			Yes
R16, R21	2	Axial Resistor, 1/4 W	0 Ω	1%	Through-hole			Yes
R18	1	Axial Resistor, 1/4 W	560 kΩ	1%	Through-hole			Yes
R23	1	Axial Resistor, 1/4 W	820 kΩ	1%	Through-hole			Yes
R24	1	Axial Resistor, 3 W, ±1%	50 mΩ	1%	Through-hole	Vishay	RLP30R050	No
R25, R40	2	SMD Resistor, 1206, 1/4 W	27 kΩ	1%	SMD, 1206			Yes
R31, R32, R38, R39, R41, R42, R43, R44	8	Axial Resistor, 1/4 W	1800 kΩ	1%, 1/4 W	Through-hole			Yes
R33	1	SMD Resistor, 1206, 1/4 W	18 kΩ	1%	SMD, 1206			Yes
R34	1	SMD Resistor, 1206, 1/4 W	270 kΩ	1%	SMD, 1206			Yes
R36	1	SMD Resistor, 1206, 1/4 W	33 kΩ	1%	SMD, 1206			Yes
R37	1	SMD Resistor, 1206, 1/4 W	4.7 kΩ	1%	SMD, 1206			Yes
R45	1	SMD Resistor, 1206, 1/4 W	0 Ω	1%	SMD, 1206			Yes
R46	1	SMD Resistor, 1206, 1/4 W	120 kΩ	1%	SMD, 1206			Yes
R121, R122, R123	3	SMD Resistor, 1206, 1/4 W	680 kΩ	1%	SMD, 1206			Yes
U1	1	Diode Bridge	KBU6K			General Semiconductor	KBU6K	No
U2	1	Interleaved PFC Controller, SOIC-16	NCP1631	−	SO16	ON Semiconductor	NCP1631	No
X1, X5	2	PFC Inductor	150 μH	−		CME	OF9120	No
	2	TO220 Isolators				Bergquist	3223-07FR-43	Yes
	5	Board “legs”				RICHCO	TCBS-801	Yes
F1	1	Fuse	4 A Temporised	250 V		Shurter	34.3123	Yes
X4, X6	2	MOSFET	IPP50R250CP	550 V	TO220	Infineon	IPP50R250CP	No

NOTE: All devices are Pb-Free.

Results and Performance Curves

Evaluation Board Manual [4] details the performance of the presented 300 W interleaved PFC stage.

The main results are however reported here.

Figure 7−8 shows the input current at low and high line. As expected, the input current looks like a CCM one. At high line, the frequency clamp slightly increases the input current ripple.

The bottom waveforms are magnified views. The drive signals are shown to check that the 180° phase shift is properly obtained. At low line (left), the branches operate in CrM. At high line they operate in DCM (right) as attested by the oscillating current near the valley since the frequency clamp is set to 130 kHz at nominal load (at a lower level at light load as dictated by the frequency foldback function to improve the efficiency). It is worth reminding that the NCP1631 like other FCCrM circuits, automatically modulates the MOSFET conduction time to still exhibit near unity power factor in DCM. PF and THD performance are detailed in [4].

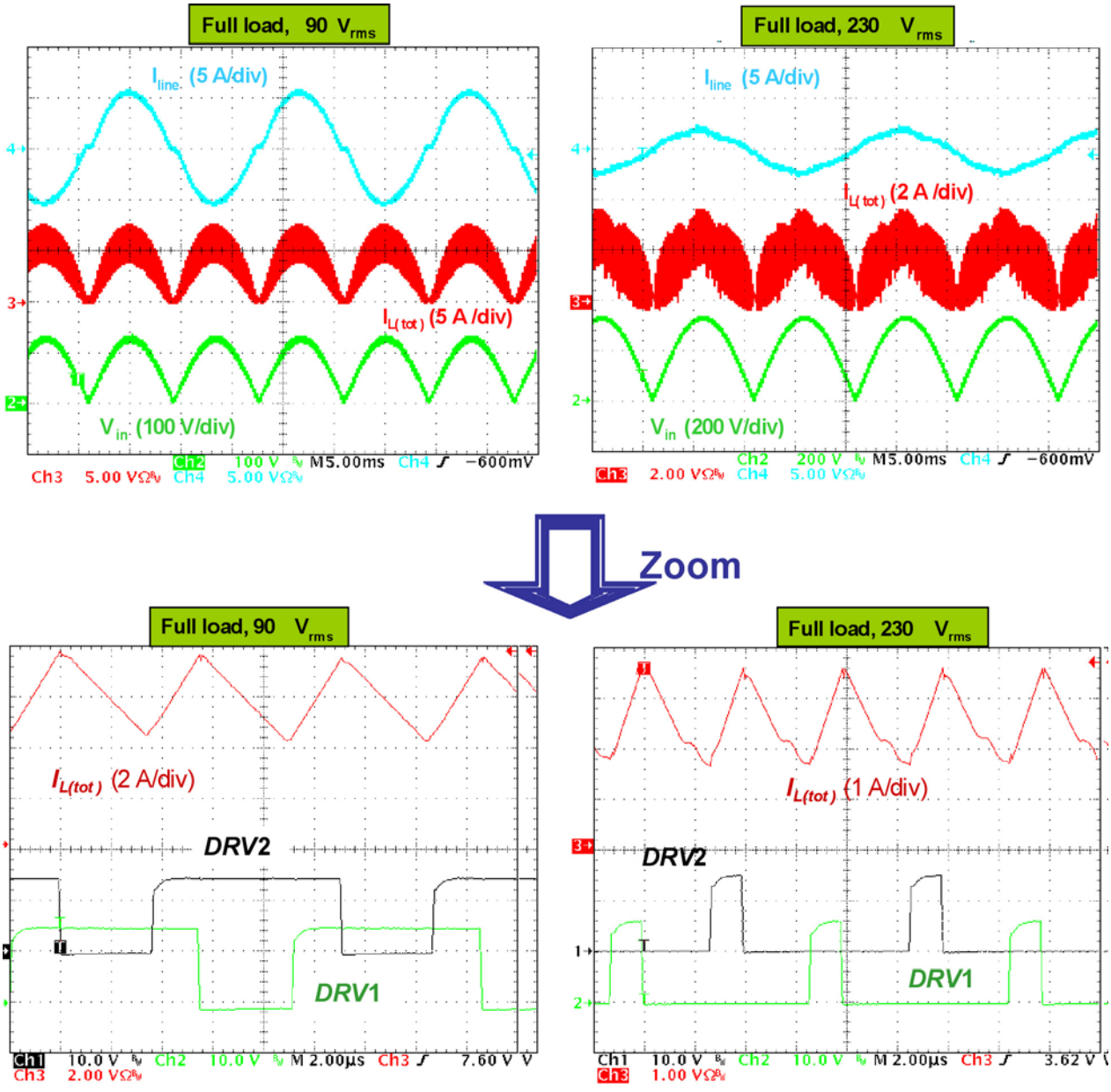

Figure 7−8. Typical Waveforms at Full Load

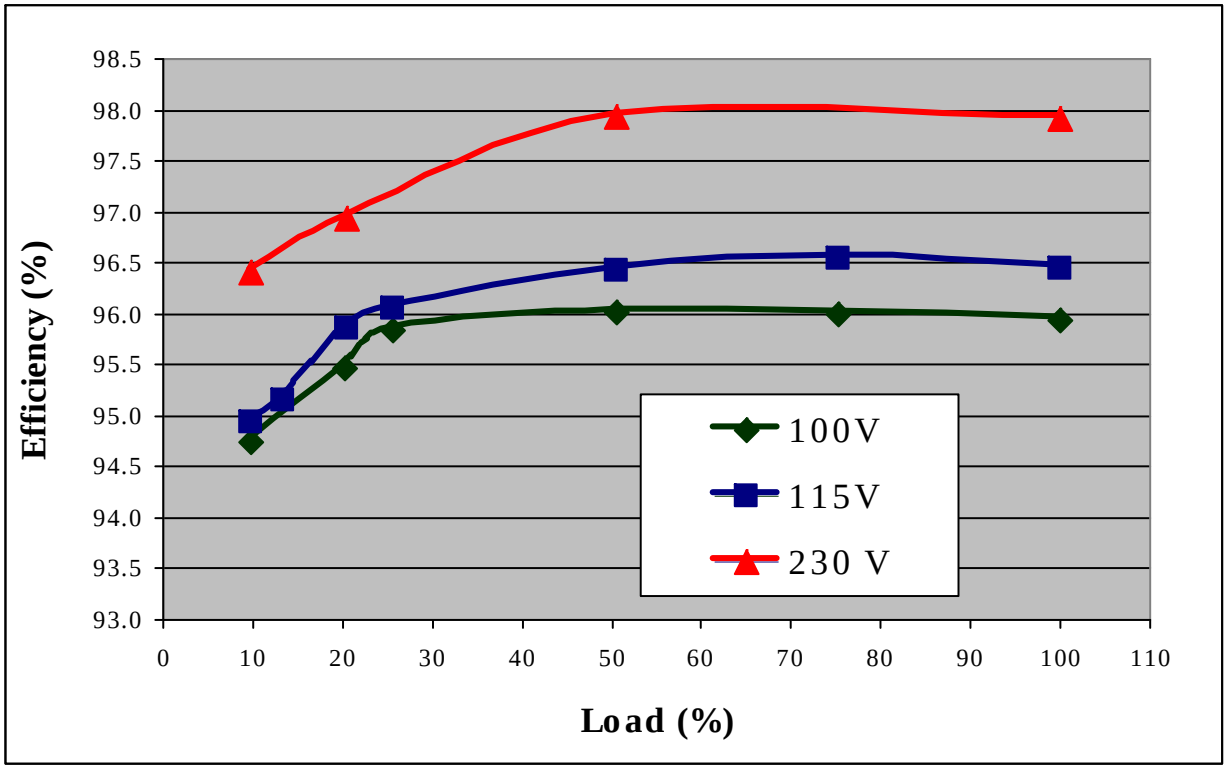

Figure 7−9. Efficiency versus Load

As shown by Figure 7−9, the efficiency characteristic over load is particularly flat.

This is because the interleaved PFC limits the weight of the conduction losses at full load by sharing the stress between two branches. At light-load, the frequency clamp and the frequency fold-back functions mitigate the switching losses and hence, effectively limit the efficiency decay usually observed at light load.

These efficiency performances were obtained using the typical frequency fold-back characteristic. When superior light-load efficiency ratios are required, the frequency fold-back can be tweaked. For instance, application note AND8456/D [5] teaches how to abruptly drop the switching frequency by adding a simple resistor, when the power goes below a programmed level. Figure 7−10 shows that such a technique can further improve the efficiency at 10% and 20% of the load by forcing a 20-kHz operation at these power levels. The PFC stage keeps running in CrM at 50% and 100% of the load as necessary for an efficient operation.

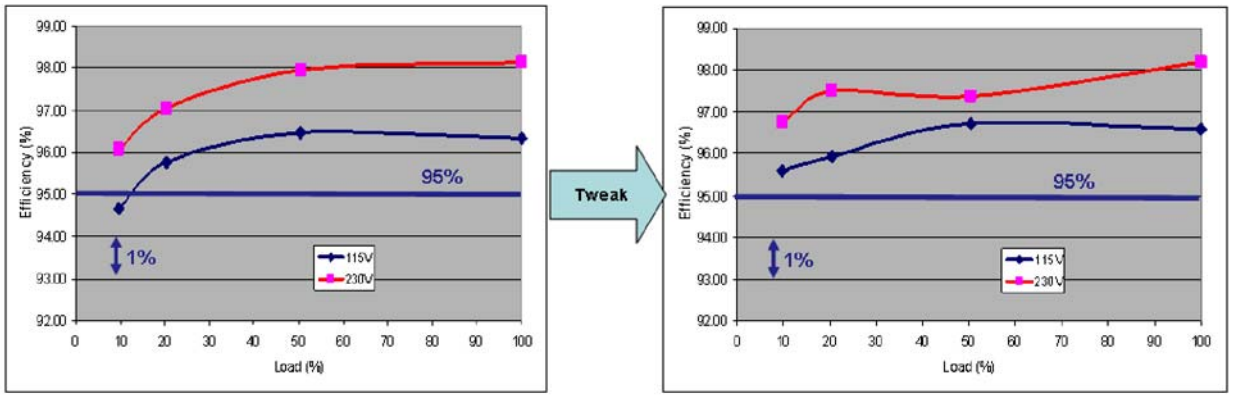

Figure 7−10. Tweaking the Frequency Fold-back Characteristic can Help Improve the Light-load Efficiency

References

[1] L. Huber, B. T. Irving and M. M. Jovanovic, “Open-Loop Control Methods for Interleaved DCM/CCM Boundary Boost PFC Converters”, IEEE trans. Power Electron., vol. 23, no. 4, pp 1649−1657, July 2008
[2] Joel Turchi, “Characteristics of Interleaved PFC Stages”, Application note AND8355/D, http://www.onsemi.com/pub_link/Collateral/AND8355-D.PDF
[3] NCP1631 datasheet, http://www.onsemi.com/pub_link/Collateral/NCP1631-D.PDF
[4] Stéphanie Conseil, “Performance of a 300 W Interleaved PFC Driven by the NCP1631”, Evaluation Board Manual, NCP1631EVB/D, http://www.onsemi.com/pub_link/Collateral/NCP1631EVB-D.PDF
[5] Joel Turchi, “Further Improve the Low-Power Efficiency of Your NCP1631-Driven Interleaved PFC”, Application note AND8456/D, http://www.onsemi.com/pub_link/Collateral/AND8456-D.PDF

CHAPTER 8

Bridgeless PFC

Introduction

The need for higher efficiencies from the PFC stage has led the circuit designers to look closely at all sections of the circuit and develop possible lower loss alternatives. One section that contributes significantly to the losses is the input bridge rectifier. As a result, the alternatives to eliminate the diode bridge or convert it into a dual-use circuit have been explored for many years. This elimination/conversion of diode bridge brings about its own set of challenges. This chapter provides a more in-depth look at the bridgeless techniques and works through a design example for an 800 W bridgeless PFC converter.

Why Remove the Bridge?

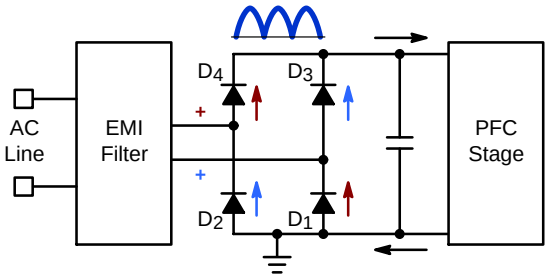

Figure 8−1. The Input Current Flows Through Two Diodes

Figure 8−1 portrays the diode bridge that is usually inserted between the EMI filter and the PFC stage. This bridge rectifies the line voltage to feed the PFC stage with a rectified sinusoid input voltage. It is well known that as a result of this structure, the input current must flow through two diodes before being processed by the PFC boost stage:

- For one line half-wave, **D1** and **D4** conduct (**red** arrows of Figure 8−1)
- For the other one, **D2** and **D3** convey the current (**blue** arrows of Figure 8−1)

As a matter of fact, two diodes of the bridge are permanently inserted in the current path. Unfortunately, these components exhibit a forward voltage that leads to conduction losses.

The mean value of the current seen by the bridge is the line current averaged over one half-line cycle. Hence we can write the following equation:

$$\left\langle I_{bridge} \right\rangle_{\frac{T_{line}}{2}} = \left\langle I_{in}(t) \right\rangle_{\frac{T_{line}}{2}} = \frac{2\sqrt{2}}{\pi} \cdot I_{in(rms)}$$

The line rms current can be easily expressed as a function of the power and of the line voltage:

$$I_{in(rms)} = \frac{P_{out}}{\eta \cdot V_{in(rms)}}$$

Where:

- P_{out} is the output power
- η is the efficiency
- $V_{in(rms)}$ is the rms line voltage

Since two diodes permanently see the average input current, the bridge consumes a power that can be computed as follows:

$$P_{bridge} = 2 \cdot V_f \cdot \left\langle I_{bridge} \right\rangle_{\frac{T_{line}}{2}} \cong 2 \cdot V_f \cdot \frac{2\sqrt{2} \cdot P_{out}}{\eta \cdot \pi \cdot V_{in(rms)}}$$

Finally, if we assume a 1-V forward voltage per diode and computing the losses at the usual low line rms voltage (90 V), it comes:

$$P_{bridge} \cong 2 \cdot 1 \cdot \frac{2\sqrt{2} \cdot P_{out}}{\eta \cdot \pi \cdot 90} \cong 2\% \cdot \frac{P_{out}}{\eta}$$

In other words, an input bridge consumes about 2% of the input power at low line of a wide mains application. Hence, if one of the series diodes could be suppressed, 1% of the input power could be saved and the efficiency could for instance, rise from 94% to 95%. Also, the major hot spot produced by a traditional diode bridge would be eliminated with the benefit of an improved reliability of the application.

“Basic” Bridgeless Architecture

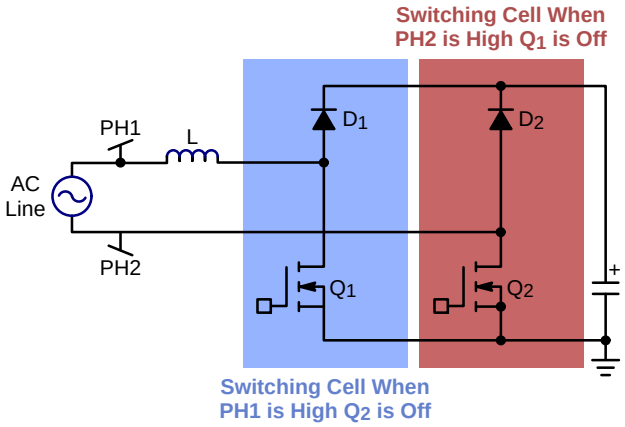

Figure 8−2. “Traditional” Bridgeless Solution

Figure 8−2 portrays a classical option for bridgeless PFC. There are two switching cells. Each of them consists of a power MOSFET and of a diode:

- The first cell (***Q*****1**, ***D*****1**) processes the power for the half-line cycle when the terminal “PH1” of the line is high and is in idle mode for the rest of the line period.
- The second cell (***Q*****2**, ***D*****2**) is active for the other half-wave when “PH1” is low compared to terminal “PH2”.

The line and the PFC inductor are placed in series and the arrangement they form is connected to the switching nodes of the two switching cells. The input current is processed by the switching cell that is active for the considered line half-wave. The MOSFET of the inactive cell has a role anyway, since its body diode serves as the current return path. Compared to a conventional PFC stage, the losses due to the bridge are saved but the body diode of the inactive MOSFET conducts the coil current. Finally, this structure eliminates the voltage drop of one diode in the line-current path for an improved efficiency.

However, the above architecture presents the following inconveniences, resulting from the fact that the line is floating with respect to the PFC stage ground (as opposed to the conventional PFC, where the line is connected to PFC ground):

- Certain PFC controllers need to sense the input voltage. In this structure, a simple circuitry cannot do the job.
- Similarly, the coil current cannot be easily monitored.

Besides these difficulties in the circuit implementation, EMI filtering is the main issue. When “PH1” is high, the negative terminal “PH2” is attached to ground by the ***Q*****2** body diode. Hence, the application ground is connected to ac line as it happens in a conventional PFC. Now, when “PH2” is high, the MOSFET ***Q*****2** switches and the voltage between the line terminals and the application ground pulses as well. More specifically, the potential of the “PH2” node nearly oscillates between 0 (when the MOSFET is on) and the PFC output voltage (when the MOSFET is off). This large “dV/dt” leads to an increased common-mode noise that is difficult to filter. This is probably the major drawback of the above solution ([1] and [2]).

Two-Phase Approach

Figure 8−3 portrays another option for bridgeless PFC. This solution was proposed by Professors Alexandre Ferrari de Souza and Ivo Barbi [3]. As shown in Figure 8−3, there is no full bridge. Instead, the ground of the PFC circuit is linked to the line

by diodes $\boldsymbol{D_1}$ and $\boldsymbol{D_2}$ and each terminal feeds a PFC stage. Hence, the solution could be viewed as 2-phase PFC where the two branches operate in parallel:

- For the half-wave when the terminal “PH1” of the line is high, diode D_1 is off and D_2 connects the PFC ground to the negative line terminal (“PH2”). D_2 grounds the input of the “PH2 PFC stage” branch that thus, is inactive and the “PH1 PFC stage” processes the power.
- For the second half-line cycle (when “PH2” is high), the “PH2 PFC stage” branch is operating and “PH1 PFC stage” that has no input voltage, is inactive.

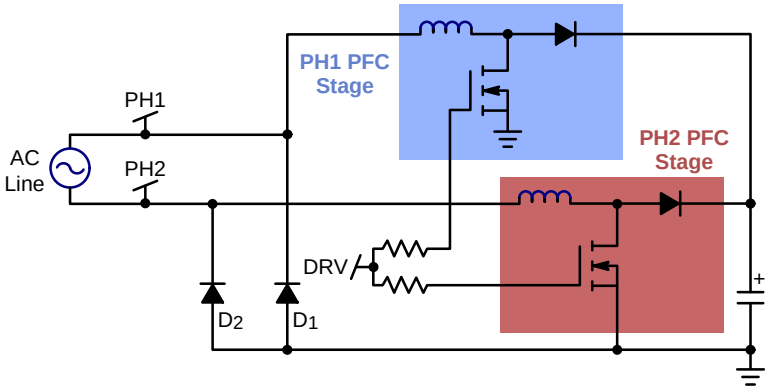

Figure 8−3. Two-Phase Architecture

Figure 8−4 gives an equivalent schematic for the two half-waves. Similarly to the traditional bridgeless structure presented in the previous paragraph, this architecture eliminates one diode in the current path and hence improves the efficiency.

One other interesting characteristic of this structure is that the PFC stage that is active, behaves as a conventional PFC boost would do:

- When the “PH1” terminal is positive (see Figure 8−4a), diode $\boldsymbol{D_1}$ opens and $\boldsymbol{D_2}$ offers the return path. The input voltage for the “PH1” PFC stage is a rectified sinusoid referenced to ground.
- For the other half-wave (see Figure 8−4b), when “PH2” is the positive terminal, $\boldsymbol{D_1}$ offers the return path. Diode $\boldsymbol{D_2}$ is off and sees a rectified sinusoid that inputs the “PH2” PFC stage. Again, we have a conventional PFC where the input voltage and the boost are traditionally referenced to ground.

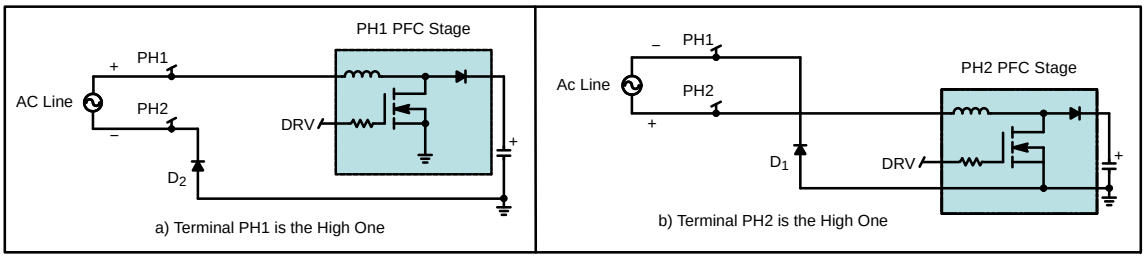

Figure 8−4. Equivalent Schematic for the Two Half−Waves

It is also worth noting that the two-phase structure does not require any specific control scheme to switch between the phases. The MOSFETs of the two branches are referenced to ground and they can be permanently driven even when their phase is in idle mode. The MOSFET of the inactive branch would then be turned on and off with no function, but:

- At the benefit of a simplified circuitry since there is no need for detecting the active phase and for directing the drive signal to the right MOSFET according to the half-line cycle.
- At the price of the additional losses due to the inactive MOSFET drive. The loss is not very high anyway since the voltage across the MOSFET is null when its input voltage is zero. Hence, the gate charge to be provided is approximately halved compared to that of the active MOSFET.

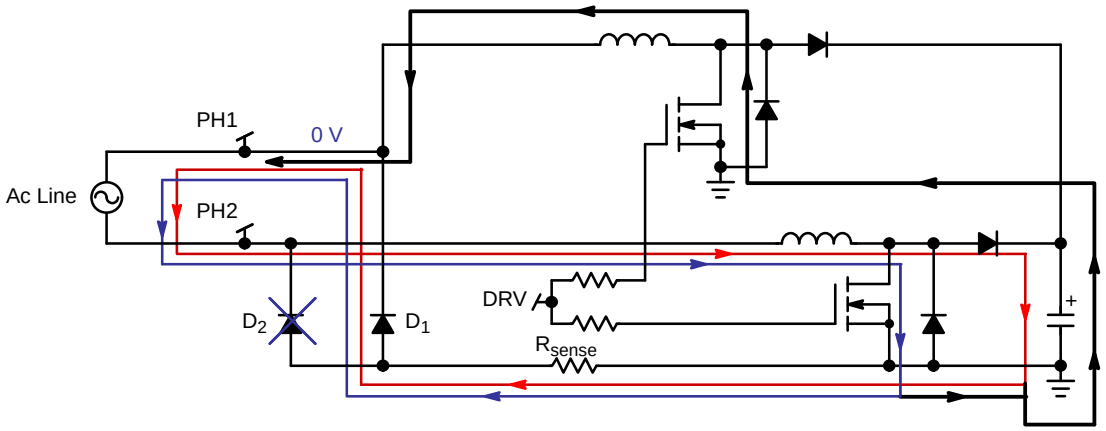

Figure 8−5. Operation for the "PH2" Half-Wave

One should however note that the current does not necessary return by the D_1 and D_2 diodes only. Figure 8−5 portrays (in blue and red) the "expected" current path when "PH2" is high (the same analysis could have been done for "PH1" high):

- The blue path is supposed to be the current path when the MOSFET is on
- The red one, that of the current when the MOSFET is open.

Actually, a large portion of the current flows as indicated in black irrespective of the MOSFET state. This is because the body diode of the supposedly inactive MOSFET provides the current with another path. Since the coil presents low impedance at the line frequency, we have two diodes in parallel and the current is shared between them in inverse proportion of actual impedance of the paths.

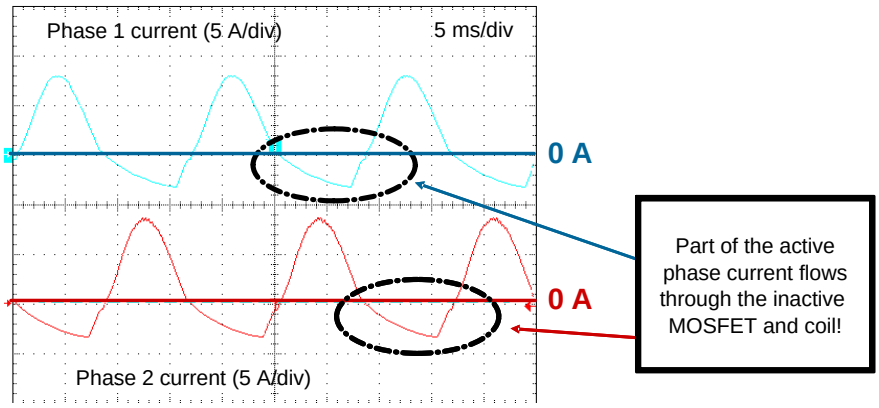

Figure 8−6. Part of the Current Flows through the Supposedly Inactive MOSFET and Coil

Figure 8−6 portrays the input current for each branch. One can see on this plot that a negative current takes place through the body diode during the "inactive" half-wave. The main inconvenience of this behavior is that the input current cannot be sensed by inserting a R_{SENSE} resistor in the supposed return path (as shown by Figure 8−5) since part of the current takes another route. A better alternative is to insert current sense transformers as detailed in the "step 6" part of the next section.

Design Procedure with an 800 W Example

The step-by-step procedure of an 800 W bridgeless PFC is described in this section with reference to Figure 8−7, which highlights the main parts of the design.

Step 1: Key Specifications

Minimum Input voltage (Vac_{LL}): 88 Vac

Maximum Input voltage (Vac_{HL}): 264 Vac

Line frequency (f_{LINE}): 50 Hz/60 Hz (47−63 Hz)

Output Voltage (V_{out}): 385 V

Maximum output voltage ($V_{out(max)}$): 420 V
PFC maximum output power (P_{out}): 800 W
Switching frequency (f_{sw}): 100 kHz
Output voltage ripple ($V_{ripple(p-p)}$): 15 V
Hold-up time ($t_{hold-up}$): 16 ms (330 V being the permissible minimal level at the end of the hold-up time)
Estimated efficiency (η): 95%.

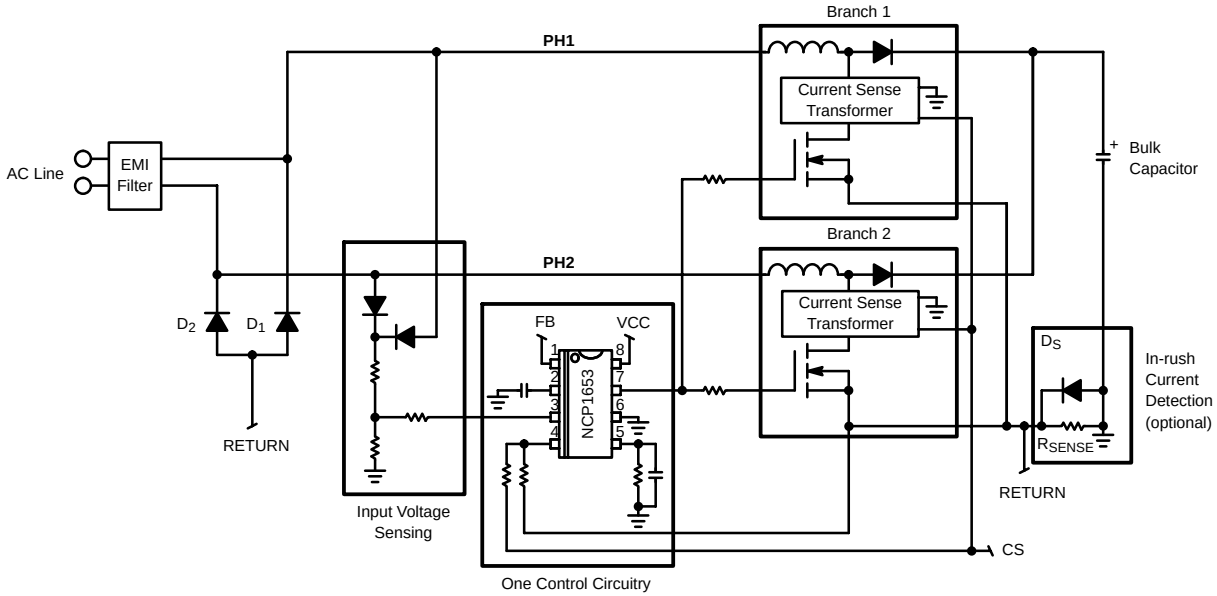

Figure 8−7. Simplified Application Schematic of Bridgeless Converter

Step 2: Power Components for each PFC Branch

Each PFC branch (branch 1 and branch 2) is designed to handle full power for half the line cycle. Hence, the design of components (power FET, boost inductor and boost diode) follows the methodology described in Chapter 6 for CCM operation. However, the fact that each branch is active for one half-line cycle only, improves the heating distribution. Also, the rms current being halved in each branch, the power components does not need to be as large as those of a conventional PFC. Resultant choices for each branch are:

- Boost diodes (1 per branch): CSD10060 (10-A, 600-V SiC diode from CREE)
- Power MOSFETs (2 per branch): SPP20N60 from Infineon (20-A, 600-V, 0.19-Ω)
- Inductors (1 per branch): 200-μH / 9.7 A_{rms} / 16-A_{pk} / 5 A_{pp} coil (ferrite core)
  Part Name: PFC−Choke LDU80025
  Part Number: 203860 (J−Lasslop)

Step 3: Bulk Capacitor Selection

The PFC bulk capacitor is common to both branches as shown in Figure 8−7. Its selection follows the common methodology based on the 3 factors: Output voltage ripple, output current ripple and hold-up time. These three factors have to be computed as it would be computed in a conventional CCM PFC. Two 330-μF, 450-V capacitors are used considering these factors.

Step 4: Input Voltage Sensing:

The input voltage needs to be sensed by the PFC controller for feed-forward (NCP1653, NCP1654) and for brown-out protection (NCP1654). As shown by Figure 8−7, two diodes are used that re-construct the rectified line voltage from the two branches that can then be monitored by the circuit. Our prototype is driven by the NCP1653. As detailed in [4], the input voltage sensing network is to be designed so that it feeds pin3 with a 15-μA dc current at low line. If the NCP1654 is used, the ripple of the voltage applied to the brown-out pin must be adjusted to program the desired line brown-out levels as shown in [5].

Step 5: Current Sense Circuit and Inrush detection

As described in the previous section, a simple current sense resistor cannot sense the MOSFET current. Thus, the MOSFETs current has to be monitored using current sense transformers. Here, two current sense transformers are used (one in series with each FET branch). The chosen current sense transformer is rated for 20 A and has 50:1 turns ratio (WCM 601-2). The current delivered by the boost diodes must also be sensed to provide the controller with a signal representative of the total current flowing through the coils. This can be done with the help of a third current sense transformer.

In our designs, however, another option is chosen in order to detect inrush current. A current sense resistor is inserted in the bulk capacitor return path that monitors the current that re-fuels the bulk capacitor, i.e.:

- in-rush currents during the start-up phase or in over-load situations
- the current provided by the boost diodes in normal operation

Due to that, the MOSFET and the input bridge are referenced to the “RETURN” potential instead of ground. The voltage between the RETURN and ground potentials is the negative voltage developed across the $\boldsymbol{R_{SENSE}}$ resistor. If this voltage becomes too large (during in-rush sequences for instance), the MOSFETs’ source potential may dramatically drop and some accidental MOSFET turn on may follow. That is why the voltage across the $\boldsymbol{R_{SENSE}}$ resistor is limited by a diode.

This diode must be able to sustain the in-rush current and its forward voltage must be high enough so that the $\boldsymbol{R_{SENSE}}$ voltage is not clamped until the current largely exceeds its permissible level in normal operation. Otherwise, the clamping diode would prevent the $\boldsymbol{R_{SENSE}}$ voltage from becoming high enough to trigger the over-current protection.

The secondary of the two current sense transformers and the $\boldsymbol{R_{SENSE}}$ voltage are combined to provide the circuit with a current proportional to the input current for over-current limitation and duty-cycle control.

Figure 8−8 summarizes the current sensing circuitry:

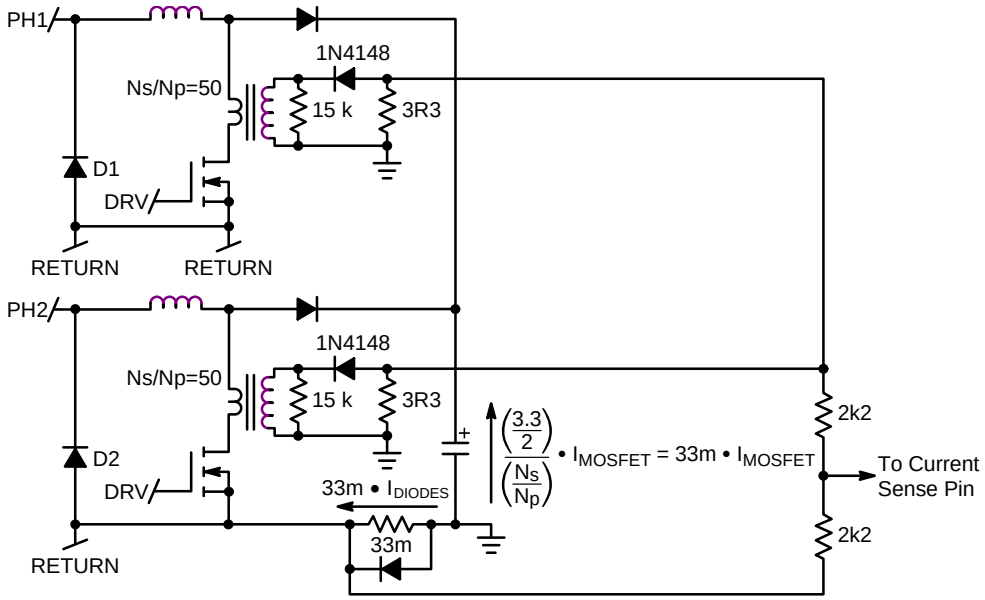

Figure 8−8. Details of the Current Sense Circuits

In our configuration, the current sense transformers and the current sense resistor provide a voltage that in both cases is linked to the sensed current by the same coefficient ($33 \bullet 10^{-3}$). That is why $\boldsymbol{R_4}$ and $\boldsymbol{R_{24}}$ of the detailed circuit schematics in Figure 8−10 on page 103 have the same value. $\boldsymbol{R_4}$ and $\boldsymbol{R_{24}}$ adjust the current sourced by the circuit to maintain the current sense pin to zero. This current is proportional to the sensed current. If the current sense transformer and the current sense resistor had different coefficients, $\boldsymbol{R_4}$ and $\boldsymbol{R_{24}}$ would have to be adapted so that the same current leads to the same current sunk from the controller current sense pin, this absorbed current having to reach 200 μA when the maximum input current is exceeded.

Step 6: Control Circuitry

As already mentioned, the two-phase bridgeless PFC does not require any complex control circuitry. A single NCP1653 PFC controller directly drives the two branches. The NCP1653 is a compact 8-pin PFC controller that operates in continuous conduction mode. As it directly adjusts the conduction time as a function of the coil current, there is no inner current loop to be compensated for an eased design. Alternatively, NCP1654, a derivative of NCP1653 with additional features such as brown-out protection and better line regulation can be used (see [4] and [5]).

Results and Performance Curves

Figure 8−9 shows the annotated picture of the 800 W prototype.

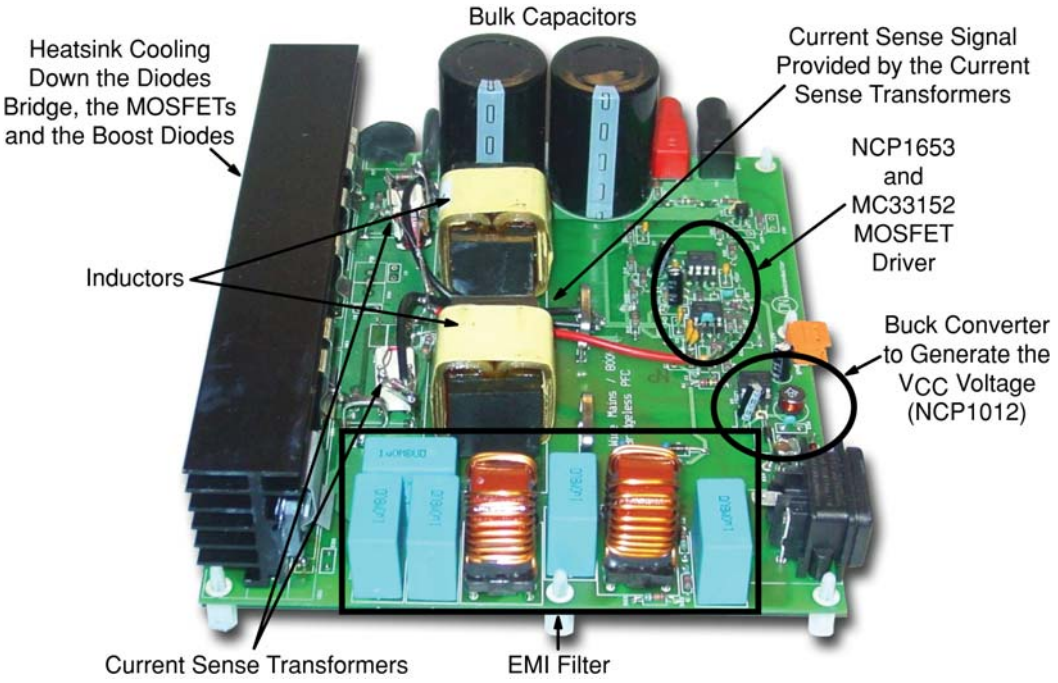

Figure 8−9. Photograph of the Evaluation Board

Circuit Schematics

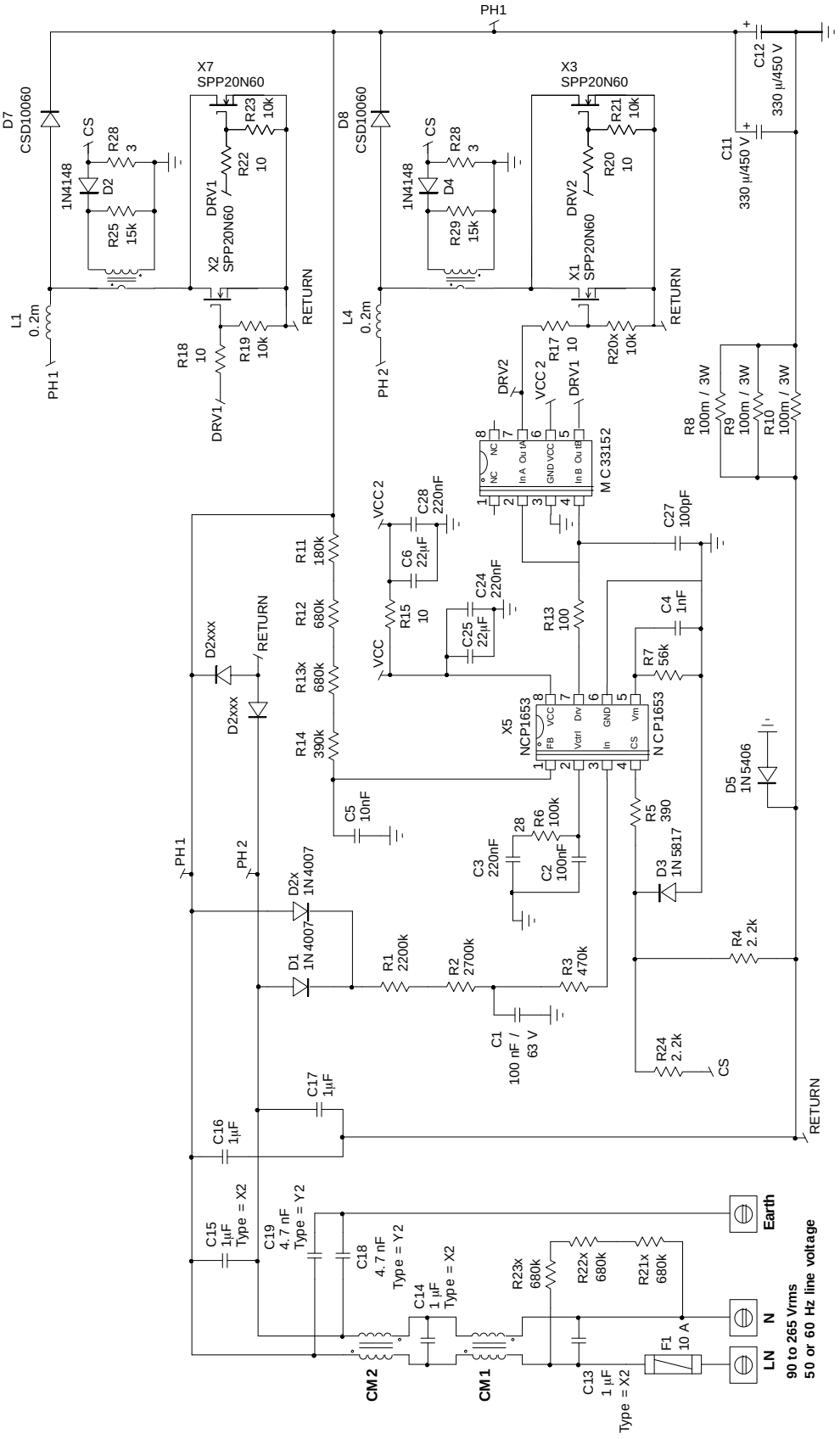

Figure 8−10. Application Schematic

The performance of the board is captured in following waveforms and graphs. Figure 8−11 shows the typical waveforms (line current, output voltage, current sense signal and rectified input voltage) for one branch at two line voltage conditions.

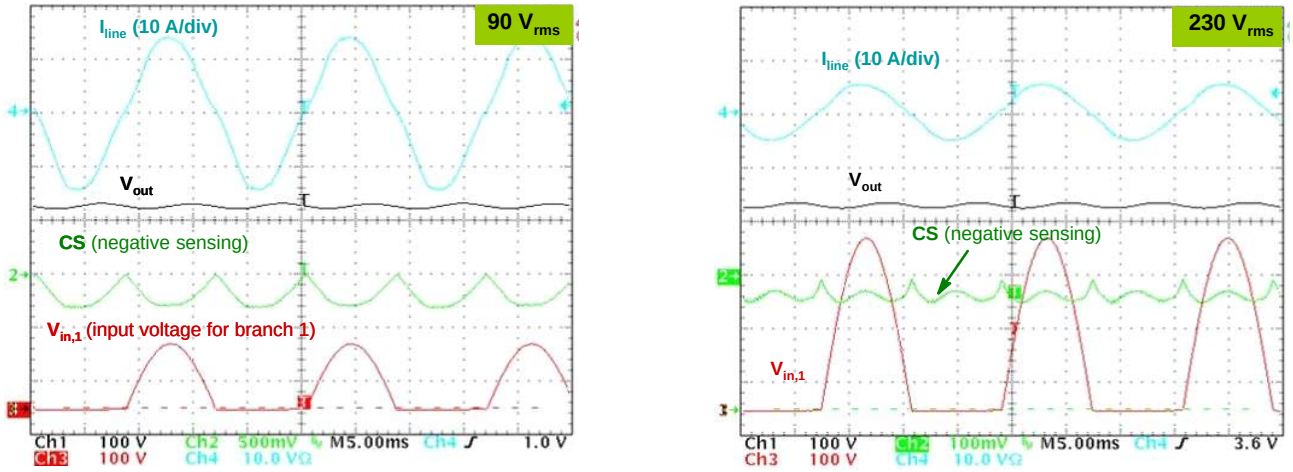

Figure 8−11. Typical Waveforms at Low Line (Left) and High Line (Right)

Plots of Figure 8−11 portray typical waveforms at full load (I_{out} = 2.1 A). “CS” is the negative voltage provided by the current sense transformers. It is representative of the current flowing into the MOSFETs of the two branches (“CS” is the common output of the two current sense transformers). As expected, the input voltage of the “PH1 PFC stage” (“$V_{in,1}$”) is a rectified sinusoid for one half-line cycle and null for the other one. The line current is properly shaped.

Figure 8−12 provides a magnified view at the top of the line sinusoid. The switching frequency is 100 kHz. The signal “V_{sense}” (identical to “CS”) is a negative representation of the MOSFET current. The current sense transformers are wired so that only the current drawn by the MOSFET drain is monitored (possible current flowing in the opposite direction cannot be sensed).

The waveforms are similar to those of a traditional CCM PFC.

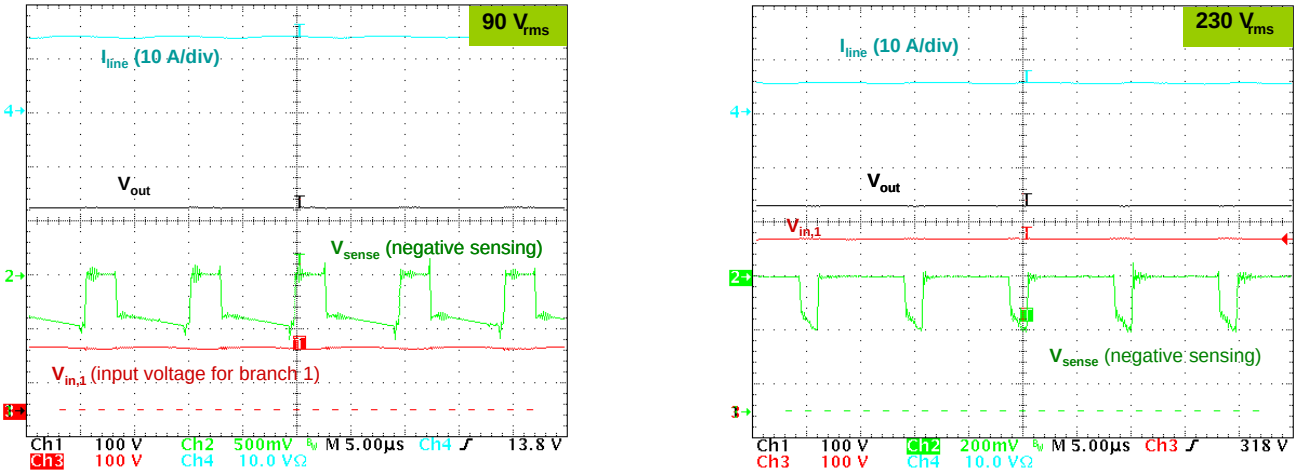

Figure 8−12. Magnified Views of Figure 8−11 Plots

Thermal Measurements

The following results were obtained using a thermal camera, after a 1/2 hour operation. The board was operating at a 25°C ambient temperature, without fan. These data are indicative.

For the bridge, the MOSFETs and diodes, the measurements were actually made on the heat-sink as near as possible to the components of interest.

Measurement Conditions:

$V_{in(rms)}$ = 88 V	I_{out} = 2 A
$P_{in(avg))}$ = 814 W	PF = 0.995
V_{out} = 381 V	THD = 9%

Devices	Bridge	MOSFET1	Diode1	Coil1	MOSFET2	Diode2	Coil2	Bulk Capacitor	CM EMI coil
Temperature (°C)	85	95	77	47	86	80	48	40	45

Efficiency and Total Harmonic Distortion

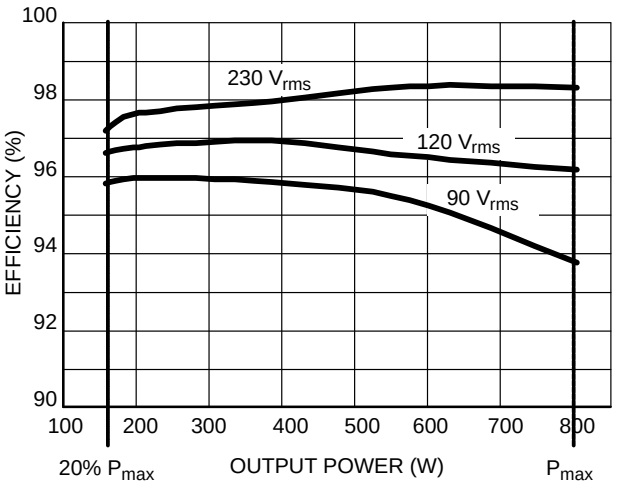

Figure 8−13. Efficiency Performance

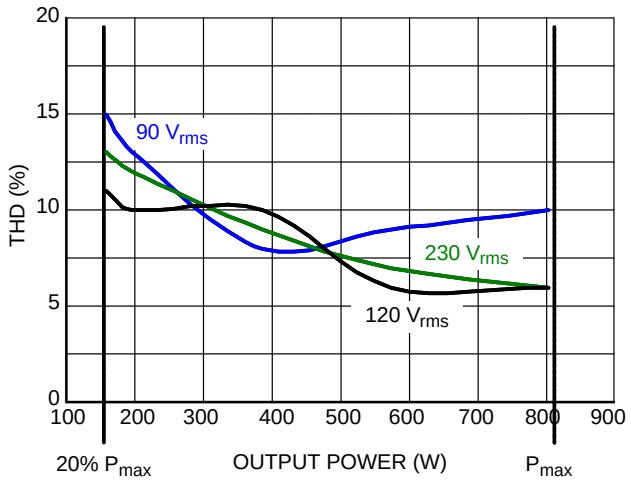

Figure 8−14. Total Harmonic Distortion Over the Load Range

Figure 8−13 portrays the efficiency over the line range, from 20% to 100% of the load.

The efficiency was measured under following conditions:

- The measurements were made after the board was operated at full load, low line for 30 minutes
- All the measurements were made consecutively without interruptions
- PF, THD, $I_{in(rms)}$ were measured by a power meter PM1200
- $V_{in(rms)}$ was measured directly at the input of the board by a HP 34401A multi-meter
- V_{out} was measured by a HP 34401A multi-meter
- The input power was computed according to: $P_{in(avg)} = V_{in(rms)} \cdot I_{in(rms)} \cdot PF$
- Open frame, ambient temperature, no fan

Reviewing Figure 8−13, it can be noted that:

- Like in a conventional PFC, the efficiency is higher at high line.
- At low line (90 V_{rms}), full load, the efficiency is in the range of 94% without a fan. When measured @ 100 V_{rms} input, full load efficiency of 95% was recorded.
- The light load efficiency is very good. For instance, at 20% of full load, efficiency is in the range of or higher than 96%. One of the reasons for this lies in the fact that a bridgeless PFC requires relatively low Qg MOSFETs compared to a conventional PFC for the same efficiency target at full load.

Figure 8−14 portrays the THD at 90, 120 and 230 V_{rms} over the load. One can note that the total harmonic distortion remains very low even in high line, light load (<15%) where the line current is small and more sensitive to all the sources of distortion like the system inaccuracies and mainly the EMI filter.

Conclusion

A bridgeless PFC based on the two-phase architecture has several merits among which one can list the ease of control or the absence of high frequency noise injected to the line (eased EMI). In this chapter, the basics of the bridgeless architecture along with a summary design procedure are covered. The designed prototype has been tested at full load (800 W output) without a fan (open frame, ambient temperature). In these conditions, the full-load efficiency was measured in the range of 94% at 90 V_{rms} and as high as 95% at 100 V_{rms}. The THD remains very low. A NCP1653 or NCP1654-driven two-phase bridgeless PFC is a solution of choice for very efficient, high power applications.

It should be noted that when traditional topologies (CCM/CrM/FCCrM boost) are scaled up to high power levels such as 800 W, they encounter several design challenges related to component size and dissipation. Hence, topologies such as two-phase bridgeless or interleaved, which spread the heat dissipation and offer other benefits, make a lot of sense. Further information on bridgeless PFC can be found in AND8392 [7] from ON Semiconductor.

Please note that a 300 W bridgeless PFC has been recently experimented. An application note is available on the ON Semiconductor website that details this application [9].

References

[1] Laszlo Huber, Yungtaek Jang and Milan M. Jovanovic, “Performance Evaluation of Bridgeless PFC Boost Rectifiers”, APEC 2007
[2] Pengju Kong, Shuo Wang, and Fred C. Lee, “Common Mode EMI Noise Suppression for Bridgeless PFC Converters”
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[4] Joel Turchi, “Four Key Steps to Design a Continuous Conduction Mode PFC Stage Using the NCP1653”, AND81842/D, ON Semiconductor, http://www.onsemi.com/pub/Collateral/AND8184-D.PDF
[5] Patrick Wang, “Four Key Steps to Design a Continuous Conduction Mode PFC Stage Using the NCP1654”, AND8322/D, ON Semiconductor, http://www.onsemi.com/pub/Collateral/AND8322-D.PDF
[6] NCP1653 data sheet and application notes, www.onsemi.com
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[9] Joel Turchi, “A High-Efficiency, 300 W Bridgeless PFC Stage”, AND8481/D, ON Semiconductor, http://www.onsemi.com/pub/Collateral/AND8481-D.PDF

CHAPTER 9

Single Stage, Isolated Power Factor Correction

Introduction

Applications that require an isolated, regulated output voltage or current along with input power factor correction typically involve a two stage conversion process as depicted in Figure 9−1. This scheme is composed of an input boost or bridge-less power factor corrector stage which converts and pre-regulates the input line into a nominal 400 Vdc bus. This bus then provides the input voltage for a conventional dc-to-dc converter which can be any appropriate topology. For lower power applications of 100 W and less, a flyback converter is commonly used.

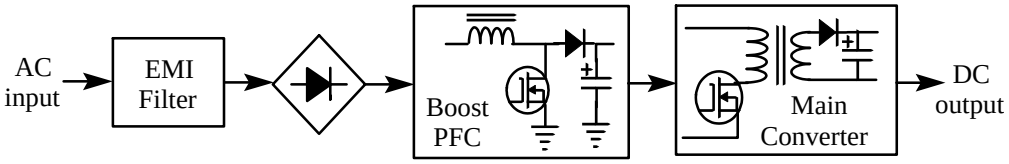

Figure 9−1. Conventional Two-Stage Conversion

With a few performance compromises, a simpler technique to develop an isolated regulated dc output voltage or current can be implemented in which the power factor corrector and main converter sections are merged into a single conversion, The advantage of this approach is reduced parts count and the potential to improve efficiency and power density in lower power applications. The block diagram is shown in Figure 9−2.

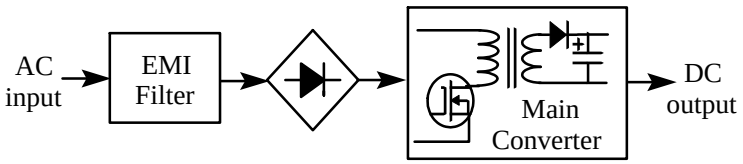

Figure 9−2. Single Stage Conversion with NCP1652

In this single stage PFC converter, the most useful power circuit is the flyback topology or an equivalent buck-boost derivation. The flyback stage not only handles the output voltage regulation and input to output isolation functions, but can provide power factor correction as well. The circuit essentially functions as a conventional boost PFC converter with the output being derived from an isolated secondary winding on the boost choke rather than using a high voltage diode directly after the choke as in the conventional high voltage boost mode. The dc input to the converter following the ac bridge rectifier is a full-wave rectified sine wave, operating at twice the line frequency (100 or 120 Hz) instead of a pure dc voltage. The normal input “bulk” capacitor following the bridge rectifier must be reduced to a value of 1 μF or less so that the capacitive input filter does not have any significant effect on the power factor. The value of this capacitor should be sufficient to provide a low impedance at the converter’s switching frequency, but small enough to offer very high impedance at the ac line frequency.

Single Stage Converter Characteristics

The single stage, isolated PFC converter can be configured from the conventional buck-boost derived flyback topology. The operational mode can be in discontinuous conduction mode (DCM), critical conduction mode (CrM), or continuous conduction mode (CCM). The most common operational mode for lower power circuits is CrM because of the overall control simplicity and ease of implementation of synchronous output rectification for lower voltage outputs (<12 Vdc). The ON Semiconductor NCL30000 PFC controller is particularly well suited for the lower power applications of 50 W or less which includes LED lighting applications as well as small power adapters. The CrM operational characteristics will be similar to any conventional critical conduction mode boost PFC or flyback converter, namely the switching frequency will vary with line and load, and recovery losses in the output rectifier will be negligible due to the secondary flyback current going to zero prior to re-activation of the main power switch. This latter characteristic makes it straightforward to implement MOSFET synchronous rectifiers in designs where low output voltages require minimal conduction losses in the output rectifier. The ON Semiconductor NCP4304 is particularly well suited for secondary side synchronous rectifier control.

Continuous conduction mode however, can offer significant advantages for applications that require fixed frequency operation; this is especially true for output voltages of 15 Vdc or higher where the use of synchronous rectification yields marginal efficiency improvements. In CCM the peak MOSFET current can be significantly less than in CrM resulting in lower MOSFET switching losses, particularly at power levels above 75 W. CCM operation also reduces the high frequency output capacitor ripple current, and the overall conversion efficiency is generally higher. The NCP1652 controller is designed particularly for CCM operation and also provides a second gate drive output for the implementation of an active clamp snubber for even higher power applications where voltage spikes caused by the flyback transformer's leakage inductance energy can become a significant issue.

The single stage PFC conversion process, regardless of the operational mode, has a few compromises over the traditional two-stage conversion scheme of Figure 9−1. They are as follows:

1. As with any power factor corrector circuit, the gain bandwidth of the control loop is very low, typically in the 10−30 Hz range. This is necessary, otherwise the control loop would attempt to regulate off the line variations of the input and this would result in poor power factor. As a consequence of the low bandwidth, transient response to load step changes will be compromised although dc regulation will be excellent. For adapter applications where point-of-load regulation (POL) is utilized anyway, the slow transient response is inconsequential.
2. Because the loop cannot regulate away the line ripple, it will appear as a ripple component on the output. Therefore sufficient output capacitance must be utilized to keep the line ripple component minimized for the specific application. As mentioned previously, the use of downstream POLs in the system should preclude excessive output capacitance since the ripple will be attenuated sufficiently by the POL regulators. In constant current LED applications, the low frequency ripple will even be less of an issue as long as the peak current requirement for the LED is not violated.
3. Due to the lack of a large input bulk capacitor, the converter has no significant inherent hold-up time other than that provided by the stored energy in the transformer and the output capacitors.
4. The power factor for the single stage converter tends to degrade with increasing line and decreasing load due to factors related to the duty cycle [D/(1−D)] transfer function and non-linearity effects in the magnetics, however, for most typical line and load conditions the PF will be above 0.90.
5. Just like any flyback topology, the effects of leakage inductance in the main power transformer will have a direct impact on performance, EMI, and overall efficiency. The transformer should be wound with proper wire sizing to minimize AC losses due to skin effect, and winding layers should be kept to a minimum to avoid proximity effect and winding self-capacitance. In most cases with off-the-shelf cores, the primary will require 2 layers so it is best to use the "sandwiched" secondary construction where half the primary is wound first, then the secondary, and then the second half of the primary over the secondary. The primaries are then connected in series externally. This construction will help minimize the leakage inductance of the magnetic structure. Under no circumstances should windings be wound in different layers and then paralleled. This construction will result in high circulating currents. Windings requiring multiple strands of wire should be wound "multifilar" and constrained to two layers or less. Moreover, the leakage inductance effects will be more prominent the lower the secondary output voltage due to the coupling effect of the primary to the secondary turns.

Despite these tradeoffs, the single stage, isolated PFC converter is an efficient and very cost effective solution for offline LED power supply units, notebook adapters and similar applications needing compact size with minimal parts count. For LED driver applications, an additional current feedback loop with output current sense resistors can be implemented to provide a constant current, constant voltage (CCCV) characteristic. The ON Semiconductor NCS1002 dual op amp plus reference is well suited for such applications.

Design Example using the NCL30000

An implementation of a CrM/DCM single stage PFC converter based on the compact SO−8 packaged NCL30000 is shown in Figure 9−3. This circuit is optimized for driving high brightness LEDs with constant current control but could be modified for fixed voltage output by changing feedback to a constant voltage configuration. As shown, this circuit provides up to 15 W at a constant 350 mA which is typical for many high brightness LEDs and is capable of powering 4 to 17 white LEDs from a source spanning 90 to 305 Vac.

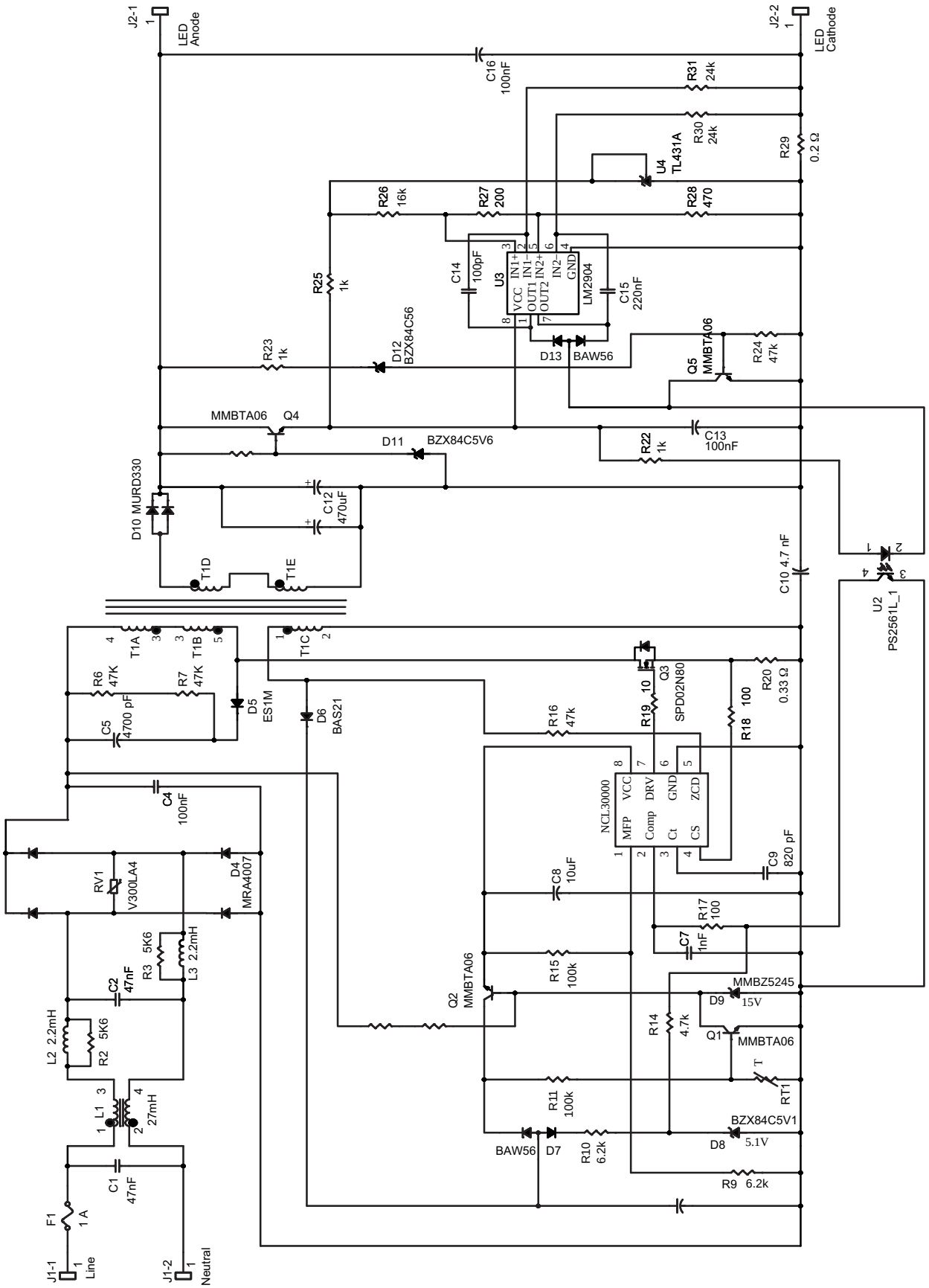

Figure 9−3. Schematic of a 15 W High Power Factor Single Stage LED Driver

The key to high power factor performance in a CrM single stage converter is maintaining fixed on-time over a half cycle of input sine wave. The pulse width is determined by average AC input voltage and power delivered to the load. This control method is explained in detail in the ON Semiconductor NCL30000 datasheet. Switching frequency will vary with input voltage and output load. The zero current detection feature built in to the NCL30000 controller ensures CrM operation by initiating a switching cycle only when the current in the flyback transformer is depleted. The primary inductance of the flyback transformer sets the switching frequency range for a given set of input voltage and output load conditions.

Energy delivered by a single stage converter follows the input sine wave shape starting at zero, reaching a peak, and then falling to zero every input half cycle. Output ripple amplitude is determined by the output filter capacitor. An open load circuit protects the output capacitor in the event the load is disconnected by providing feedback to the NCL30000 controller.

The LED driver shown in Figure 9−3 provides tight current regulation and high efficiency driving 12 white LEDs over the range of 90 to 305 Vac as shown in Figure 9−4. LED current varies less than 1% over the input voltage range. Efficiency is greater than 81% for 115 − 230 Vac applications at nominal load.

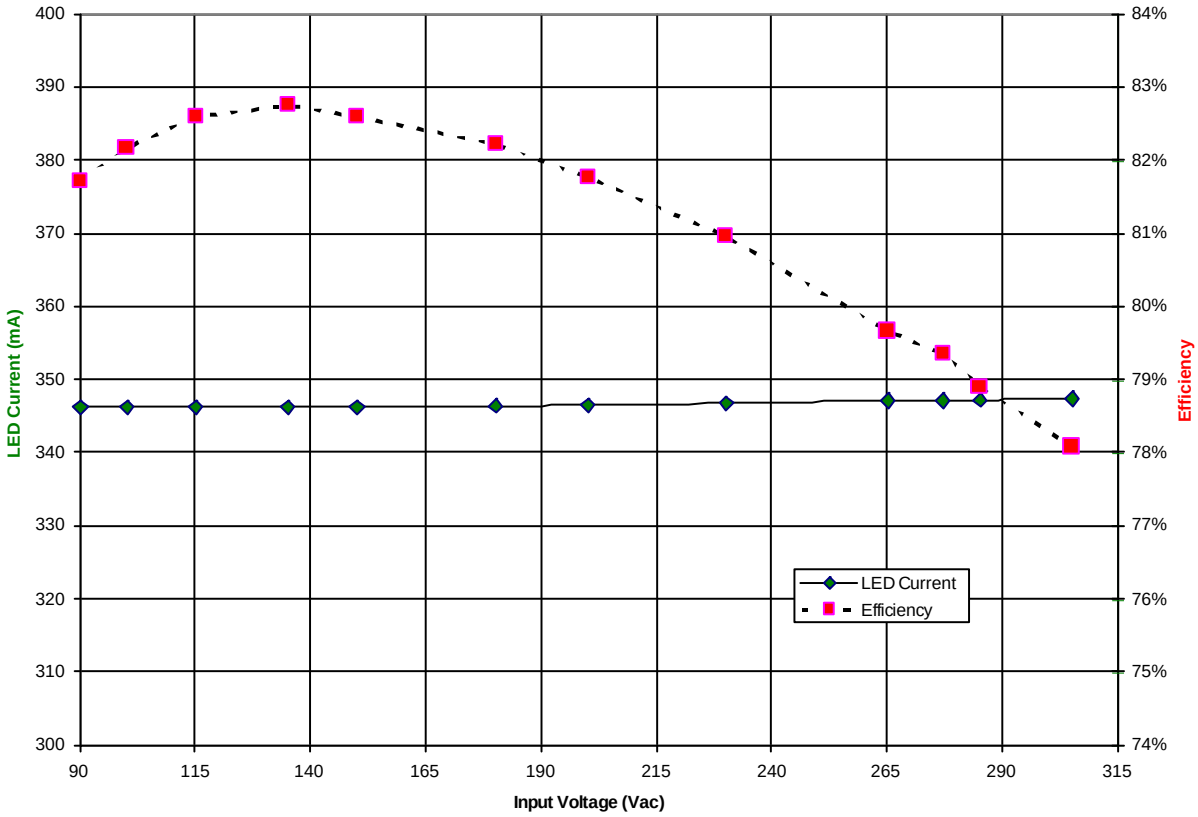

Figure 9−4. Line Regulation and Efficiency Driving 12 LED Load (Vf = 37 Vdc)

Figure 9−5 shows the power factor is maintained above 0.9 and harmonic distortion is less than 13% over the input range of 90 to 305 Vac with a 12 LED load (Vf = 37 Vdc).

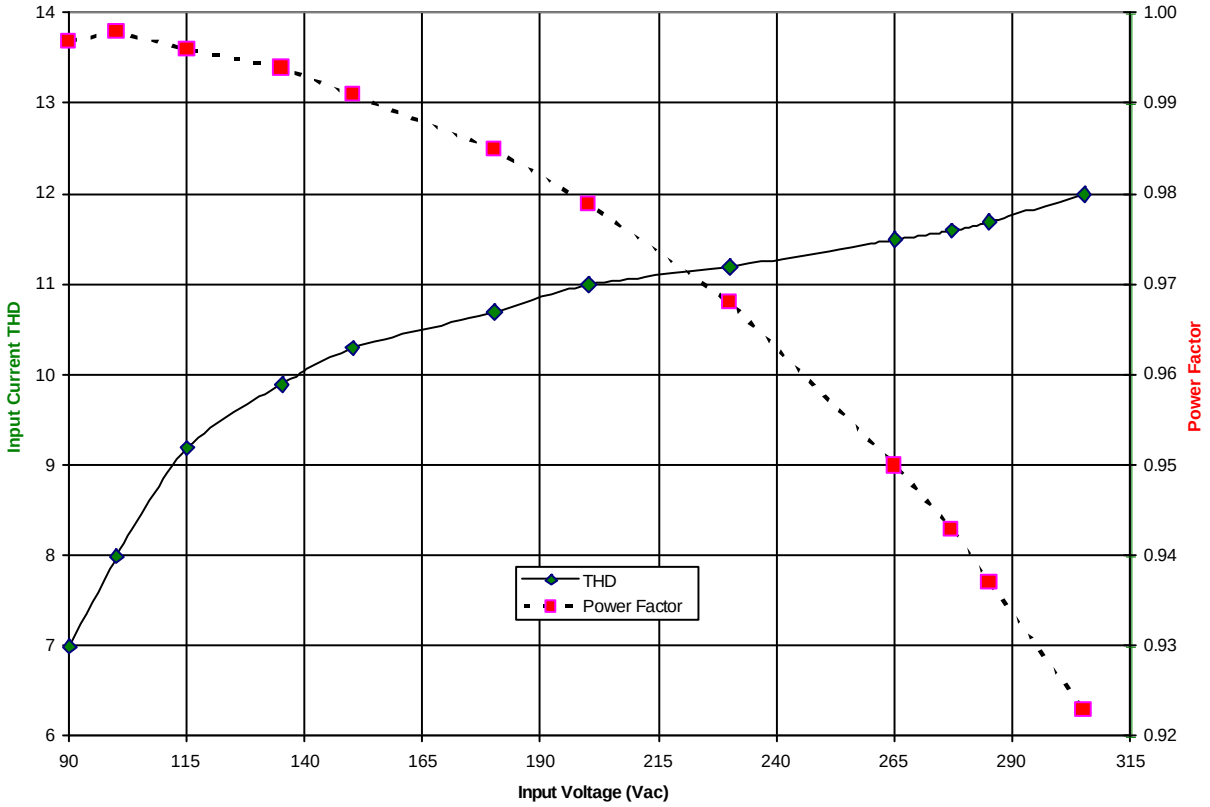

Figure 9−5. THD and Power Factor with 12 LED (Vf = 37 Vdc) Load Over a Wide Input Range

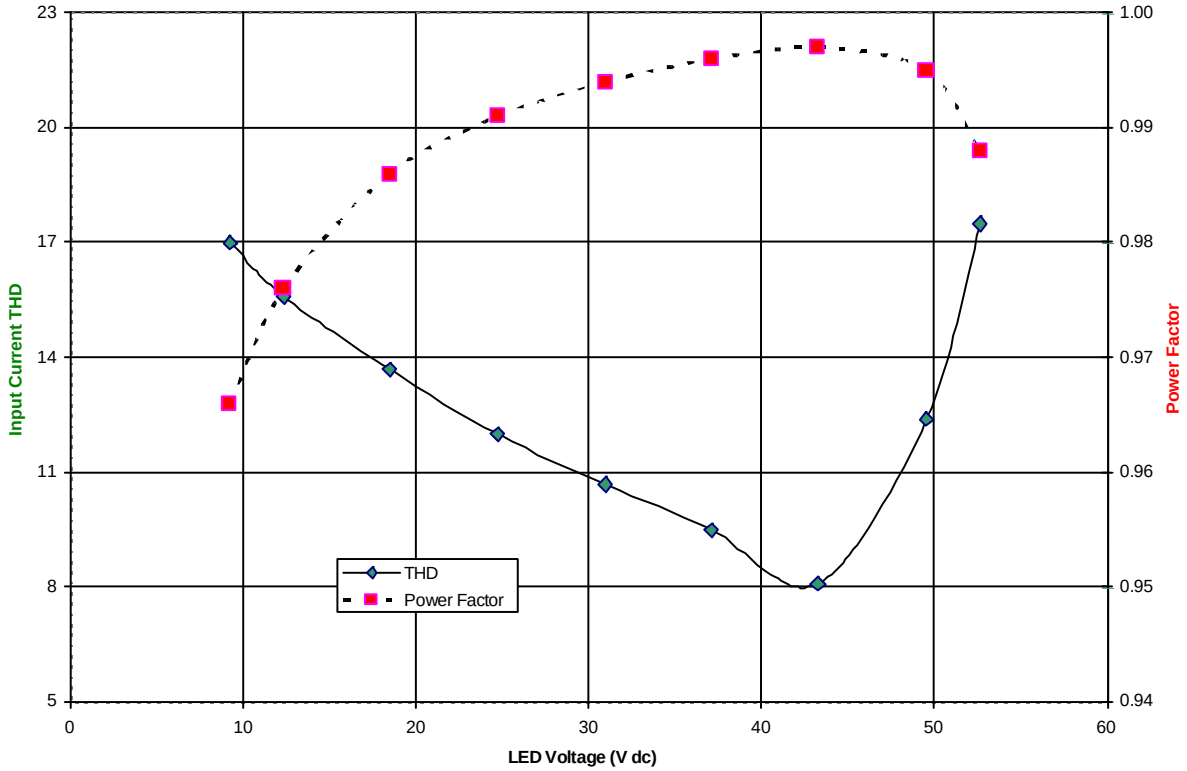

Figure 9−6. Power Factor and THD vs. Load (115 Vac Input)

Power factor is also a function of loading for a given application. Figure 9−6 shows the effect of load on the LED driver at 115 Vac input. Note the input current distortion reaches a minimum near 43 V which is about 15 W output. Power factor reaches a maximum at this same load point. Out of phase line current due to EMI filter capacitors is constant at a given input line voltage, but is a larger percentage of the total line current at lighter loads and has a greater effect on power factor. Figure 9−6 shows this reduction in power factor at light loads.

IEC 61000−3−2 Class C requirements establish the maximum allowable harmonic content for input current in lighting applications. Two limit categories are based on input power draw above or below 25 W. This example driver draws less than 25 W input and must meet requirements only at the third and fifth harmonic of input current as a percentage of fundamental line current draw as shown in Table 9−1 below.

Table 9−1. Line Current Harmonics and IEC 61000−3−2 Limits

Input (Volts)	**Fundamental** (Amperes)	**Third Harmonic**		**Fifth Harmonic**	
		Reading	**Limit**	**Reading**	**Limit**
115	0.13	6.95%	86.0%	0.61%	61.0%
230	0.07	9.91%	86.0%	2.21%	61.0%

Table 9−1 above shows the harmonic content of line current is well below the required levels. Note that requirements for lighting applications equal to or greater than 25 W must meet more restrictive levels which extend up to the 40^{th} harmonic of input current fundamental.

The NCL30000 provides a single stage CrM/DCM solution for driving constant current in LEDs. A power factor greater than 0.9, THD performance of less than 20% across line, high efficiency, and tight regulation over a wide operating range are demonstrated in a circuit with few external components.

Design Example using the NCP1652A

Figure 9−7 shows the schematic of a 19 V, 5 A single stage PFC converter utilizing the NCP1652A controller. This power supply design is intended for laptop and notebook adapters requiring up to 100 W output. The flyback transformer was designed with a high primary inductance (600 μH) to force the circuit to operate in “deep” CCM. This mode reduces the peak MOSFET current and output capacitor rms ripple current for maximum efficiency. The SO−16 and SO−20 packages provide additional pins for additional control features including brownout detection, feed-forward compensation, over-current protection, and a latch input for overvoltage and/or over-temperature protection. The loop gain, multiplier bandwidth and other control parameters can also be tailored to fit the intended application. Design details for this 19 V adapter supply and a similar 48 V, 2 A output power supply intended for telecom and LED applications can be found in ON Semiconductor application notes AND8397 and AND8394 respectively at ON Semiconductor’s website.

A version of the NCP1652A intended specifically for LED lighting applications is the NCL30001 [12]. This controller is identical to the NCP1652A but without the “OUT B” drive output. Applications using this controller in constant voltage, constant current (CVCC) LED lighting power supplies is shown in application notes AND8427 [13], AND8470 [14], and design note DN06068 [15].

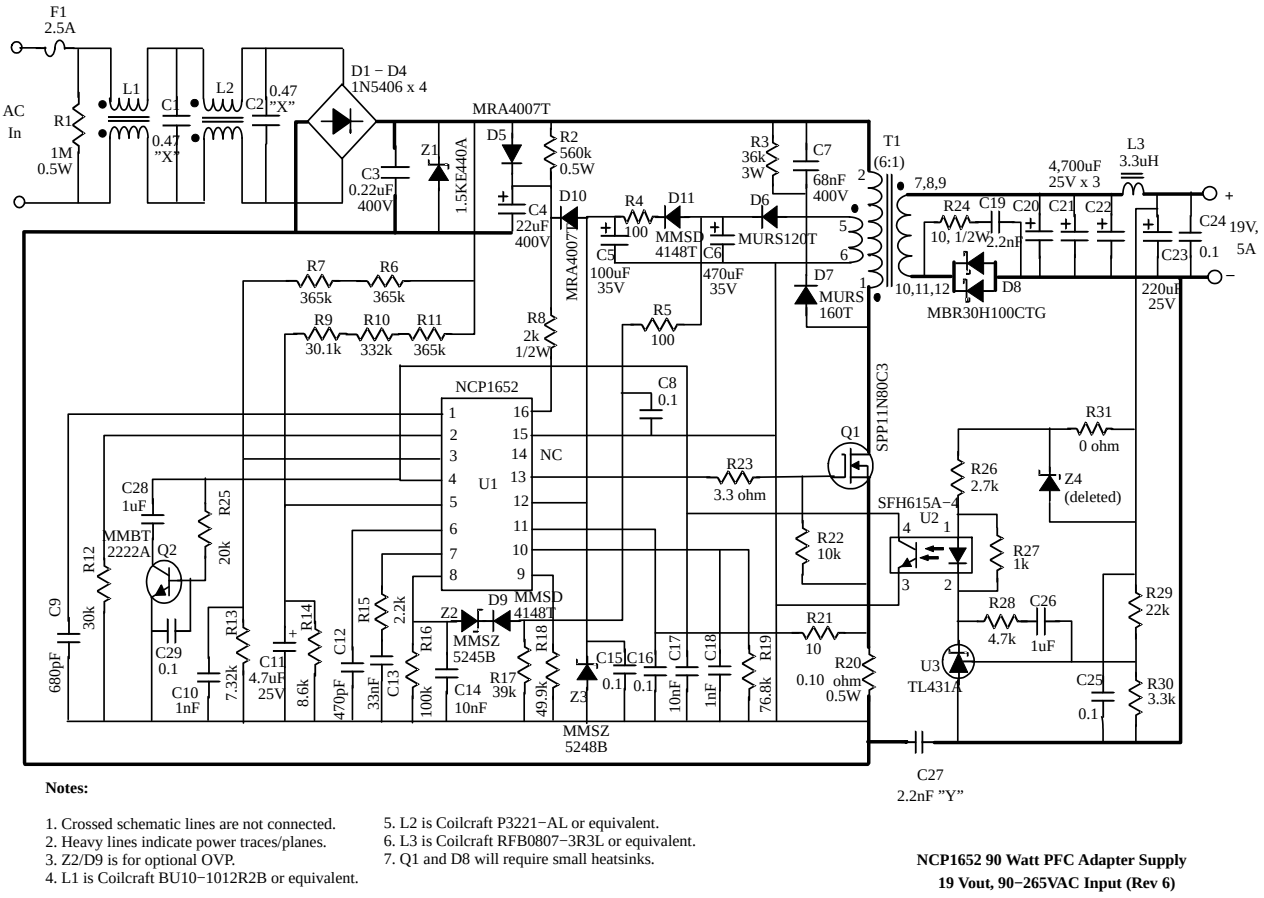

Figure 9−7. 90 W Adapter, Single Stage Converter Schematic

The 19 V, 90 W adapter circuit of Figure 9−7 achieved an average efficiency approaching 90% and a power factor greater than 0.9 for typical operational loads. The data below compares the key parametric results at different line and load conditions. Power factor, THD, and efficiency measurements were taken at loads of 25%, 50%, 75% and 100% at both mains voltages. The efficiencies were averaged per Energy Star criteria. The results are shown in the table below.

Table 9−2

	Load	100%	75%	50%	25%	
Vin = 120 Vac	THD =	6.6	4.5	7.2	11.4	
	PF =	0.995	0.993	0.986	0.948	
	Eff =	88.0	88.9	89.8	89.1	Eff avg = 89%
Vin = 230 Vac	THD =	7.1	10.3	13.8	14.6	
	PF =	0.975	0.951	0.901	0.713	
	Eff =	89.9	89.4	90.4	87.1	Eff avg = 89.2%

Note that for either AC line value, the efficiency easily exceeded the 87% minimum Energy Star requirement for adapters. At no load the input power consumption was less than 500 mW for either 120 or 230 Vac line conditions. The light load efficiency was as follows:

Table 9−3

Output Load	0.5 W	1.0 W	1.7 W
120 Vac in	57%	69%	73%
230 Vac in	47%	59%	69%

Figure 9−8 below shows the output voltage profile for the 19 V adapter at supply turn-on with no load and with full load indicating a controlled voltage rise with no overshoot that is sometimes typical with slow control loops.

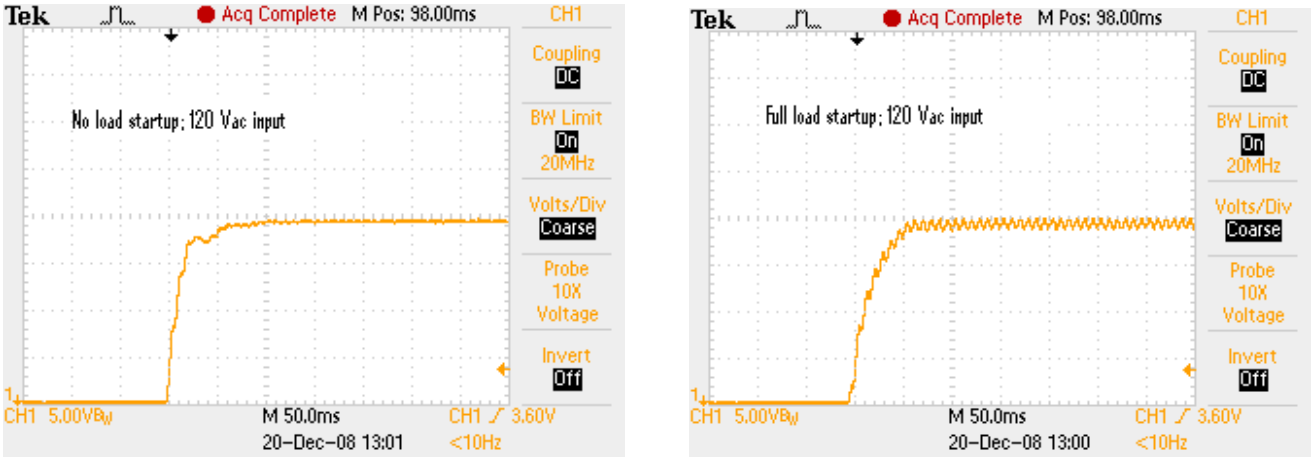

Figure 9−8. Turn-on Profiles

Figure 9−9 below displays the 120 Hz output ripple that passes through the converter. The ripple amplitude is strictly a function of the output capacitance and output load on the power supply since the regulation loop bandwidth is necessarily less than the ripple frequency to assure high power factor.

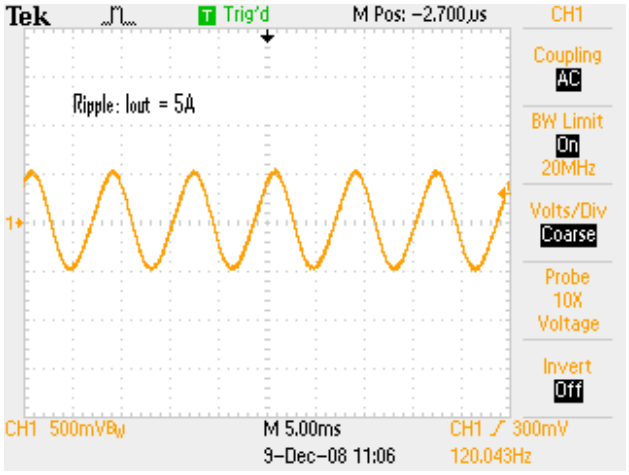

Figure 9−9. Output Ripple

Some Final Comments

Single stage power factor corrected switch mode topologies provide designers with a new tool to develop power supplies when the requirements call for high power factor and compact size and the application can allow some amount of line ripple on the output waveform. In addition to what has been highlighted with these CrM and CCM topologies, it is important to be aware of the limitation in applying these topologies for lower output voltages. Traditionally when the output voltage is 12 volts and less, the efficiency can be enhanced by the use of synchronous output rectifiers instead of convention PN or Schottky diodes. Synchronous output rectifiers are not, however, wholly compatible with continuous conduction mode (CCM) operation.

This is because CCM or DCM operation will almost always transition into the other depending on the load situation. At light load CCM will transition to DCM, and with DCM operation, the startup and over-current conditions usually revert to CCM for fixed frequency converters. As a result of these two different modes of operation, the required gate drive signal to the synchronous MOSFET must be based on different sensing criteria for each mode which causes additional circuit complexity.

The “problem mode” is CCM because there has to be a delayed timing sequence to the sync MOSFET to prevent simultaneous conduction overlap with the main primary side MOSFET. Even though the necessary timing sequence can be achieved, one critical issue still remains. When the sync MOSFET is turned off just prior to the main primary MOSFET coming on, the intrinsic body diode of the sync MOSFET must carry the still flowing continuous flyback current. This parasitic body diode usually has very poor recovery characteristics and when the main MOSFET turns on, the body diode is force commutated off and significant reverse current will flow in the body diode during the recovery process. This current along with the associated circuit reactive parasitics generates large voltage spikes and ringing on the sync MOSFET and main MOSFET during this transition. This usually necessitates the addition of larger snubbers and/or TVS clamping circuits to avoid MOSFET failure. In many cases, the added circuit cost and dissipative issues are generally not worth the increased cost and circuit complexity. So, if synchronous rectification is desired, the control technique to use is critical conduction mode (CrM) where all of the critical switching transitions can take place simultaneously when current in both the primary side and synchronous MOSFETs are zero. In this case no timing sequencing is required and a simple secondary current detection scheme is all that is necessary for effective synchronous rectifier control. Unlike DCM or CCM implementations, CrM does not have any load dependent mode transition, and currents are always zero when switching transitions takes place. For further information on these circuits, please view the detailed applications notes and data sheets available from ON Semiconductor.

References

[1] NCP1652/D: Device Data Sheet
[2] AND8394/D: A 48 V, 2 A High Efficiency, Single Stage, Isolated Power Factor Corrected Power Supply for LED Drivers and Telecom Power (NCP1652)
[3] AND8397/D: A 90 Watt High Efficiency Notebook Adapter Power Supply with Inherent Power Factor Correction (NCP1652)
[4] AND8124/D: 90 W, Universal Input, Single Stage, PFC Converter (NCP1651)
[5] AND8147/D: An Innovative Approach to Achieving Single Stage PFC and Step-Down Conversion for Distributive Systems (NCP1651)
[6] AND8209/D: 90 W, Single Stage, Notebook Adaptor
[7] TND317/D: 90 W Notebook AC/DC Adapter Reference Design
[8] DN06069/D: NCP1028: Single Stage, Off-line, Isolated 12 V, 800 mA Converter with High Power Factor
[9] AND8470/D: A 25 to 55 V, 0.7 to 1.5 A, Single Stage Power Factor Corrected Constant Current Offline LED Driver with Flexible Dimming Options
[10] AND8427/D: A Constant Current Adjustable 0.7 A to 1.5 A, Up to 55 Vdc Single Stage Power Factor Corrected LED Power Supply
[11] NCL30000/D: Power Factor Corrected TRIAC Dimmable LED Driver − Device Data Sheet
[12] NCL300001/D: High Efficiency Single Stage Power Factor Corrected LED Driver − Device Data Sheet
[13] AND8427/D: A Constant Current Adjustable 0.7 A to 1.5 A, Up to 55 Vdc Single Stage Power Factor Corrected LED Power Supply (NCL30001)
[14] AND8470/D: A 25 to 55 V, 0.7 to 1.5 A, Single Stage Power Factor Corrected Constant Current Offline LED Driver with Flexible Dimming Options (NCL30001)
[15] DN06068/D: NCL30001, NCS1002: Up to 28 V, 3.3 A Constant Current Offline High PF LED Driver

CHAPTER 10

Detailed Analyses and Comparisons

This chapter provides a detailed analysis of the results obtained with the three topologies for power factor correction where direct comparison is applicable. These topologies are Continuous Conduction Mode (CCM), Critical Conduction Mode (CrM) and Frequency-Clamped Critical Conduction Mode (FCCrM). Comparative analyses and rankings are provided for the topologies for given criteria.

Comparison Methodology

As discussed in Chapter 2, the comparisons between different topologies are necessary to answer the question of how these topologies perform for a given application. However, the methodology and basis for comparison have to be kept fully under control in order to make meaningful comparisons. If that is not done, the results would come out different and could be misleading.

In order to keep the number of variables as low as possible, the comparisons between the 3 topologies were made with a single power stage PCB. This PCB shown in Figure 10−1 was originally designed for the NCP1654 (CCM) PFC and hence the NCP1654 circuitry was on-board. For the FCCrM and CrM topologies, a daughter card using the NCP1605 and the NCP1607 respectively were made and connected to the main board as shown in Figure 10−2. The flexibility of NCP1605 allows it to be used for pure CrM mode or in the FCCrM mode depending on the choice of the C_{osc} capacitor that sets the maximum frequency. For FCCrM, the C_{osc} choice was set to 730 pF for a maximum frequency of 65 kHz. For CrM, there was an option to use the NCP1605 in pure CrM mode by changing C_{osc} to 100 pF (max frequency to 400 kHz), however, a true CrM controller (NCP1607) was used for more definitive comparisons.

Figure 10−1. Picture of NCP1654 Demo Board Used for Comparisons

The daughter card for FCCrM (NCP1605) shown in Figure 10−2 was modified from the board used in the application note AND8281. For CrM (NCP1607), the daughter card was modified from the board used in the application note AND8353.

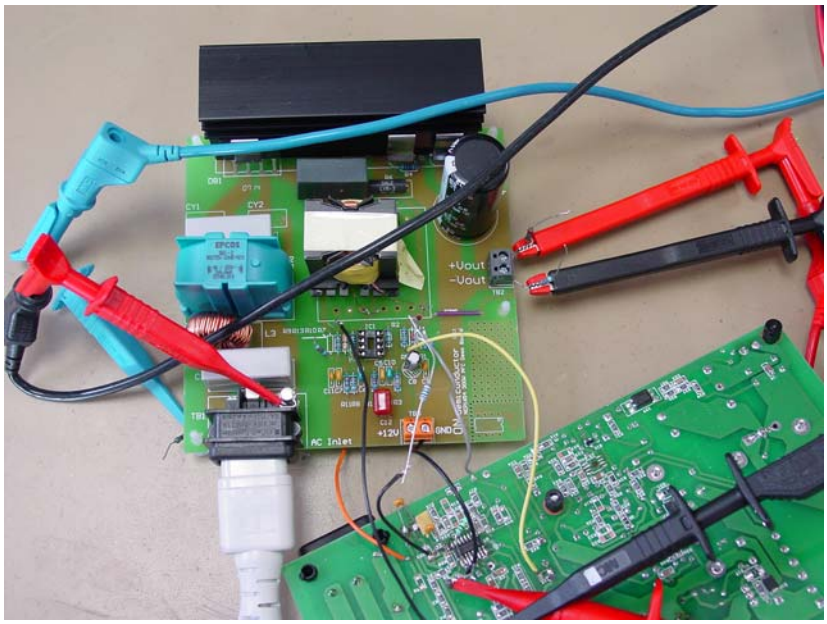

Figure 10−2. Picture of Daughter Board Used for FCCrM Application

This methodology ensured that the same power traces and layout are used for all the topologies. In addition, the consistency of measurements was maintained to make the comparisons more meaningful. The only components that were changed (as needed) for different topologies were the FET, diode and the power inductor and the control circuit. The summary of these choices is shown in Table 10−1 with appropriate comments.

Table 10−1. Component Comparisons for PFC Options

Attribute	P1 − CrM	P2 − FCCrM	P3 − CCM	Comments
Inductor	250 μH 9.33 Apk PQ3230 Core 11.5 cm^2 37.7 cm^3	250 μH 9.33 Apk PQ3230 Core 11.5 cm^2 37.7 cm^3	650 μH 5.42 Apk RM14 Core 20.4 cm^2 61.3 cm^3	Despite the higher inductance value, the CCM inductor size is not much greater than the other options.
Power Switch	600 V 99 mΩ $R_{DS(on)}$ IPP60R099CP TO−220 Package	600 V 99 mΩ $R_{DS(on)}$ IPP60R099CP TO−220 Package	600 V 190 mΩ $R_{DS(on)}$ SPP20N60C3 TO−220 Package	In CCM, relatively higher $R_{DS(on)}$ (and lower cost) FET can be used
Power Diode	Ultrafast 600 V, 8 A MUR550 TO−220 Package	Ultrafast 520 V, 5 A MUR550 TO−220 Package	Merged PN Schottky 600 V, 8 A LQA08TC600 TO−220 Package	CrM and FCCrM allow use of Ultrafast diodes but CCM requires a low Qrr diode for good efficiency
Frequency Range	20−400 kHz	22−67 kHz	65 kHz Fixed	Frequency range of FCCrM offers the advantage of CCM without the diode recovery issues
Control	V-mode	V-mode	I-mode	Dictated by controller design − performance can be optimized around each

Inductor (Lp)

Based on the results in Table 10−1, it may appear at first that the CrM and FCCrM represent the best solution, considering the low inductance value. As mentioned earlier however, this inductor is subjected to larger flux swings as its peak-to-peak current and frequency vary over the line and extra care has to be given to the selection of the magnetic core. Furthermore, P1 and P2 are exposed to much larger inductor currents and will typically require larger gage wire to handle the current capacity. When designing the inductor it is also very important to minimize DCR in order to reduce conduction losses. Strictly comparing the P1 and P2, the FCCrM is better as it subjects the inductor to lower frequency variations.

It should also be noted that one major FCCrM merit is the possibility to use smaller inductors compared to those required by traditional CrM circuits. Since FCCrM clamps the switching frequency, there is no need for a large inductor to pull down the CrM switching frequency range and smaller inductors can be used without any significant efficiency reduction. This study is however based on the same inductor for CrM and FCCrM approaches for the sake of consistency.

The CCM boost inductor needs a higher inductance. Thanks to its lower flux density swing, the CCM topology could use a low loss core material such as KoolMu or MPP. In FCCrM or CrM, because the flux density swing is high, the core loss dominates. It is therefore necessary to choose Ferrite to reduce the core losses. In this test, we still use Ferrite core for the CCM topology for a more fair comparison, because the Ferrite's core losses are minimal.

Power Switch

For CrM and FCCrM, a lower $R_{DS(on)}$ and new generation MOSFET (IPP60R099CP) was used, that allowed conduction loss reduction without increasing switching losses. However, as was shown in Chapters 3 and 6, the CCM topology is less sensitive to the MOSFET change to a higher $R_{DS(on)}$ value, so it was implemented using a FET that is twice the $R_{DS(on)}$ (SPP20N60C3) from older generation. This is understandable because the rms and peak currents are lower in CCM and hence, when a higher $R_{DS(on)}$ FET is used, the conduction loss increase is not that significant. On the other hand, the lower Coss of the FET will result in lower switching losses. For the CrM, the conduction loss is a dominant factor at heavy load while the turn-on losses are low. So, the CrM and FCCrM take benefit from a low $R_{DS(on)}$ power switch.

Power Diode

The diode choices were made based on the appropriate technology and availability of components. For CCM, for example, the diode choice is more critical – this led to the selection of the LQA08TC600 from QSpeed. Similarly, the FCCrM topology was able to utilize a lower current, lower voltage diode (MUR550) without impacting the efficiency. That same diode was tried in the CrM topology.

Results

Figure 10−3 summarizes the results for the PFC stages. It can be seen that the three topologies offer a high efficiency. The CCM solution is however a bit worse at low line, full load as a consequence of higher switching losses. FCCrM provides a slightly better efficiency under most conditions than the other two. The CrM performance is similar to the FCCrM at low line, full load but declines at light load and high line as a result of the switching frequency taking off. In terms of power density, the dominant factor was the inductor, and it is larger for the CCM topology. All other aspects of the designs are similar. From a cost perspective, the higher cost of the CCM PFC inductor and diode is likely to be offset by the lower cost of the power MOSFET, leading to a very comparable cost metric at these power levels. Detailed cost analysis is not within the purview of this study as it depends on many other commercial considerations.

The next three figures have a graphical representation of the efficiency observed at different power levels and different input voltages.

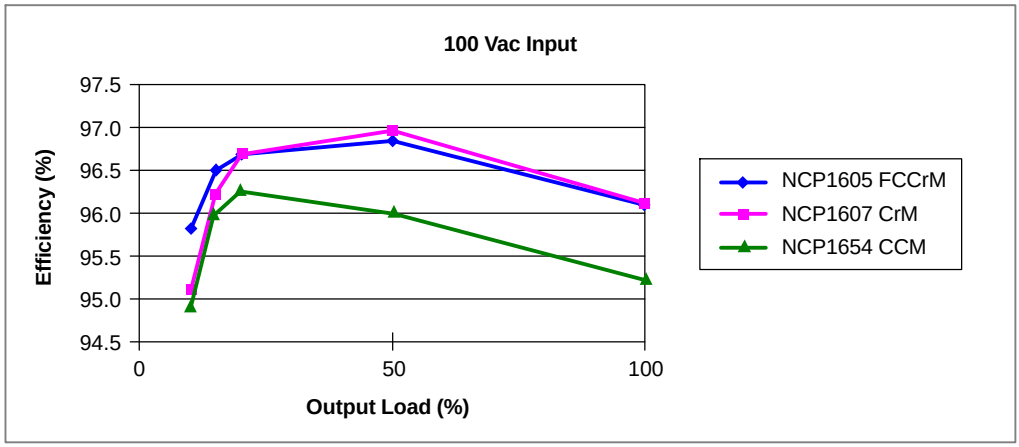

Figure 10−3. Efficiency Performance at 100 Vac

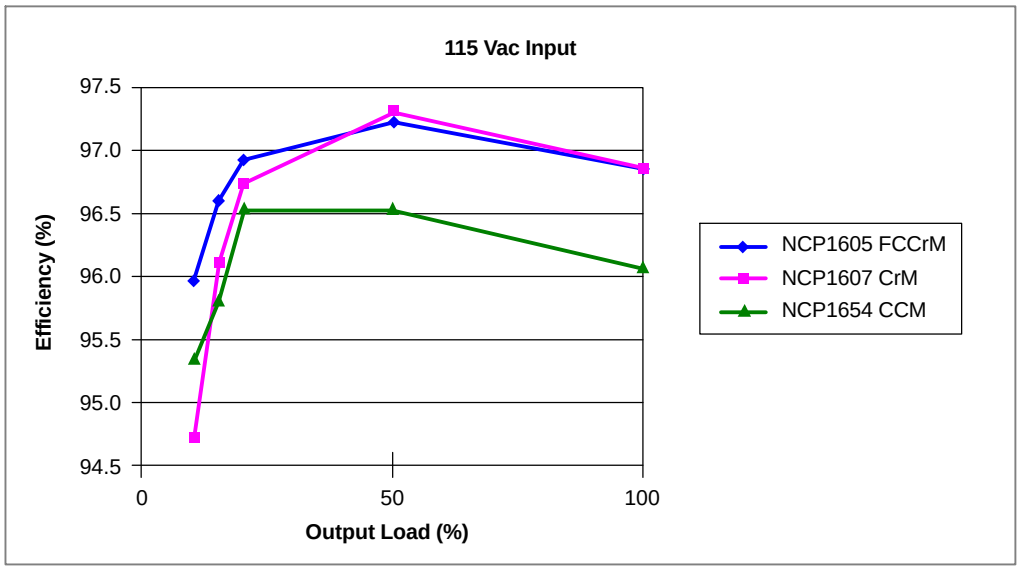

Figure 10−4. Efficiency Performance at 115 Vac

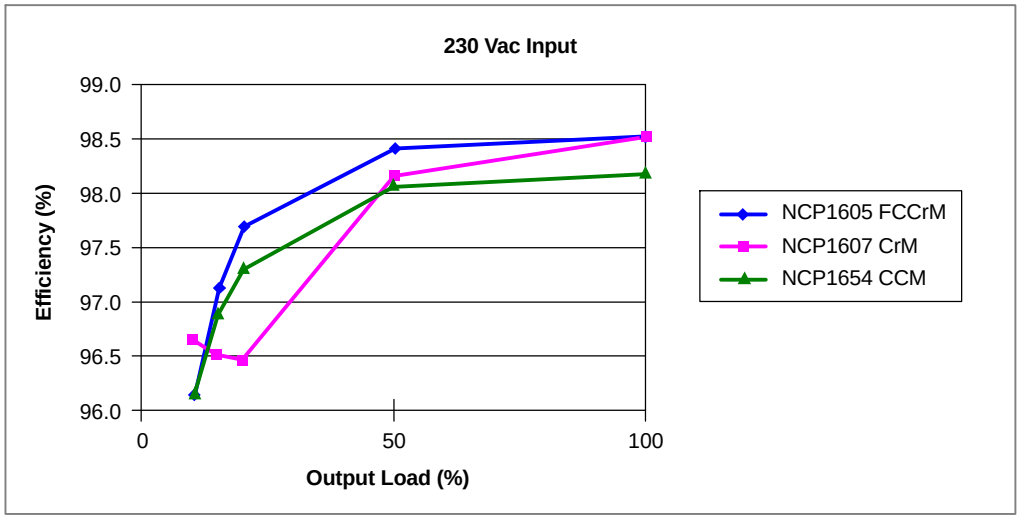

Figure 10−5. Efficiency Performance at 230 Vac

The THD data are plotted in Figure 10−6 and the corresponding PF and THD table is given in Table 10−2. Table 10−3 further gives the PF performance at mid-load. The THD and PF data indicate that all the three topologies yield low harmonics and high power factor which will comfortably meet the existing IEC61000−3−2 and Energy Star requirements. However, amongst the three topologies, the CCM consistently provides better power factor and lower harmonic distortion. This can be attributed to the fixed frequency, the lower current ripple operation and the total absence of dead-time (1). Also, the EMI filter that influences the performance was optimized for the CCM topology. The FCCrM topology yields THD and PF performance which is very comparable to the CCM topology. At low line, the data are slightly worse, but that can be partly attributed to the daughter board set-up. Finally, the CrM topology seems to perform slightly better at low line, but deteriorates at high line – this can be attributed to much higher frequency variation at high line compared to low line. Since the THD performance is typically measured at high line, it is apparent that both CCM and FCCrM topologies give superior performance for THD compared to the CrM topology.

Table 10−2. Total Harmonic Distortion Comparison

	CrM		FCCrM		CCM	
Vin	**PF**	**THD** (%)	**PF**	**THD** (%)	**PF**	**THD** (%)
100	0.997	7.2	0.996	7.5	0.998	5.2
115	0.996	7.9	0.997	6.1	0.998	4.9
230	0.980	15.9	0.988	7.2	0.993	6.3

(1) *In CrM and FCCrM, the MOSFET does not turn on immediately when the inductor current reaches zero but after the short dead-time necessary for the MOSFET drain-source voltage to drop to its valley (for reduced turn-on losses). This dead-time and the small resonant current that takes place are sources of distortion.*

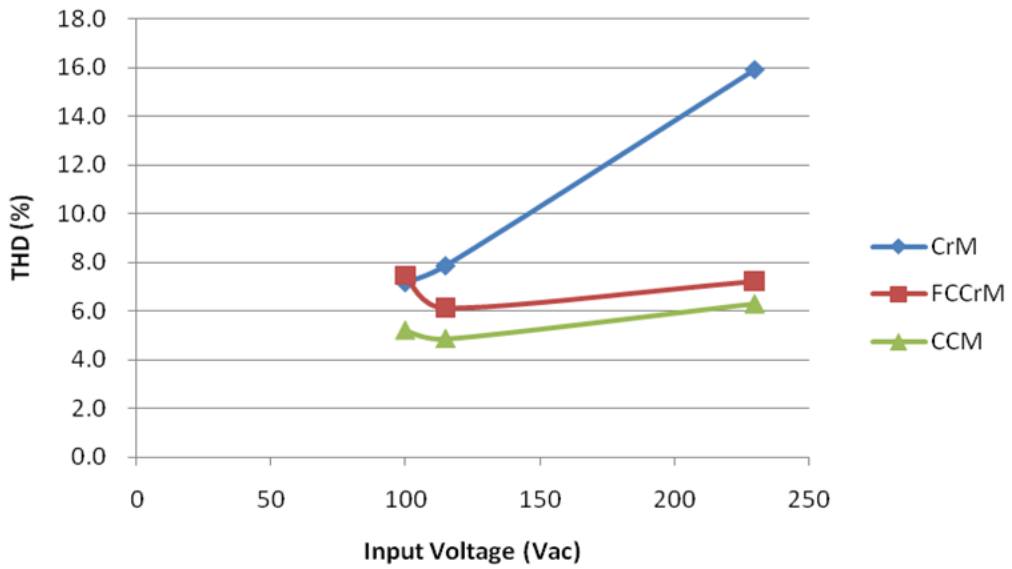

Figure 10−6. Total Harmonic Distortion Comparison

Table 10−3. Measured Power Factor for Different Line and Load Conditions

Load	Input Voltage (V)	CrM	FCCrM	CCM
50%	100	0.996	0.994	0.996
50%	115	0.993	0.995	0.994
50%	230	0.892	0.945	0.978
100%	100	0.998	0.994	0.998
100%	115	0.998	0.992	0.997
100%	230	0.970	0.967	0.991

Trends and Projections

While the results in these sections have provided a good direct performance comparison between different topologies for PFC, they are for a specific application and power level. As we look for broader range of power and applications, some general observations and priorities can be made which are useful guidelines in selecting the appropriate topology for that power level and application.

Applicability of PFC Topologies

In addition to the efficiency, there are many other attributes that can dictate the choice of the most appropriate PFC topology. Following table (Table 10−4) provides the comparison of the different topologies with respect to the key design attributes.

Table 10−4. Ranking of PFC Topologies for Different Attributes

	CrM	FCCrM	CCM	Interleaved	Bridgeless	Single Stage	Follower Boost
Low Profile	****	****	***	+	****	–	****
EMI	***	****	****	+	****	–	***
Isolation						+	
Efficiency	****	****	****	+	+	****	•
Compactness	****	****	****	–	****	+	****
Hold-Up Time	****	****	****	****	****	–	–
Transient Response	****	****	****	****	****	**	*****
Harmonic Performance	****	*****	*****	*****	*****	***	****
Relative Cost	****	****	***	***	–	+	•
High Power Capability	***	****	*****	****	+	–	***

+ indicate a major strength
− indicate a major limitation
• are for major benefits that may affect the downstream converter design

Also, depending on end application segments, certain topologies are more preferred than others. Following Table 10−5 highlights the choices of PFC circuits for different topologies.

Table 10−5. Application Based Preferences of PFC Topologies

	Power Range (W)	Preferred Topology 1	Preferred Topology 2	Preferred Topology 3
Notebook Adapter	75−150	FCCrM	CrM	Single Stage
ATX Power Supply	200−500	CCM	FCCrM	CrM
Server Power Supply	400−1000	CCM	Interleaved	Bridgeless
Flat TV Power Supply	100−500	FCCrM	Interleaved	CCM
Lighting	10−100	Single Stage	FCCrM	CrM
Telecom Rectifier	1000+	Bridgeless	CCM	Interleaved
On-Line UPS	500+	Bridgeless	CCM	

Suggestion only − Make final choice after careful consideration.

Tables 10−4 and 10−5 are indicative as specific requirements or particular embodiment of the considered topology can change the ranking. For instance, the need for a superior efficiency, may lead to prefer the bridgeless or interleaved topology to the CCM one in server applications. Similarly, the need for compactness may cause the FCCrM or CCM solution to be adopted in lieu of the CrM option for adapters.

Summary

The above comparisons yield some interesting information and the following observations can be made for the three different control modes:

CrM

- **Pros**: Good efficiency for power levels below 300 W.
- **Cons**: Wide frequency, bigger PFC choke, a differential mode choke is needed to reduce the input current ripple and EMI. This differential mode choke introduces more losses that affect the overall efficiency.

FCCrM

- **Pros**: At power levels below 300 W, FCCrM PFC can have the same efficiency as CrM at low AC line and an even better efficiency at high line. Furthermore, additional benefits include a smaller choke (verified in our testing) and a substantial EMI and THD improvement thanks to the frequency clamp.
- **Cons**: Its complexity makes it difficult to understand how to control the on time (but it has been done inside the controller). A differential mode choke is also needed to reduce the input current ripple and EMI, which affects the overall efficiency.

CCM

- **Pros**: Fixed frequency, lower EMI filter, and a smaller ripple on the input and output stage which creates little stress for the input filter and output capacitor. Therefore this control mode is more suitable for high power applications.
- **Cons**: This control mode exhibits higher switching losses due to the Qrr of the boost diode. In this control mode, the boost diode therefore becomes a critical component of the PFC stage.

CCM seems to produce a lower efficiency than FCCrM and CrM at 270 W. It is however important to note that the efficiency was measured with an EMI stage tailored for the CCM solution (keep in mind that the NCP1654 demo-board is used for the three topologies). The CrM and FCCrM topologies would require a bigger differential mode choke that would lead to some additional losses.

Based on the results, it can be said that the FCCrM topology offers the best alternative for the given application. However, the other topologies also yielded very good efficiency and THD performance and can certainly be made to work in the applications without any problems.

NOTES

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RS Components KK	jp.rs-online.com	(81) 45 335 8550
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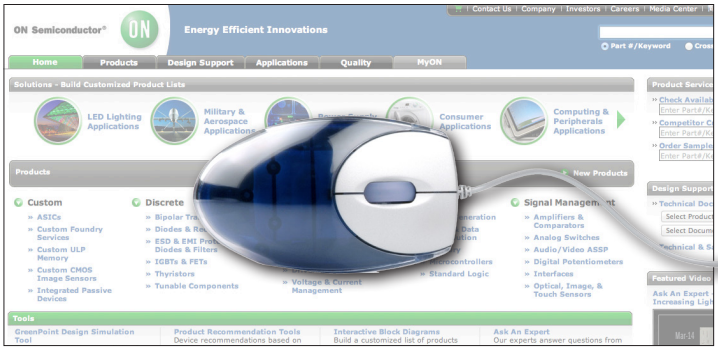

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