High Performance Switcher Integrated with HV Startup and SENSEFET®

Advance Information

FSL518H, FSL538H, FSL518A, FSL538A

The FSL5x8 is an integrated peak-current-mode controlled pulse width modulation (PWM) power switch, specifically designed for off-line switch-mode power supplies. The PWM controller includes an advanced soft-start, frequency hopping, optimized gate driver, internal transconductance amplifier, temperature-compensated precise current source for loop compensation and enhanced self-protections as well. Compared to a discrete MOSFET and PWM controller solution, the FSL5x8 allows to reduce total cost, component count, size, and weight, while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform for cost-effective design of both isolated and non-isolated Flyback converters.

Features

- Integrated Rugged 800 V Super-Junction MOSFET with SENSEFET Technology
- Built-in HV Current Source for Start-up
- Peak-current-mode Control with Slope Compensation
- AC Line Compensation for Accurate Over Power Protection
- Advanced Soft-start for Low Electrical Stress
- Pulse-by-pulse Current Limit
- FSL5x8A: 100 kHz and FSL5x8H: 130 kHz
- Line Brown-in, Brown-out Function
- Line Over-voltage Protection (LOVP)
- Adjustable Burst−mode Operation
- Frequency Hopping for Low EMI
- All Protections are Auto-Recovery: Brown-out, OLP, OVP, AOCP and TSD
- These Devices are Pb-Free, Halogen Free/BFR Free and RoHS Compliant

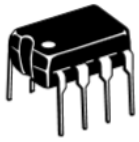
Typical Applications

- Power Supplies for White Goods
- Industrial Auxiliary Power Supply, E-metering SMPS
- Consumer Electronics (Chargers, Set-top-boxes and TVs)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ON Semiconductor®

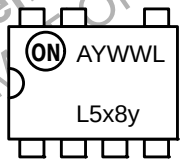
www.onsemi.com



PDIP−7
CASE 626A

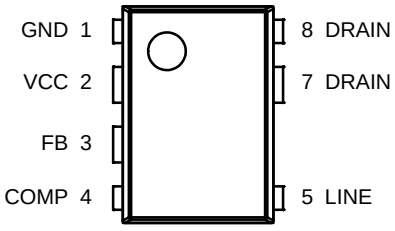
PDIP−7 MISSING PIN GW
CASE 707AA

MARKING DIAGRAM



A	= Plant Code
Y	= 1−digit Year Code
W	= 1−digit Week Code
WL	= 2−digit Die−Run Code
L5x8	= Specific Device Code
x	= Device Option (1 or 3)
y	= Frequency Option (A or H)

PIN CONNECTIONS



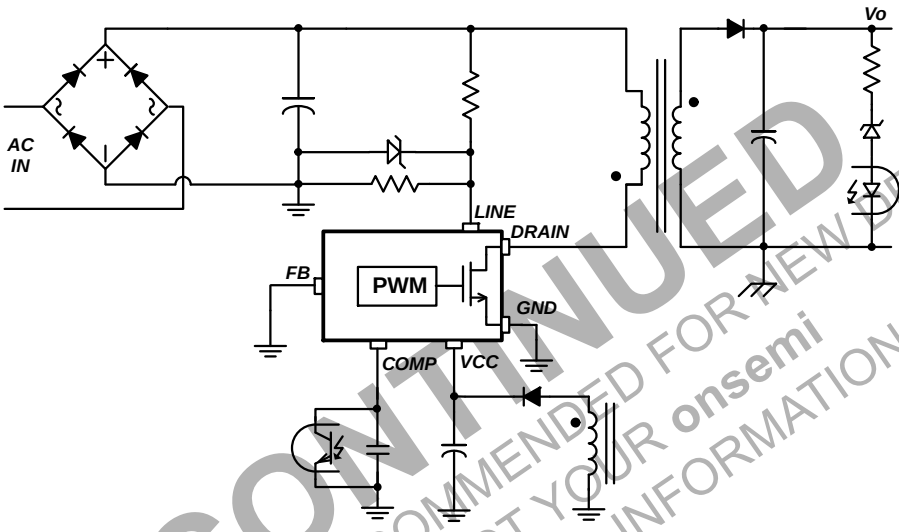
ORDERING INFORMATION

See detailed ordering and shipping information on page 25 of this data sheet.

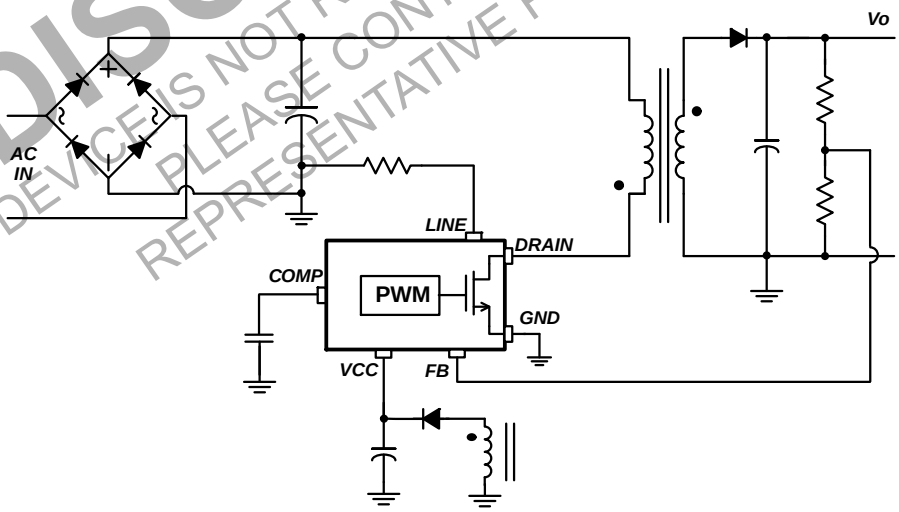
PRODUCT INFORMATION & INDICATIVE RECOMMENDED OUTPUT POWER

Part Number	Package	Operating Junction Temperature	Operation Frequency	Output Power Table (Open Frame) (Notes 1, 2)			
				Current Limit (A)	Max. $R_{DS(ON)}$ (Ω)	230 V_{AC} ± 15%	85 ~ 265 V_{AC}
FSL518H	PDIP−7 / PDIP−7 GW	−40 ~ 125°C	130 kHz	0.46	8.0	15 W	12 W
FSL538H	PDIP−7 / PDIP−7 GW	−40 ~ 125°C	130 kHz	0.66	4.6	21 W	17 W
FSL518A	PDIP−7 / PDIP−7 GW	−40 ~ 125°C	100 kHz	0.61	8.0	17 W	14 W
FSL538A	PDIP−7 / PDIP−7 GW	−40 ~ 125°C	100 kHz	0.86	4.6	25 W	20 W

1. The junction temperature can limit the maximum output power.
2. Maximum practical continuous power in an open-frame design at 50°C ambient.



(a) Isolated Opto−coupler Feedback (Enable Line Detection)



(b) Non−isolated Direct Feedback (Disable Line Detection)

Figure 1. Application Schematic − Isolated or Non-isolated Flyback Converter

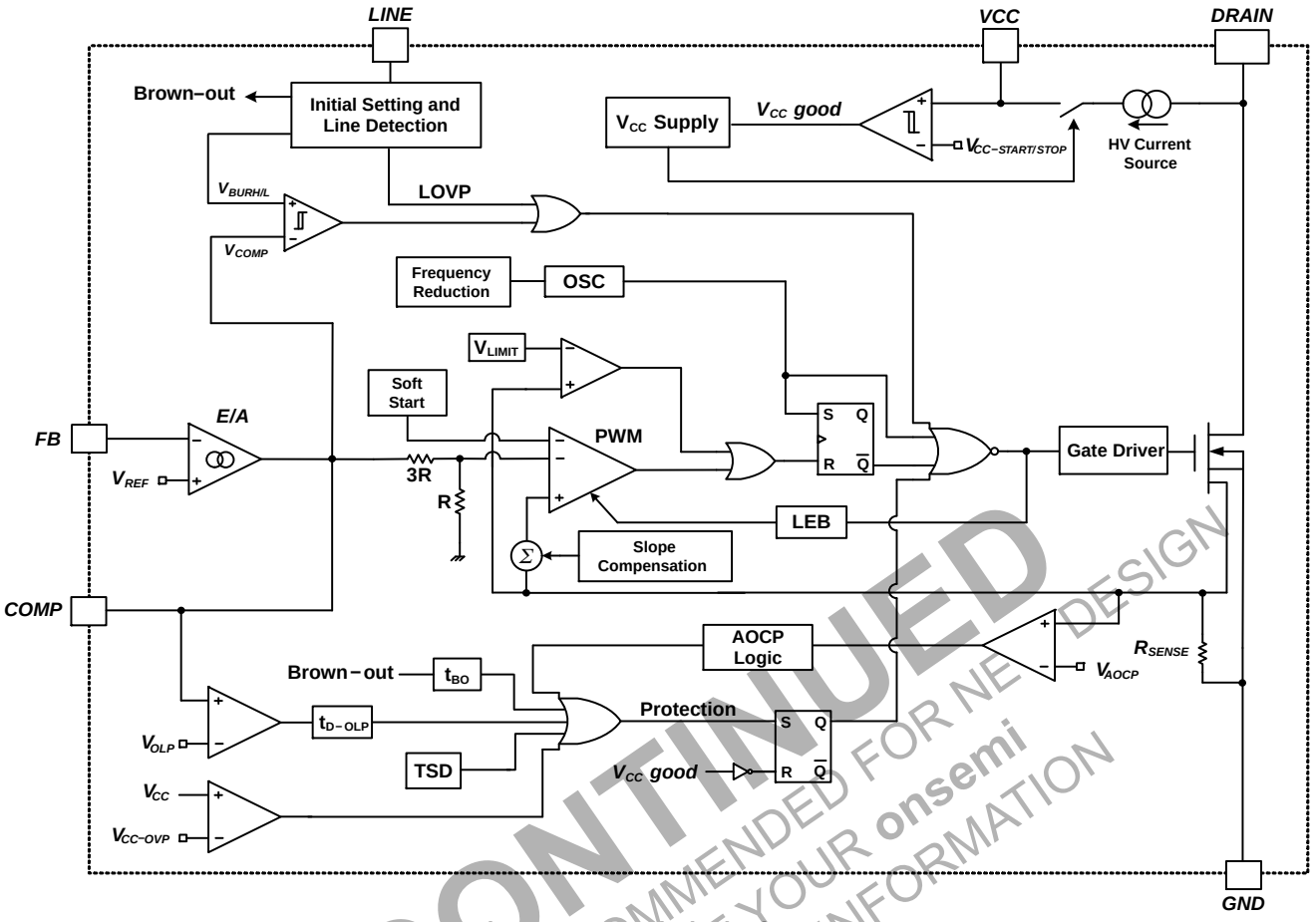


Figure 2. Internal Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Pin Function	Description
1	GND	Ground	SENSEFET source terminal and internal controller ground.
2	VCC	Power Supply	This pin is connected to an external capacitor and provides internal operating current of the IC. It also includes an auto-recovery over-voltage protection.
3	FB	Feedback	This pin is connected to the input of transconductance amplifier for regulating output voltage of the power converter. If transconductance amplifier is not used, connect FB to GND.
4	COMP	Feedback-Loop Compensation	Control-loop compensation. For opto-coupler feedback, connect COMP to opto coupler directly.
5	LINE	Brown in/out, LOVP, Burst-mode Setting	For line detection(Line OVP, Brown in/out), this pin needs to be connected to the high-voltage DC link through voltage divider. And it's also multiple-function pin for burst−mode adjustment.
7,8	DRAIN	MOSFET Drain	High-voltage power MOSFET drain connection. In addition, during startup and protection mode, the internal high-voltage current source supplies internal bias current and charges the external capacitor connected to the VCC pin.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DRAIN Pin Voltage	V_{DS}	−0.3 to 800	V
VCC Pin Voltage	V_{CC}	−0.3 to 26	V
Feedback Pin Voltage	V_{FB}	−0.3 to 5.0	V
Compensation Pin Voltage	V_{COMP}	−0.3 to 5.0	V
Line-detection Pin Voltage	V_{LINE}	−0.3 to V_{CC}	V
DRAIN Pin Pulsed Current (Note 3) FSL518H/A FSL538H/A	$I_{D-PULSE}$	 2.1 2.8	A
Single Pulse Avalanche Energy (Note 4) FSL518H/A FSL538H/A	E_{AS}	 6.0 11.7	mJ
Total Power Dissipation (PDIP−7 / PDIP−7 GW) FSL518H/A & FSL538H/A	P_D	 1.25	W
Junction Temperature (Note 5)	T_J	150	°C
Operating Junction Temperature (Note 6)	T_J	−40 to +125	°C
Storage Temperature	T_{STG}	−55 to +150	°C
ESD Capability HBM, JESD22−A114 ESD Capability HBM, JESD22−A114 (Except DRAIN pin)		1000 2000	V
ESD Capability CDM, JESD22−C101		1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. Repetitive peak switching current when the inductive load is assumed: Limited by maximum duty and junction temperature.
4. L= 45 mH, starting T_J = 25°C.
5. Although this parameter guarantees IC operation, it does not guarantee all electrical characteristics.
6. Junction temperature can limit maximum output power of power converter controlled by the device.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, PDIP−7 / PDIP−7 GW Thermal Resistance, Junction-to-Air (Note 7) FSL518H/A & FSL538H/A Thermal Reference, Junction-to-Lead (Note 7) FSL518H/A & FSL538H/A	 $R_{\theta JA}$ $R_{\psi JL}$	 100 18	°C/W

7. JEDEC recommended environment, JESD51−2, and test board, JESD51−3, with minimum land pattern.

ELECTRICAL CHARACTERISTICS

T_J = −40 to +125°C and V_{CC} = 14 V unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SENSEFET Section						
MOSFET Peak Current Limit	T_J = 25°C, Duty = 60% di/dt = 100 mA/μs FSL518H di/dt = 100 mA/μs FSL518A di/dt = 143 mA/μs FSL538H di/dt = 143 mA/μs FSL538A	I_{LIM}	 428 560 614 790	 460 610 660 860	 492 660 706 930	mA
Drain-to-Source On-State Resistance	MOSFET ON, T_J = 25°C FSL518H/A, I_{DRAIN} = 0.46 A FSL538H/A, I_{DRAIN} = 0.66 A	$R_{DS(ON)}$		 6.3 3.8	 8.0 4.6	Ω
Output Capacitance (Note 9)	V_{DS} = 480 V, V_{GS} = 0 V, f = 1 MHz, T_J = 25°C FSL518H/A FSL538H/A	C_{OSS}		 3.8 5.0		pF

ELECTRICAL CHARACTERISTICS (continued)
T_J = −40 to +125°C and V_{CC} = 14 V unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SENSEFET Section						
Effective Output Capacitance (Note 9)	V_{DS} = 0 to 480 V, V_{GS} = 0 V, T_J = 25°C FSL518H/A FSL538H/A	$C_{OSS(eff)}$		 31 40		pF
DRAIN Voltage Rise Time (Note 8)	V_{DRAIN} = 40 V to 360 V FSL518H/A, I_{DRAIN} = 0.4 A FSL538H/A, I_{DRAIN} = 0.6 A	t_r		 26 35		ns
DRAIN Voltage Fall Time (Note 8)	V_{DRAIN} = 360 V to 40 V FSL518H/A, I_{DRAIN} = 0.4 A FSL538H/A, I_{DRAIN} = 0.6 A	t_f		 34 30		ns
Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA, T_J = 25°C	BV_{DSS}	800			V
Zero Gate Voltage Drain Current	V_{DS} = 800 V, V_{GS} = 0 V, T_J = 25°C V_{DS} = 640 V, V_{GS} = 0 V, T_J = 125°C	I_{DSS}			25 250	μA
VCC Section						
Controller Turn-on Threshold Voltage		$V_{CC-START}$	15	16	17	V
Under-voltage Lockout Threshold Voltage		$V_{CC-STOP}$	7	8	9	V
V_{CC} Regulation Voltage	During Protection, T_J = 25°C	$V_{CC-HVREG}$	9	10	11	V
Restart Time in Protection Mode (Note 9)		t_{AR}		800		ms
Soft-start Time		t_{SS}	7	10	13	ms
Oscillation Section						
Switching Frequency	V_{CC} = 14 V, V_{COMP} = 3.6 V, T_J = 25°C FSL5x8H FSL5x8A	f_S	 122 94	 130 100	 138 106	kHz
Switching Frequency Variation	T_J = −40 ~ 125°C	Δf_S		±5	±10	%
Frequency Modulation Range	V_{COMP} = 3.6 V FSL5x8H FSL5x8A	f_M		 ±6.2 ±4.8		kHz
Frequency Modulation Period (Note 9)	V_{COMP} = 3.6 V	T_{FM}		3.2		ms
Green-mode Entry Frequency	V_{COMP} = 1.4 V FSL5x8H FSL5x8A	f_N		 115 89		kHz
Green-mode Ending Frequency	V_{BURL} = 0.4 V	f_G	22	25	28	kHz
Frequency-limiting Voltage		V_{COMP-S}		V_{OLP}		V
Green-mode Entry COMP Voltage (Note 9)		V_{COMP-N}		1.4		V
Green-mode Ending COMP Voltage		V_{COMP-G}		V_{BURL}		V
Burst-Mode Section						
COMP Threshold Voltage for Entering Burst−mode when Line Detection is Enabled	V_{LINE} in $V_{LINE-SET0}$ during t_{SET} V_{LINE} in $V_{LINE-SET1}$ during t_{SET} V_{LINE} in $V_{LINE-SET2}$ during t_{SET}	V_{BURL}	0.35 0.45 0.55	0.4 0.5 0.6	0.45 0.55 0.65	V
COMP Threshold Voltage for Entering Burst−mode when Line Detection is Disabled	0.9 V < V_{LINE} < 1.2 V 1.2 V < V_{LINE} < 3.6 V	V_{BURL}	0.4 $A_{V-BURST} \times V_{LINE}$			V
COMP Threshold Voltage for Leaving Burst−mode		V_{BURH}	V_{BURL} + 0.1			V

ELECTRICAL CHARACTERISTICS (continued)
T_J = −40 to +125°C and V_{CC} = 14 V unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Control Section						
Maximum Duty Ratio	V_{COMP} = 3.6 V	D_{MAX}	68	75	82	%
COMP Output High Voltage	COMP−pin Open	$V_{COMP-OPEN}$		5		V
COMP Sourcing Current		I_{COMP}	70	100	135	μA
Transconductance of Internal Error Amplifier		G_M		300		μS
Current-sourcing capability of Internal Error Amplifier	$V_{FB} = V_{REF} - 1$ V	$I_{GM-SOURCE}$	55	90	125	μA
Current-sinking capability of Internal Error Amplifier	$V_{FB} = V_{REF} + 1$ V	$I_{GM-SINK}$	−55	−90	−125	μA
Reference Voltage to Regulate FB-pin Voltage		V_{REF}	2.45	2.5	2.55	V
Leading-edge Blanking Time of Internal SENSEFET Current Signal (Note 9)		t_{LEB}		250		ns
Propagation Delay of Turning-off Power MOSFET (Note 9)		t_{PD}		100		ns
LINE Section						
Threshold Voltage for Line Detection Enable	$V_{LINE} > V_{LINE-DET}$	$V_{LINE-DET}$	0.15			V
Threshold Voltage for Line Detection Disable	$V_{LINE} < V_{LINE-ADJ}$	$V_{LINE-ADJ}$			0.05	V
Burst-mode Level Setting Time when Line Detection is Enabled (Note 9)		t_{SET}		100		μs
Sourcing Current for Detecting Burst Setting Zener Voltage in t_{SET}	During t_{SET}, V_{CC} = 15 V, V_{LINE} = 10 V	I_{SET}	1.6	2.7	3.8	mA
Burst-mode Level 0 Set up Voltage	During t_{SET}	$V_{LINE-SET0}$	12.4			V
Burst-mode Level 1 Set up Voltage	During t_{SET}	$V_{LINE-SET1}$	9.3		10.6	V
Burst-mode Level 2 Set up Voltage	During t_{SET}	$V_{LINE-SET2}$			7.9	V
Sourcing Current for Setting Burst-mode Level when Line Detection is Disabled	V_{LINE} = 0 V before V_{CC} is charged to $V_{CC-START}$	I_{BURST}	9.4	10	10.6	μA
LINE-pin Voltage to Burst-mode Level Attenuation when Line Detection is Disabled (Note 9)		$A_{V-BURST}$		1/3		V/V
Protections: Over-Voltage Protection (OVP)						
Over-Voltage Protection Threshold Voltage for VCC−pin		V_{CC-OVP}	23.0	24.5	26.0	V
Delay time for OVP (Note 9)		t_{D-OVP}		6.0		μs
Protections: Over-Load Protection (OLP)						
OLP-Triggering Threshold Voltage on COMP−pin		V_{OLP}	3.3	3.6	3.9	V
Delay Time for OLP	$V_{COMP} > V_{OLP}$ after Soft-start Time	t_{D-OLP}	30	60	90	ms

ELECTRICAL CHARACTERISTICS (continued)
T_J = −40 to +125°C and V_{CC} = 14 V unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Abnormal Over-Current Protection (AOCP)						
AOCP Monitoring duration after t_{LEB} (Note 9)		t_{AOCP}		150		ns
Threshold Drain Current for Triggering AOCP (Note 9)		I_{AOCP}		I_{LIM}		mA
Number of pulse for AOCP to skip switching operation for $N_{AOCP-HALT}$ times (Note 9)		$N_{AOCP-TRIG}$		2		times
Number of skipped pulses after $N_{AOCP-TRIG}$ is satisfied (Note 9)		$N_{AOCP-HALT}$		7		times
Number of Pulse for Satisfying $N_{AOCP-TRIG}$ to Trigger Auto-restart Protection (Note 9)		$N_{AOCP-COUNT}$		3		times
Protections: Line Detection (BI, BO, LOVP)						
Brown-out (BO) Threshold Voltage on LINE−pin		$V_{LINE-BO}$	0.80	0.85	0.90	V
Brown-in (BI) Threshold Voltage on LINE−pin		$V_{LINE-BI}$	0.95	1	1.05	V
Hysteresis between BI and BO	$V_{LINE-BI} - V_{LINE-BO}$	$\Delta V_{LINE-BIBO}$	0.09	0.15	0.21	V
Delay Time for Brown−out (Note 9)		t_{BO}		100		ms
Threshold Voltage for Line Over−Voltage Protection (LOVP)		$V_{LINE-OVP}$	4.3	4.5	4.7	V
Recovering Level for LOVP		$V_{LINE-OVP-RECOVER}$	4.2	4.4	4.6	V
Hysteresis Voltage for LOVP	$V_{LINE-OVP} - V_{LINE-OVP-RECOVER}$	$\Delta V_{LINE-OVP}$	0.05	0.1	0.15	V
Delay Time for LOVP (Note 9)		$t_{LINE-OVP}$		2		μs
Protections: Thermal Shutdown						
Junction Temperature to Trigger Thermal Shutdown (Note 9)		T_{SD}		147		°C
Junction Temperature for Resuming from Thermal Shutdown (Note 9)		$T_{RECOVER}$		95		°C
Total Device Section						
Operating Supply Current (Control Part in Burst−mode)	V_{COMP} = 0 V, V_{DRAIN} = 12 V, R_{DRAIN} = 500 Ω	I_{OP1}		0.9	1.2	mA
Operating Supply Current	V_{COMP} = 3.2 V, V_{DRAIN} = 12 V	I_{OP2}		1.7	2.0	mA
VCC-pin current at startup condition	V_{CC} = 14.9 V, V_{COMP} = 3.6 V (Before V_{CC} Reaches $V_{CC-START}$)	I_{START}		170	205	μA
Startup Charging Current (JFET saturation current)	V_{CC} = 0 V, V_{DRAIN} = 40 V	I_{CH}	1.2	4		mA
Minimum DRAIN-pin Voltage to Start Operation (Note 10)	V_{CC} = V_{COMP} = 0 V	V_{START}			40	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
8. Evaluated in the typical flyback application board, T_A = 25°C
9. This parameter is not tested in production, but verified by design/characterization.
10. It is guaranteed that I_{CH} can charge V_{CC} up to $V_{CC-START}$ if DRAIN-pin voltage is higher than V_{START}.

TYPICAL CHARACTERISTICS

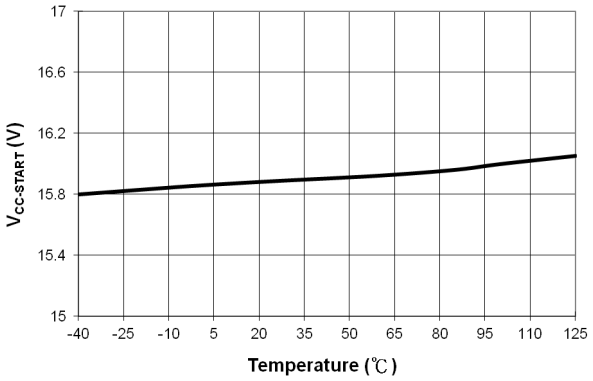


Figure 3. $V_{CC-START}$ vs. Temperature

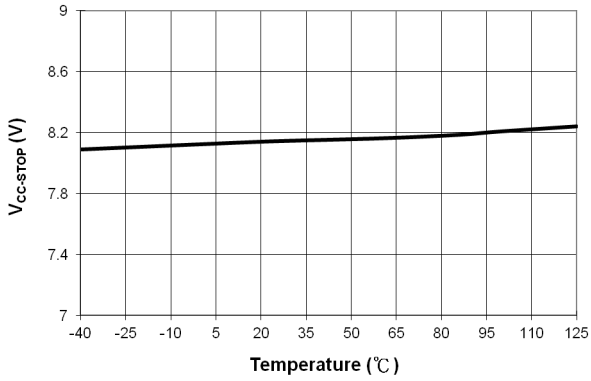


Figure 4. $V_{CC-STOP}$ vs. Temperature

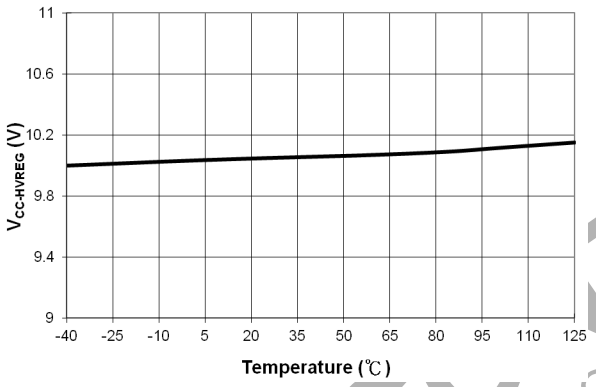


Figure 5. $V_{CC-HVREG}$ vs. Temperature

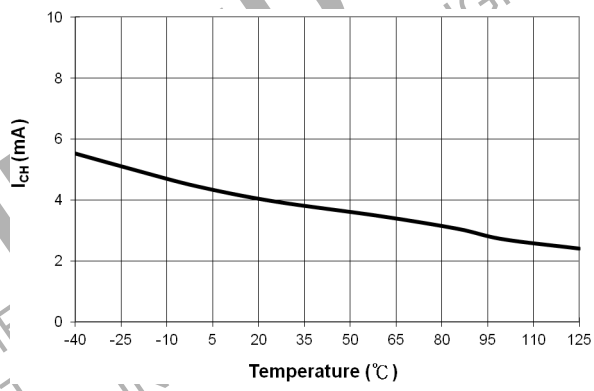


Figure 6. I_{CH} vs. Temperature

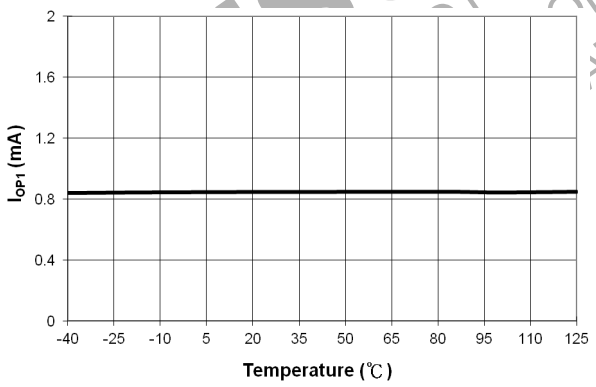


Figure 7. FSL5x8H I_{OP1} vs. Temperature

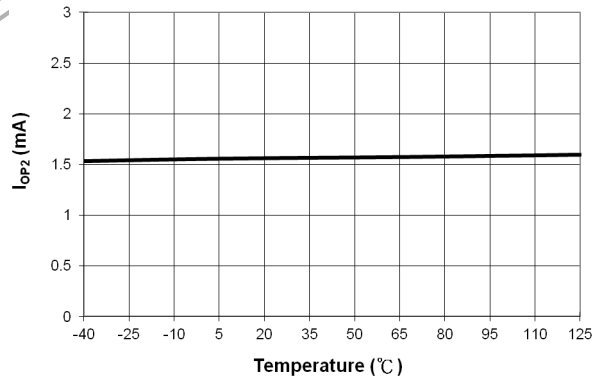


Figure 8. FSL5x8H I_{OP2} vs. Temperature

TYPICAL CHARACTERISTICS

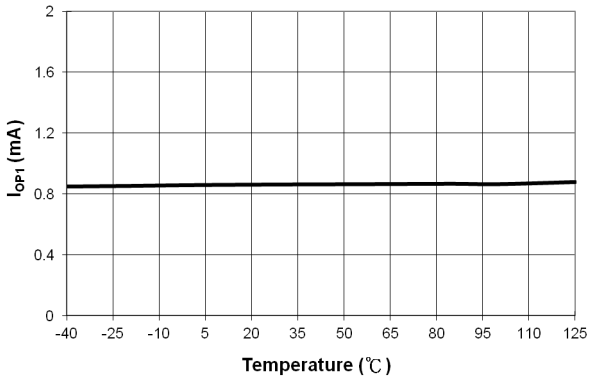


Figure 9. FSL5x8A I_{OP1} vs. Temperature

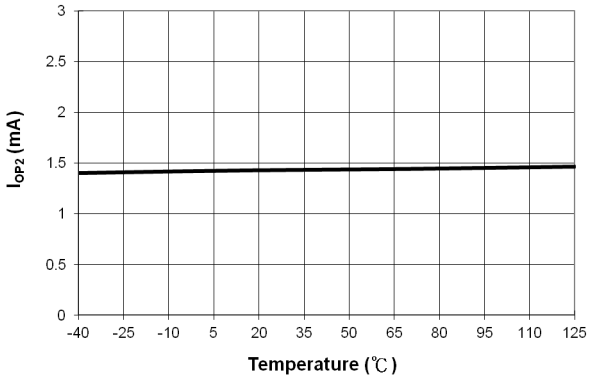


Figure 10. FSL5x8A I_{OP2} vs. Temperature

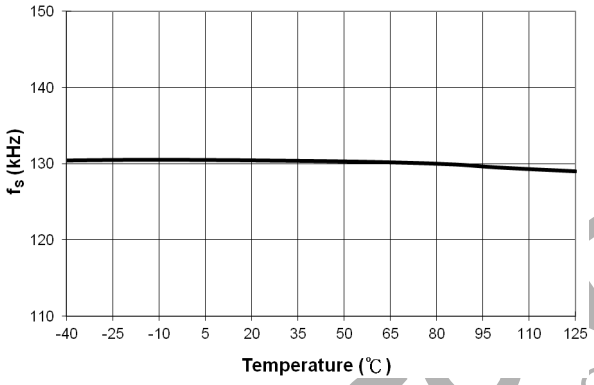


Figure 11. FSL5x8H f_S vs. Temperature

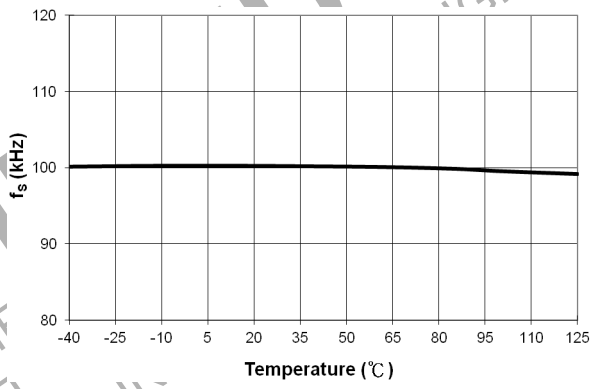


Figure 12. FSL5x8A f_S vs. Temperature

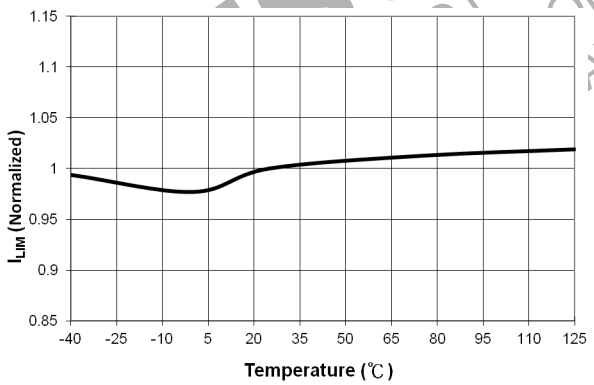


Figure 13. FSL518H I_{LIM} (Normalized to 25°C) vs. Temperature

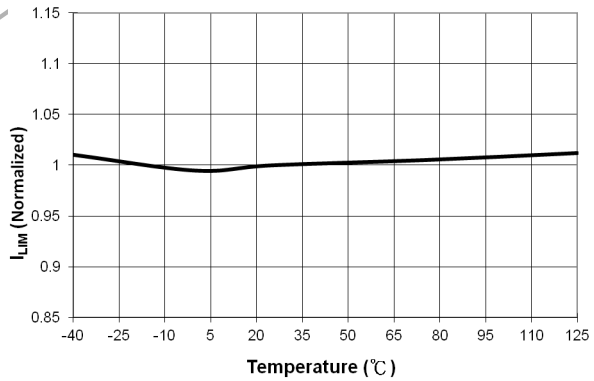


Figure 14. FSL518A I_{LIM} (Normalized to 25°C) vs. Temperature

TYPICAL CHARACTERISTICS

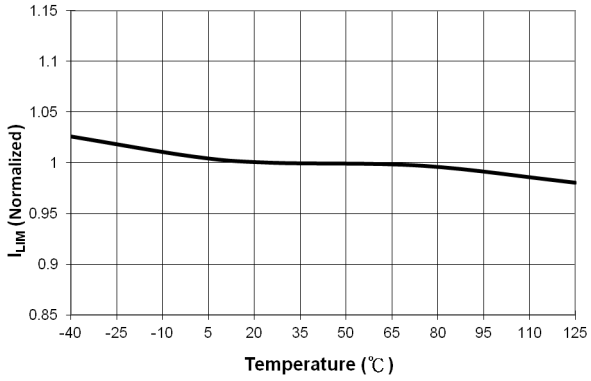


Figure 15. FSL538H I_{LIM} (Normalized to 25°C) vs. Temperature

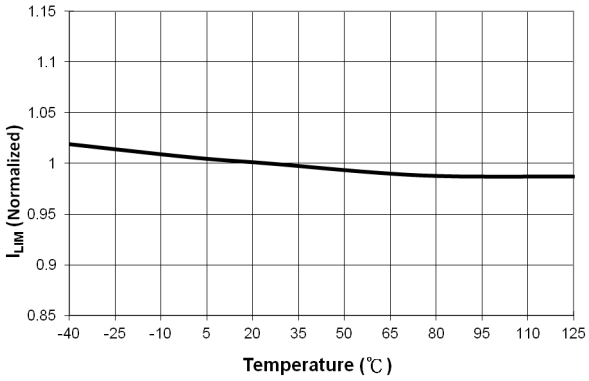


Figure 16. FSL538A I_{LIM} (Normalized to 25°C) vs. Temperature

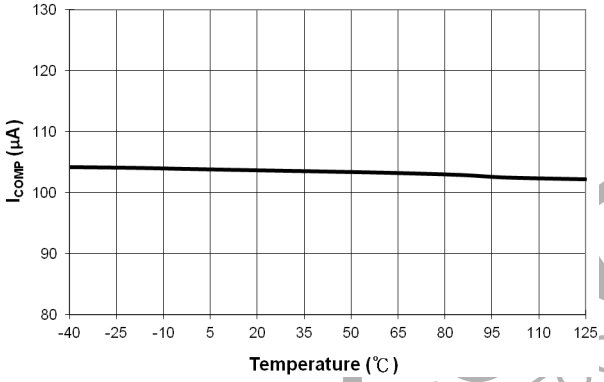


Figure 17. I_{COMP} vs. Temperature

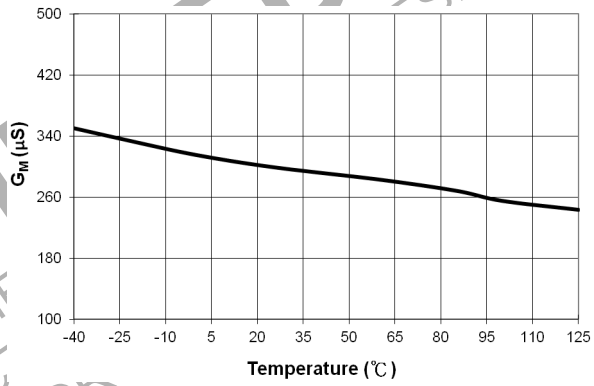


Figure 18. G_M vs. Temperature

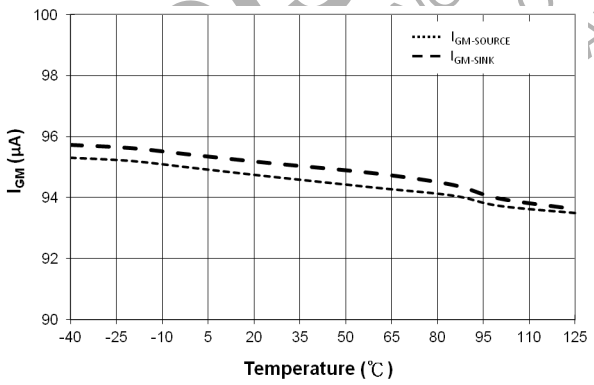


Figure 19. I_{GM} vs. Temperature

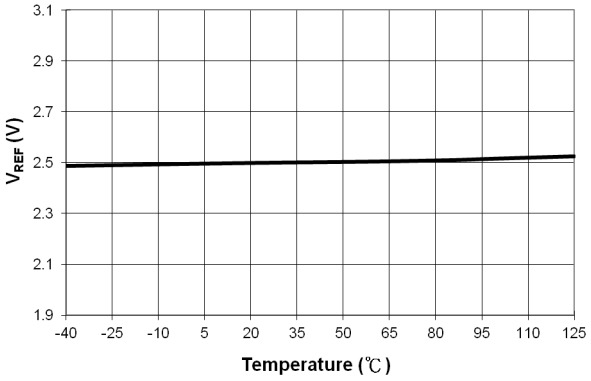


Figure 20. V_{REF} vs. Temperature

TYPICAL CHARACTERISTICS

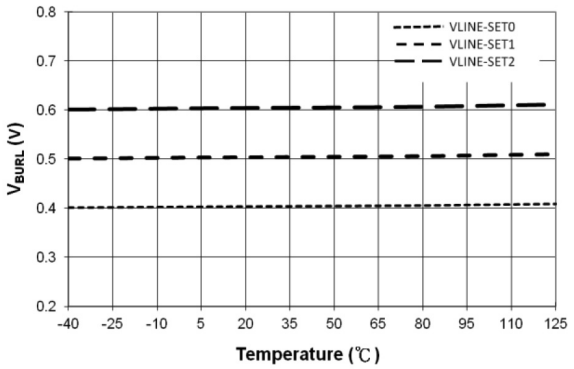


Figure 21. V_{BURL} vs. Temperature

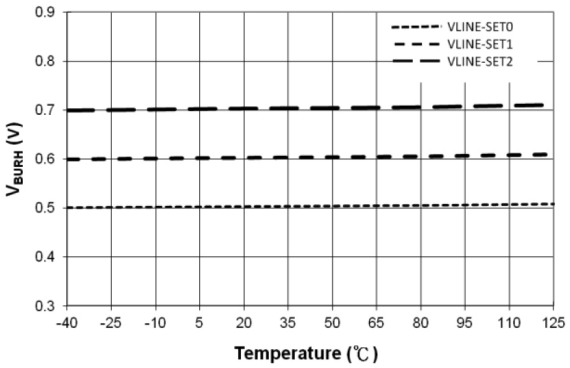


Figure 22. V_{BURH} vs. Temperature

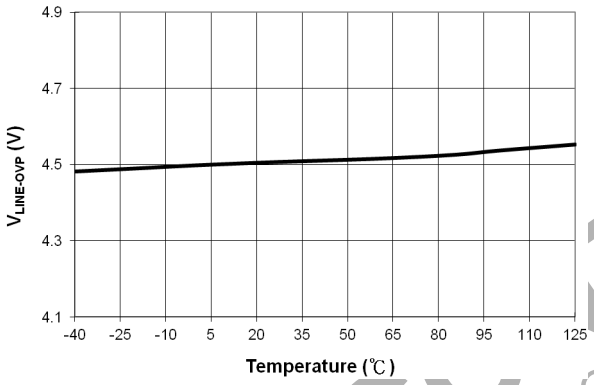


Figure 23. $V_{LINE-OVP}$ vs. Temperature

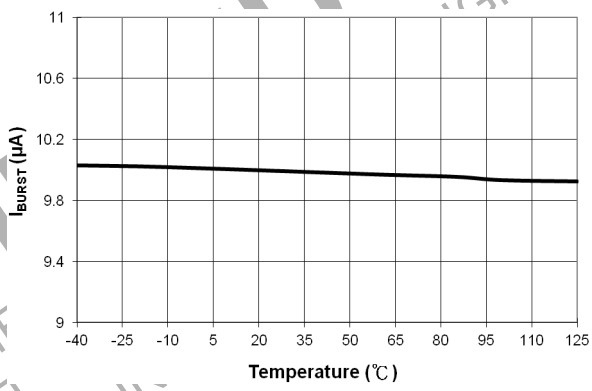


Figure 24. I_{BURST} vs. Temperature

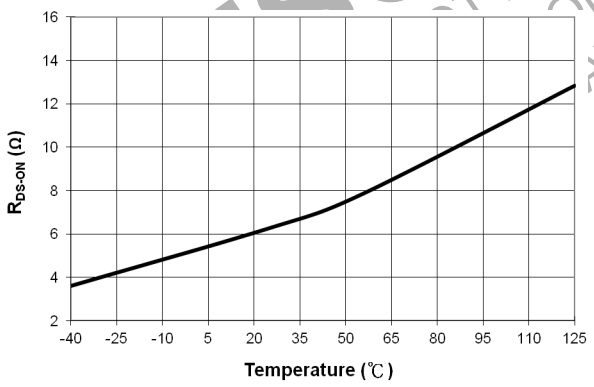


Figure 25. FSL518H/A $R_{DS(ON)}$ vs. Temperature

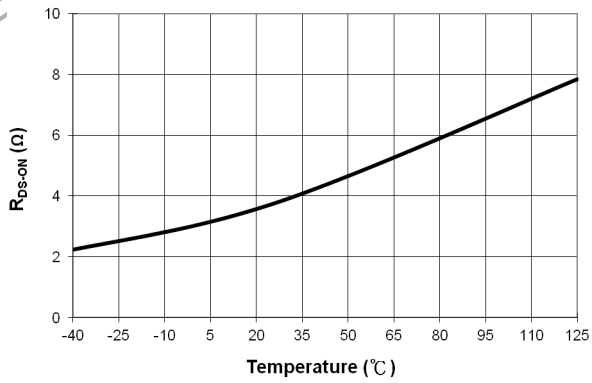


Figure 26. FSL538H/A $R_{DS(ON)}$ vs. Temperature

TYPICAL CHARACTERISTICS

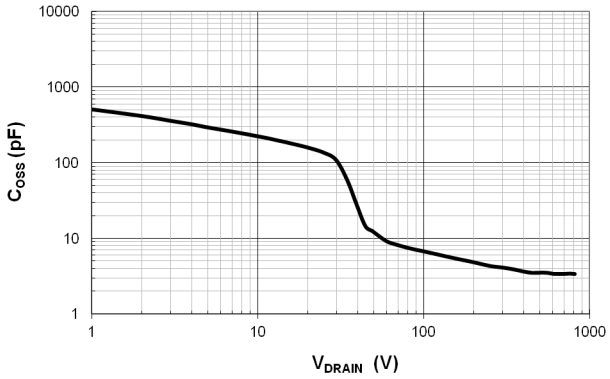


Figure 27. FSL518H/A C_{OSS} vs. V_{DRAIN}

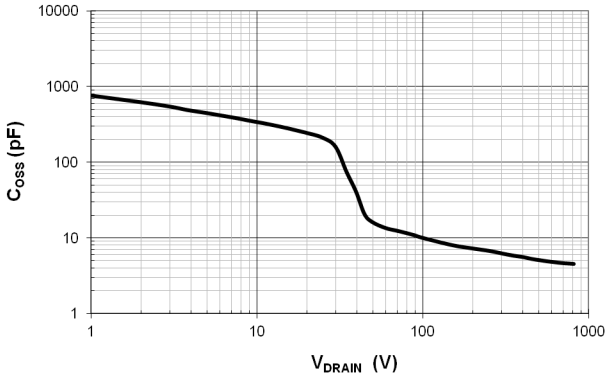


Figure 28. FSL538H/A C_{OSS} vs. V_{DRAIN}

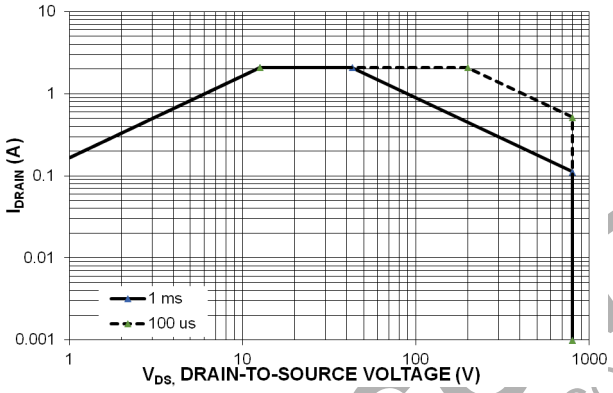


Figure 29. FSL518H/A Safe Operating Range

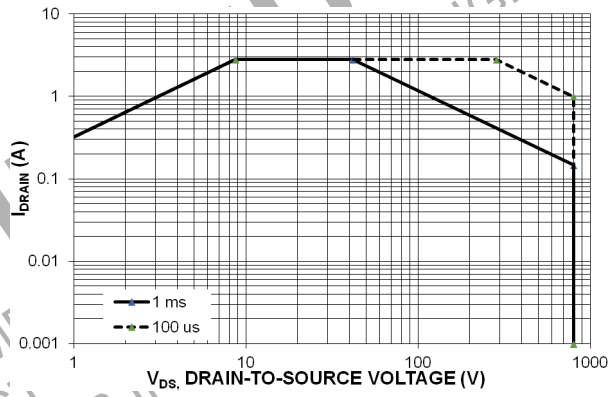


Figure 30. FSL538H/A Safe Operating Range

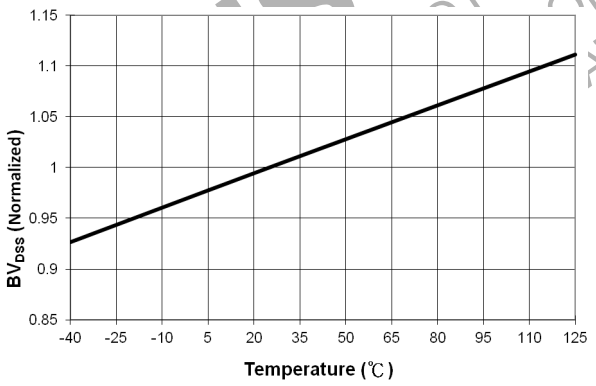


Figure 31. FSL518H/A BV_{DSS} vs. Temperature

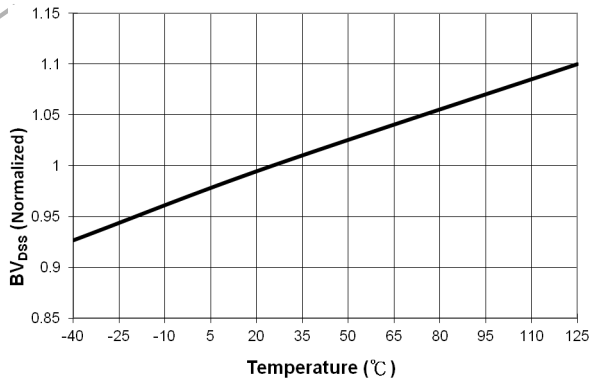


Figure 32. FSL538H/A BV_{DSS} vs. Temperature

TYPICAL CHARACTERISTICS

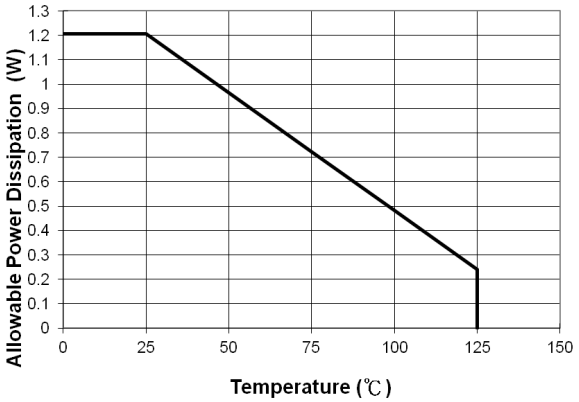


Figure 33. FSL5x8H/A Power Dissipation vs. Temperature

APPLICATION INFORMATION

HV Current Source for V_{CC} Start up and V_{CC} Regulation

The HV current source utilizes voltage on DRAIN pin to charge capacitor on VCC pin. This current source is activated during start-up and provides operating current when V_{CC} is lower than $V_{CC-HVREG}$. Thanks to V_{CC} start-up function, no external start-up circuitry is needed. The HV current source is disabled when V_{CC} voltage is charged to $V_{CC-START}$.

V_{CC} regulation also helps avoiding start-up failure during soft-start and keeps FSL5x8 operating to count auto-restart delay time (t_{AR}) in protection mode, as illustrated in Figure 34. It also enables the use of smaller capacitance for V_{CC} biasing. The V_{CC} regulation is not functional when the external bias is higher than $V_{CC-HVREG}$.

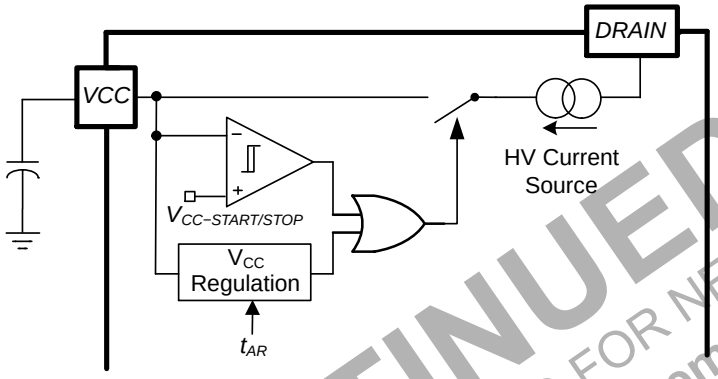


Figure 34. V_{CC} Start Up and V_{CC} Regulation

Initial Setting for Line Detection and Adjusting Burst-mode Operation

LINE pin is used for both input-voltage detection and burst-mode setting. When a voltage divider is connected between bulk capacitor and LINE pin, a Zener diode connected to LINE pin will allow to set level of burst-mode operation. If there is no voltage divider, the line-detection function is disabled and burst-mode operation level is set linearly by simply connecting a resistor between LINE pin and GND pin. In order to avoid interference from switching noise, connecting a ceramic capacitor to LINE pin is recommended.

When line detection is enabled, voltage on LINE pin is monitored to offer brown-in (BI), brown-out (BO) and line over-voltage protections (LOVP).

With I_{BURST}, V_{LINE} reflects resistance of the external resistor. FSL5x8 adjusts burst-mode operation threshold based on real-time V_{LINE} level. Please refer to burst threshold setting table for LINE pin configuration and settings.

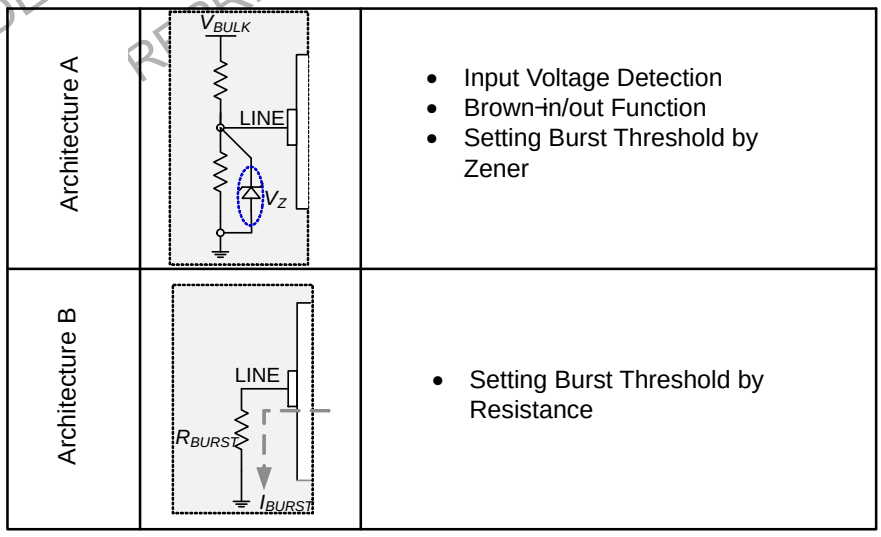


Figure 35. Architecture of LINE-pin Setting

BURST THRESHOLD SETTING TABLE

	Line Detection Enable/Disable	V_{LINE} (V)	V_{BURH}/V_{BURL} (V)
Architecture A	Enable	12.4 V < V_Z	0.5 / 0.4
		9.3 V < V_Z < 10.6 V	0.6 / 0.5
		V_Z < 7.9 V	0.7 / 0.6
Architecture B	Disable	0.9 V < $I_{BURST} \times R_{BURST}$ < 1.2 V	0.5 / 0.4
		1.2 V < $I_{BURST} \times R_{BURST}$ < 3.6 V	$A_{V\text{-}BURST} \times (I_{BURST} \times R_{BURST}) + 0.1$ /$A_{V\text{-}BURST} \times (I_{BURST} \times R_{BURST})$

Initial Setting for Configuration of Feedback Regulation

Being simultaneous to the initial setting of LINE-pin functions, configuration of feedback regulation is also decided based on peripheral circuitry to FB pin. If a voltage divider is connected to FB pin, the IC will regulate output voltage by referring to the reference voltage, V_{REF} of transconductance error amplifier.

In the case that external error amplifier is used for output regulation, simply connect FB pin to GND pin. The external output regulation circuitry will sinks I_{COMP} (100 μA) to control PWM duty cycle for accuracy output regulation.

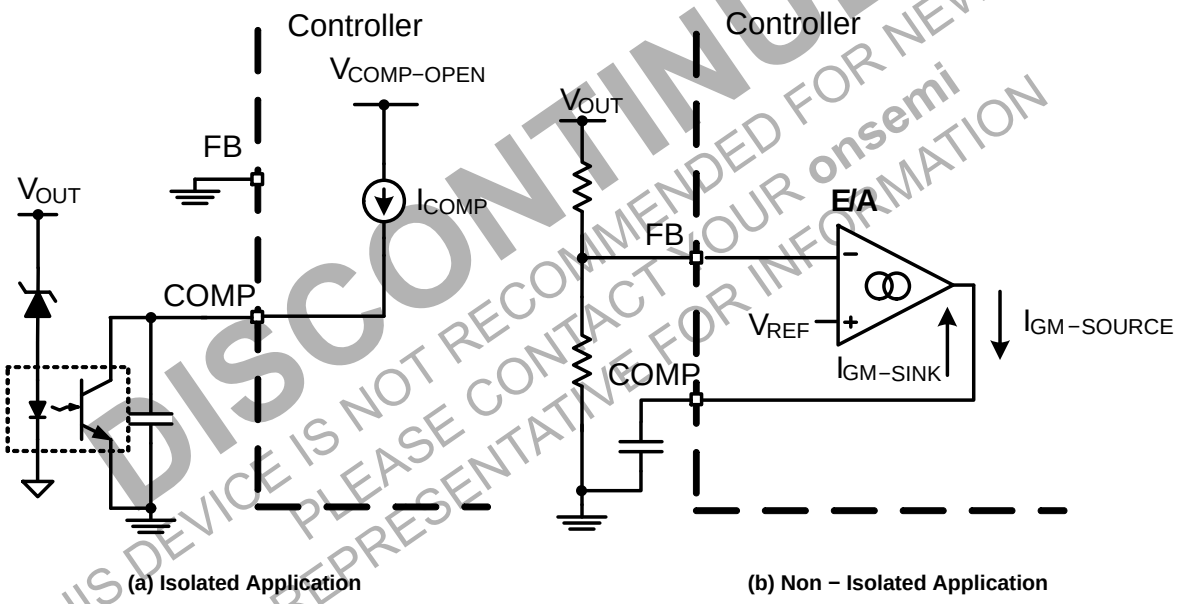


Figure 36. Isolated vs. Non-Isolated Application

Advanced Soft-Start Operation

After V_{CC} is charged to $V_{CC\text{-}START}$ and all settings about LINE-pin and FB-pin functions are done, switching operation can be initiated with a soft-start period. For soft−start period of 10 ms, both drain current and switching frequency limits are settled to target value gradually as shown in Fig. 37. Thus, output voltage will be increased smoothly and the voltage stresses in switching devices can be minimized.

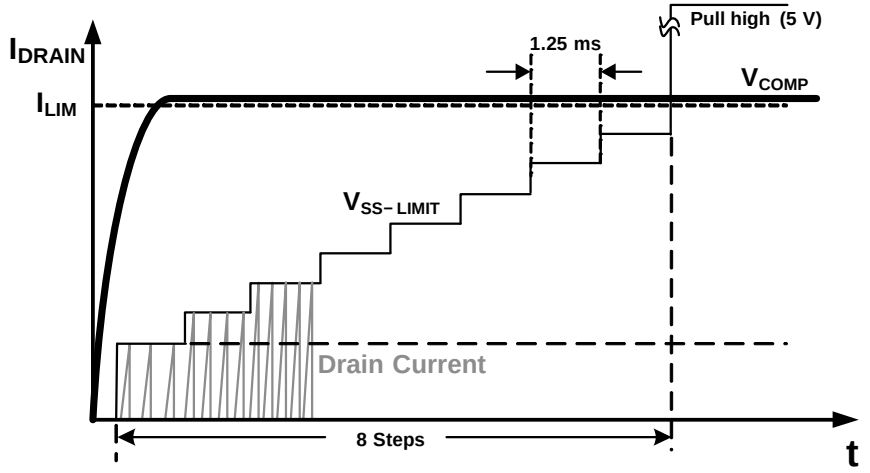


Figure 37. Soft-start Operation

Main Control Frequency Reduction

Operating frequency of switching operation is synchronized with COMP-pin voltage, V_{COMP}. When V_{COMP} drops, operating frequency will also decrease. This helps reducing switching losses and thus improve light-load efficiency operation. The operating frequency will not be decreased below 22-kHz so acoustic noise can be avoided.

PWM Control

The FSL5x8 operates with peak−current mode to regulate output voltage. The duty cycle of PWM is determined by comparing drain peak current and V_{COMP}. The V_{COMP} can be controlled by either the input signal of error amplifier or the signal delivered via opto−coupler and feedback loop for output regulation.

Slope Compensation

Built-in slope compensation is added into the PWM procedure when duty cycle is higher than 45%. It helps to avoid sub-harmonic oscillation of peak-current control.

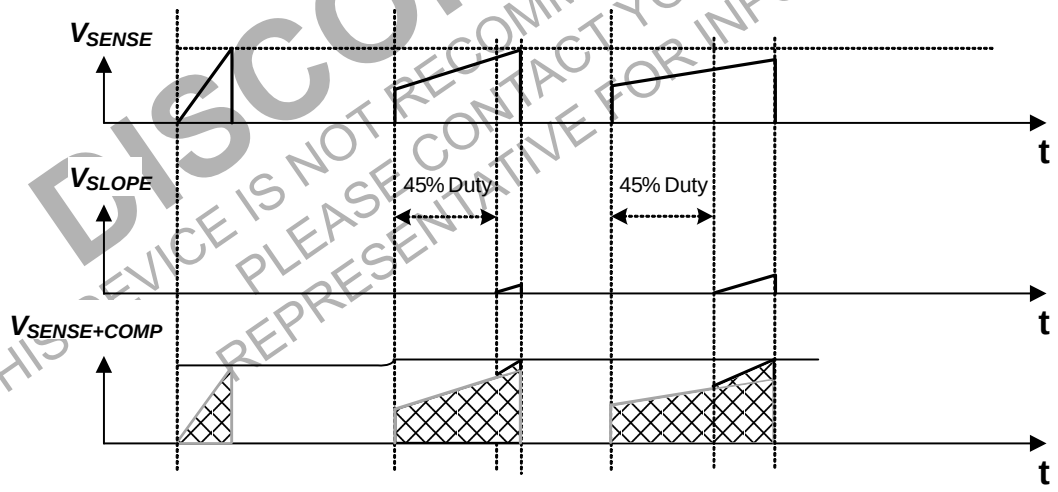


Figure 38. Slope Compensation

Burst−mode Operation

As loading of the power converter decreases, V_{COMP} decreases, thus reducing switching frequency of the oscillator. When minimum operating frequency is reached, to further reduce delivered output power, the device goes into burst−mode. In burst−mode, switching operation is halted when V_{COMP} is lower than V_{BURL} and resumed when V_{COMP} is higher than V_{BURH}. By skipping un-needed switching cycles, the FSL5x8 drastically reduced the power wasted during light load conditions.

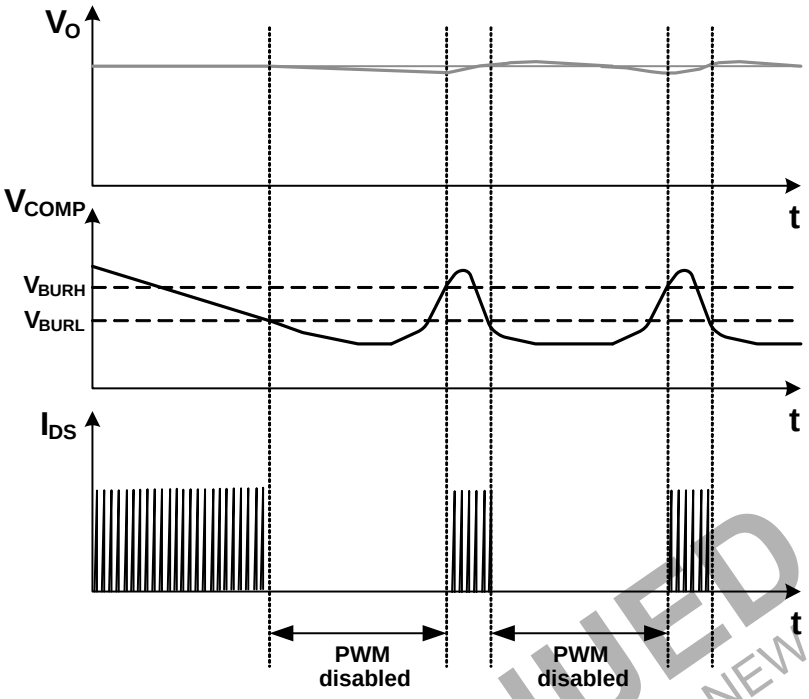


Figure 39. Burst−mode Behavior

V_{BURL} and V_{BURH} can be adjusted LINE-pin voltage detected. It is provided for tuning light load efficiency and acoustic noise. By adjusting V_{BURL}, minimum peak value of drain current of each switching cycle is adjusted as described in Equation 1.

$$I_{DRAIN.PEAK.BURL} = \frac{V_{BURL}}{4 \cdot 0.6} \cdot I_{LIM} \quad \text{(eq. 1)}$$

Line Compensation

Propagation delay in turning off power MOSFET makes drain current exceed current limit by an amount that related to slope of drain current. The device adjusts its internal current-limit reference voltage according to duty cycle to compensate the effect of propagation delay. As a result, the delivered output power is kept under control across different input voltage conditions.

Protections

Over Load Protection (OLP)

V_{COMP} will be pulled higher than V_{OLP} when drain current hits current limit and switching frequency operates at its highest range. If the condition continues for t_{D-OLP}, OLP will be triggered and switching operation is stopped as shown in Fig. 40.

The figure also shows typical protection mode behavior of the IC. The operation current is supplied by HV current source for t_{AR} that can extend the restart period to reduce average power dissipation when fault is still present. After t_{AR}, V_{CC} drops to $V_{CC-STOP}$ to reset protective operation and then, controller will be restarted.

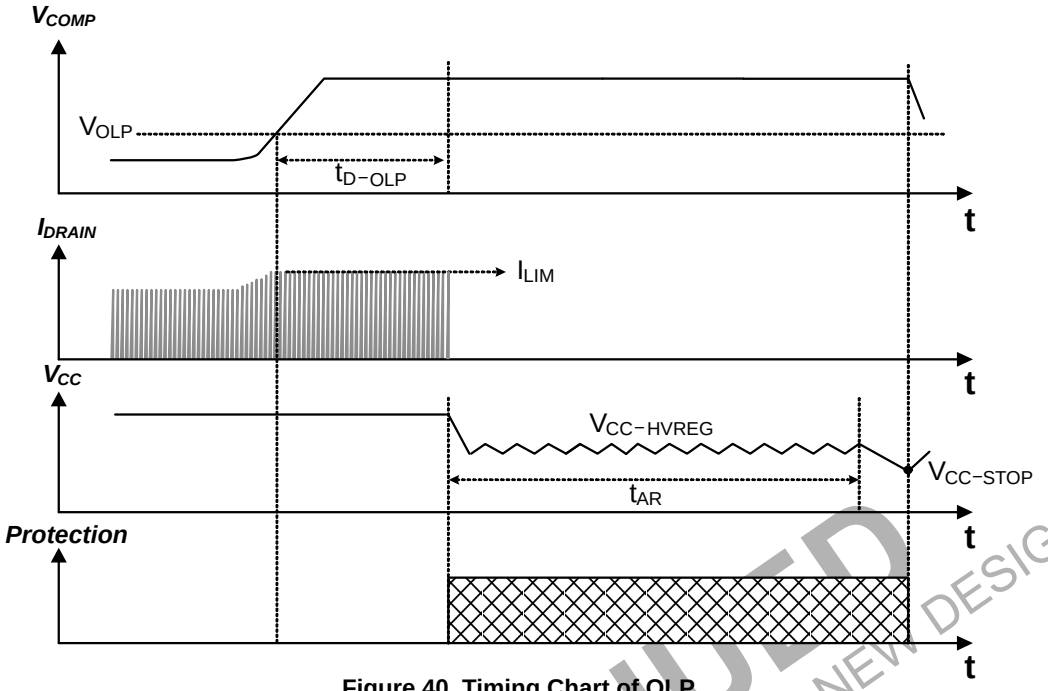


Figure 40. Timing Chart of OLP

Over Voltage Protection (OVP)

A malfunction of voltage-feedback circuitry for output regulation in power converter could result in excessive energy delivered to output. In this condition, both output voltage and V_{CC} can be increased by unstable operation, and OVP will be triggered after delay time t_{D-OVP} when V_{CC} rises above V_{CC-OVP}.

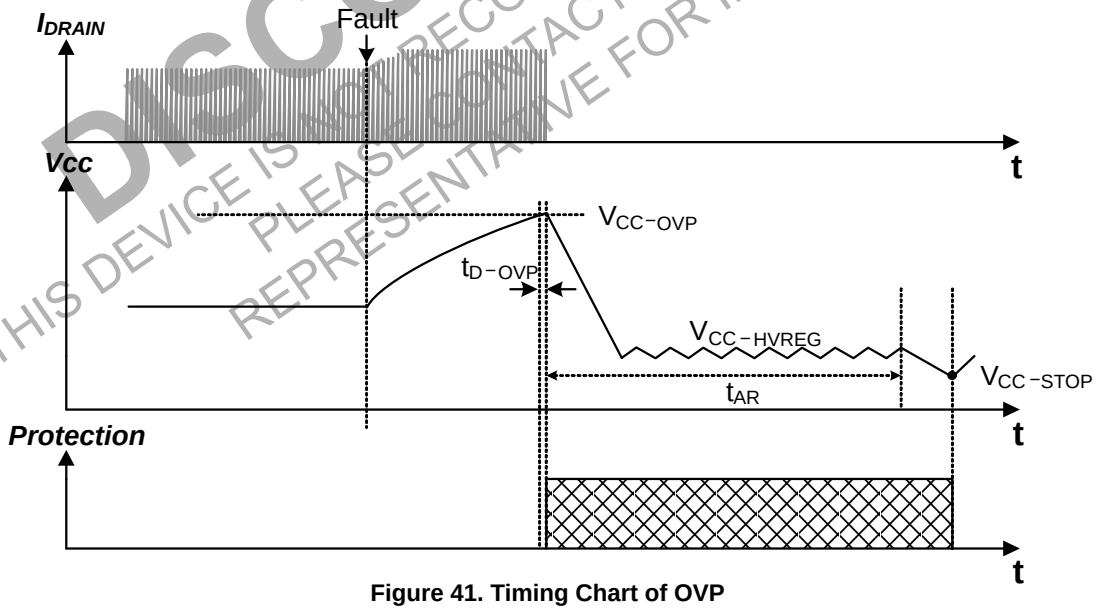


Figure 41. Timing Chart of OVP

Abnormal Over-Current Protection (AOCP)

When the secondary-side rectifier diodes or the transformer windings are shorted, a steep drain current with extremely high di/dt will flow through the MOSFET during the minimum turn-on time. Under this condition, each switching cycle generates very high current stress on power MOSFET. The controller monitors drain current within a limited leading-edge time duration t_{LEB} + t_{AOCP} of each switching cycle. If drain current exceeds current limit for a few consecutive switching cycles, $N_{AOCP-TRIG}$, switching will be stopped for number of pulses, $N_{AOCP-HALT}$. If the fault condition is met for three times, $N_{AOCP-COUNT}$, the controller goes into protection mode as shown in Fig. 42.

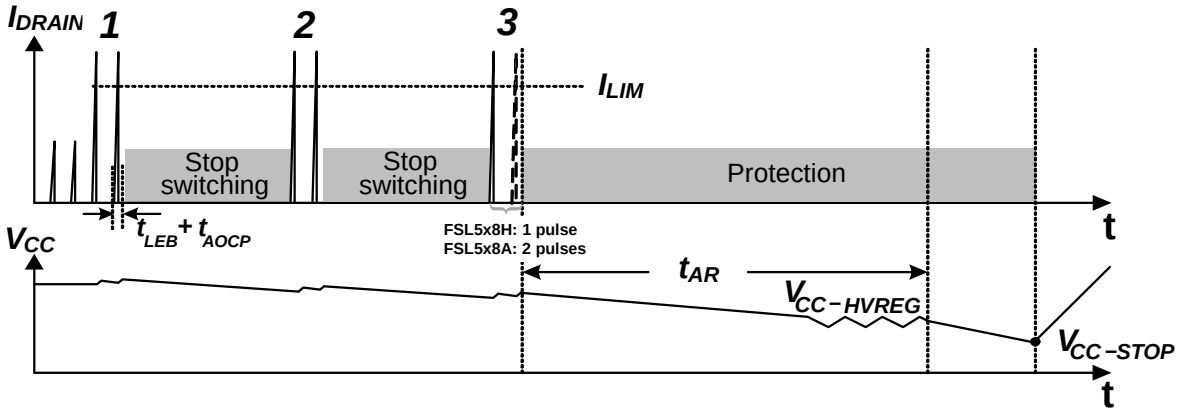


Figure 42. Timing Chart of AOCP

Brown−in, Brown−out (BI/BO) and Line Over-Voltage Protection (LOVP)

When a voltage divider is connected between LINE pin and input bulk capacitor, line-detection function is enabled and V_{LINE} reflects peak of AC input voltage. If V_{LINE} is below $V_{LINE-BI}$ after initial setting, switching operation will not be initiated until V_{LINE} reaches $V_{LINE-BI}$. If V_{LINE} is lower than $V_{LINE-BO}$ for t_{BO} during normal operation, brown-out will be triggered and the controller will go into protection mode. If V_{LINE} is higher than $V_{LINE-OVP}$, switching operation is halted until V_{LINE} drops down below $V_{LINE-OVP-RECOVER}$. Both recovering from LOVP or after BI, the controller performs a soft start sequence.

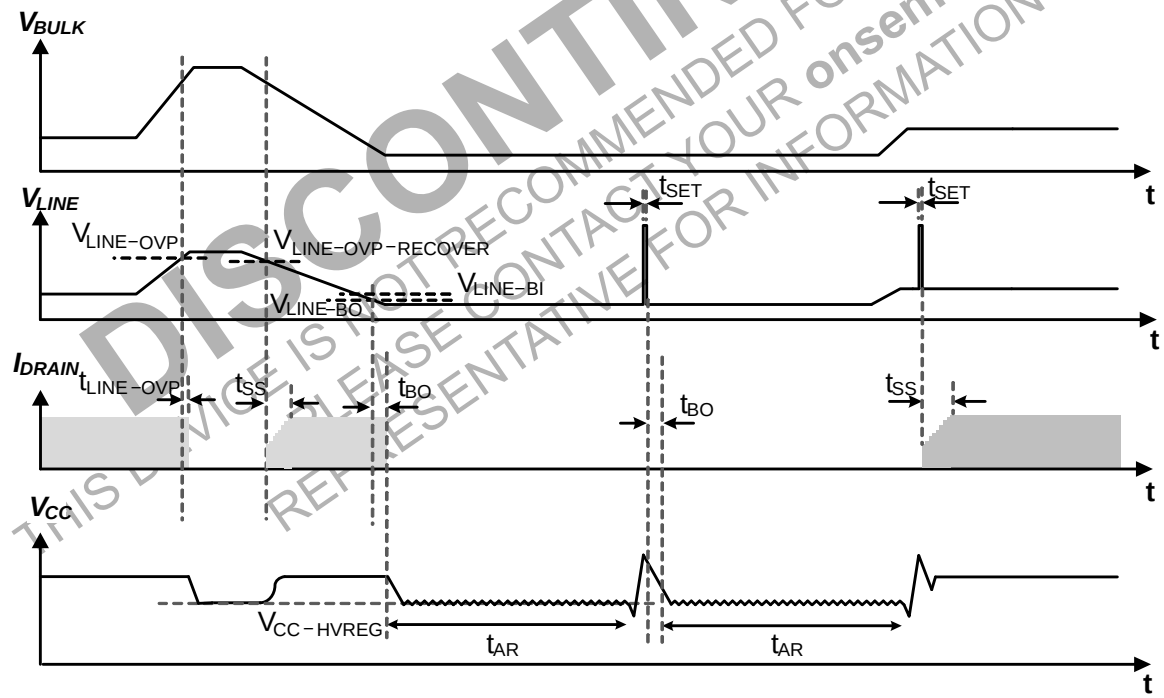


Figure 43. LOVP, Brown-out and Brown-in Behavior

Thermal Shutdown (TSD)

Since SENSEFET and controller are integrated in the same package, it is easier for the controller to detect temperature inside the package. When junction temperature exceeds shut-down temperature, T_{SD}, thermal shutdown is activated. The controller will go into protection mode after thermal shutdown. If temperature is not lower than $T_{RECOVER}$, switching operation will not be resumed.

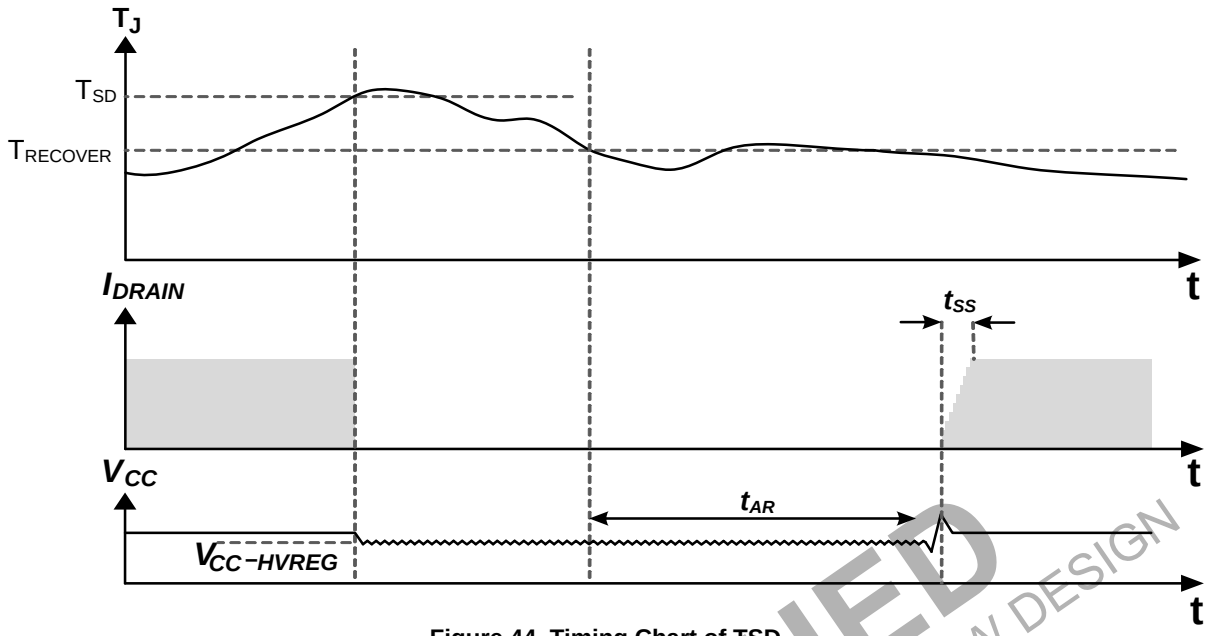


Figure 44. Timing Chart of TSD

DESIGN CONSIDERATIONS

Peripheral Components

While designing flyback converters using FSL5x8H/A, there are some design considerations on selecting value and rating of components and PCB (Printed Circuit Board) layout as the following.

- Input/Output Capacitor

It is typical to select the input capacitor as 2~3 μF per watt of peak input power for universal input range (85−265 V_{RMS}) and 1 μF per watt of peak input power for European high input voltage range (195−265 V_{RMS}).

The minimum DC link voltage is obtained as:

$$V_{DC_{min}} = \sqrt{2 \cdot \left(V_{line_{min}}\right)^2 - \frac{P_{in} \cdot (1 - D_{ch})}{f_L \cdot C_{DC}}}, \qquad \text{(eq. 2)}$$

where D_{ch} is the DC link capacitor charging duty ratio which is typically about 0.2. f_L is line voltage frequency.

Considering the output voltage ripple, capacitance at the output terminal can be determined as the following. For better voltage ripple at output terminal, low ESR (Effective Series Resistance) type capacitor is recommended.

$$C_{OUT} = \frac{0.25 \cdot I_{OUT}}{V_{OUT-ripple} \cdot f_{min}}, \qquad \text{(eq. 3)}$$

where I_{OUT} is a max output load current, $V_{OUT\text{-}ripple}$ is deviation of a ripple voltage and f_{min} should minimum freqeuncy between operating frequency deviation.

- V_{CC} Capacitance

FSL5x8 includes HV start-up circuit providing startup current, which determine startup time. It can be calculated with I_{CH} and V_{CC} capacitance. The typical value of V_{CC} capacitor is selected in a range of 10 to 47 μF. It is recommended that V_{CC} capacitor and FSL5x8 should be placed as close as possible to reject noise decoupling.

$$\text{Start-up Time} = \frac{C_{VCC} \cdot V_{CC-START}}{I_{CH}}, \qquad \text{(eq. 4)}$$

- Consideration on Designing BI/BO/LOVP

Line input voltage can be detected for brown-in (BI), brown-out (BO) and input line over-voltage protection (LOVP) by connecting LINE pin with dividing resisters linking to input bulk capacitor. Each level of BI and LOVP can be determined as following. Meanwhile, $C_{LINE\text{-}F}$ should be choosen considering some noises on the line induced by switching of the main switch and etc. It is typical to select 3~5 times of time constant higher than switching frequency.

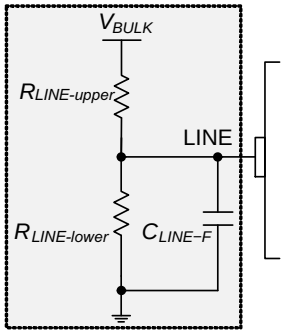


Figure 45. LINE Pin Settle for BI/BO/LOVP

$$\text{Brown-in AC Voltage} = V_{LINE-BI} \times \frac{R_{LINE-upper} + R_{LINE-lower}}{R_{LINE-lower}} \times \frac{1}{\sqrt{2}} \qquad \text{(eq. 5)}$$

$$\text{Line OVP AC Voltage} = V_{LINE-OVP} \times \frac{R_{LINE-upper} + R_{LINE-lower}}{R_{LINE-lower}} \times \frac{1}{\sqrt{2}} \qquad \text{(eq. 6)}$$

$$C_{LINE-F} = \frac{3}{\left(R_{LINE-upper} // R_{LINE-lower}\right) \cdot f_{SW}} \qquad \text{(eq. 7)}$$

- Selecting FB/COMP and Consideration when One of Both is Selected

For non-isolated converters, connects the output voltage divider to FB pin. For isolated converters, FB pin should be connected to GND, and the external feedback circuit should connect to COMP as well.

- Preventing Audible Noise

Even though the switching frequency of the FSL5x8 is above the range of human hearing, audible noise can be generated during transient or burst operation. In most flyback converters, the major noise sources are transformers and capacitors. Transformers produce audible noise, since they contain many physically movable elements, such as coils, isolation tapes and bobbins. The most effective way to reduce the audible noise in the transformer is to remove the possibility of physical movement of the transformer elements by using adhesive material or by varnishing.

Ceramic capacitors can also produce audible noise, because of their piezoelectric characteristics. By replacing the ceramic capacitor with a film capacitor, the audible noise can be reduced. Another way to lower audible noise is to reduce the snubber capacitor value,

which decreases the pulse current that charges the capacitor every time the FSL5x8 resumes switching operation in burst−mode.

For more information, please refer to AN−4148.

- Maximum Duty and Reflected Output Voltage

When MOSFET in FSL5x8 is turned off, the input voltage together with the reflected output voltage (V_{RO}) on primary winding of the transformer are imposed on MOSFET.

$$V_{DRAIN_{max}} = \sqrt{2} \cdot V_{line_{max}} + V_{RO} \quad \text{(eq. 8)}$$

$V_{linemax}$ is maximum ac-input voltage in r.m.s. value. V_{RO} is a function of maximum duty (D_{max}) and minimum DC-link voltage.

$$V_{RO} = \frac{D_{max}}{1 - D_{max}} \cdot V_{DC_{min}} \quad \text{(eq. 9)}$$

The designed D_{max} should not exceed FSL5x8's maximum duty raio specification, D_{MAX}. It is typical to have 70% of de-rating on $V_{DRAINmax}$ according to MOSFET's breakdown voltage. With 800 V of breakdown voltage in FSL5x8, more room are created to target higher D_{max}.

- Transformer Design Considerations

When D_{max} is assigned, turn ratio of the transformer has been decided.

$$n = \frac{N_P}{N_S} = \frac{V_{RO}}{V_{OUT} + V_F}, \quad \text{(eq. 10)}$$

where N_P and N_S stands for primary and secondary windings' turn ratio of the transformer, V_{OUT} stands for output voltage, and V_F stands for forward voltage of rectifying diode connecting to the secondary winding.

Inductance (L_m) of the primary winding can be obtained from input power (P_{in}) and switching frequency (f_{sw}), with ripple factor (K_{RF}) left to be decided. $K_{RF} \geq 1$ results in lower inductance and discontinuous-conduction-mode (DCM) design, which tend to have smaller switching loss. $K_{RF} < 1$ results in a continuous-conduction-mode (CCM) design. Which tend to be able to deliver more power with same maximum drain current.

$$L_m = \frac{\left(V_{DC_{min}} \cdot D_{max}\right)^2}{2 \times P_{in} \cdot f_{SW} \cdot K_{RF}} \quad \text{(eq. 11)}$$

The inductance value affects maximum drain current ($I_{DRAINPEAK}$), which should be limited by FSL5x8's I_{LIM} specification with some margin. Care needs to be taken when designing L_m and choosing part from FSL5x8 series.

$$I_{DRAIN_{PEAK}} = \frac{P_{in}}{V_{DC_{min}} \cdot D_{max}} = \frac{V_{DC_{min}} \cdot D_{max}}{2 \cdot L_m \cdot f_{SW}} \quad \text{(eq. 12)}$$

- Clamping Circuit for internal MOSFET

Due to parasitic or leakage inductance, it is inevitable that voltage on DRAIN pin of MOSFET shows some spikes during switching off. A clamping circuit is generally implemented if the spike can be so high that makes DRAIN voltage possibly exceeds MOSFET's breakdown voltage, BV_{DSS}. The clamping circuit can be RCD snubber or transient-voltage suppressor. In both cases, the design target is to clamp the reflected voltage that appears across primary winding with a clamping voltage V_{clamp}.

V_{clamp} should be set up properly considering power loss and BV_{DSS} of MOSFET. V_{clamp} is way too high, MOSFET is likely to get damage at maximum input voltage. Whereas, too low one could cause power loss increasing at the clamp circuit. Generally, value in 2~2.5 times of VRO is usually chosen. Additionally, it should not exceed over 90% of BV_{DSS}.

$$\sqrt{2} \cdot V_{line_{max}} + V_{clamp} \leq 90\% \cdot BV_{DSS} \quad \text{(eq. 13)}$$

AN−4137 and AN−4140 provide detailed flyback converter, transformer, and snubber design information. A design tool with accompanying manual is also made for FSL5x8 series.

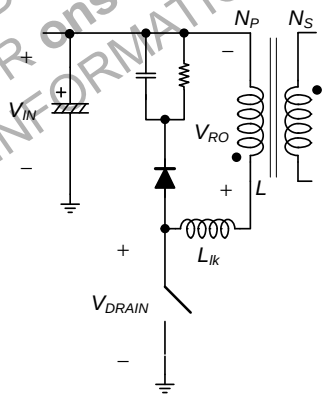


Figure 46. Magnetic Component and RCD Snubber

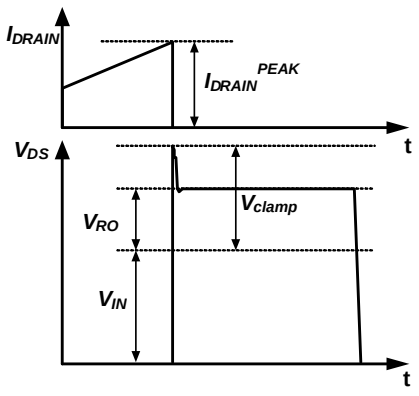


Figure 47. Typical Waveform of DRAIN Current and Voltage

PCB Layout Recommendations

Hereafter are a few hints that would help designers to make their SMPS working better.

- High-frequency switching current/voltage makes PCB layout a very important design issue. Good PCB layout minimizes EMI (Electromagnetic Interference) and helps the power supply survive during surge/ESD (ElectroStatic Discharge) tests.
- To improve EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor C_{DC} as close as possible.
- The high-frequency current loop is formed from the beginning of bridge rectifier, C_{DC}, power transformer, Integrated MOSFET and return to GND of C_{DC}. The area enclosed by this current loop should be designed as small as possible to reduce conduction and radiation noise. Keep the traces (especially **2a** → **2b** → **1**) short, direct, and wide. High-voltage traces related the drain of MOSFET and RCD snubber should be kept far way from control circuits to prevent unnecessary interference. If a heatsink is used for MOSFET, connect this heatsink to power ground.
- As indicated by **2a**, the ground of control circuits should be connected first, then to other circuitry.
- Place C_{Vcc} as close to VCC pin of the FSL5x8H/A as possible for good decoupling. It is recommended to use a few of micro-farad capacitor and 100 nF ceramic capacitor for high frequency noise decoupling as well.

There are some suggestions for grounding connection.

- GND: There are two kinds of GND in power conversion board and should be separated for avoiding interference and better performance.
- Regarding the ESD discharge path, the charges go from secondary, through the transformer stray capacitance, to GND first, and back to mains. It should be noted that control circuits should not be placed on the discharge path. Point discharge for common choke can decrease high-frequency impedance and increase ESD immunity.
- 3 should be a point-discharger route to bypass the static electricity energy. It is suggested to map out this discharge route.
- Should a Y-cap be required between primary and secondary, connect this Y-cap to the positive terminal of C_{DC}. If this Y-cap is connected to primary GND, it should be connected to the negative terminal of C_{DC} (GND) directly. Point discharge of this Y-cap helps for ESD; however, the creepage between these two pointed ends should be at least 5 mm according to safety requirements.

Thermal Considerations

Power MOSFET dissipates heat during switching operation. If chip temperature exceed T_{SD}, thermal shutdown would be triggered and FSL5x8 stops operating to protect itself from damage. The path of lowest thermal impedance from FSL5x8's chip to external are DRAIN pins. It is recommended to increase area of connected copper to DRAIN pin as much as possible.

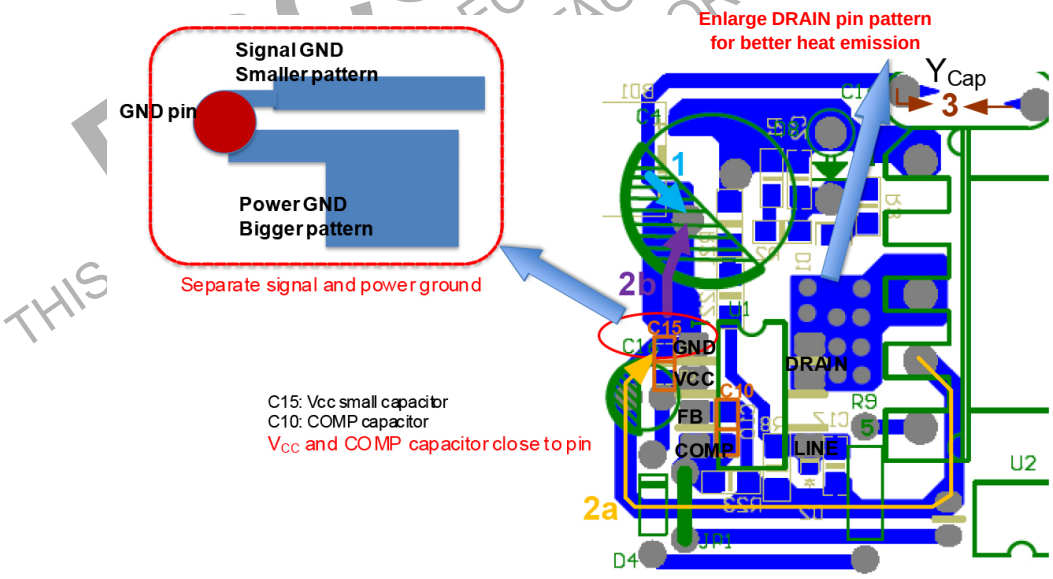


Figure 48. Layout Considerations

Design Example

Hereafter is a typical schematic of an isolated flyback.

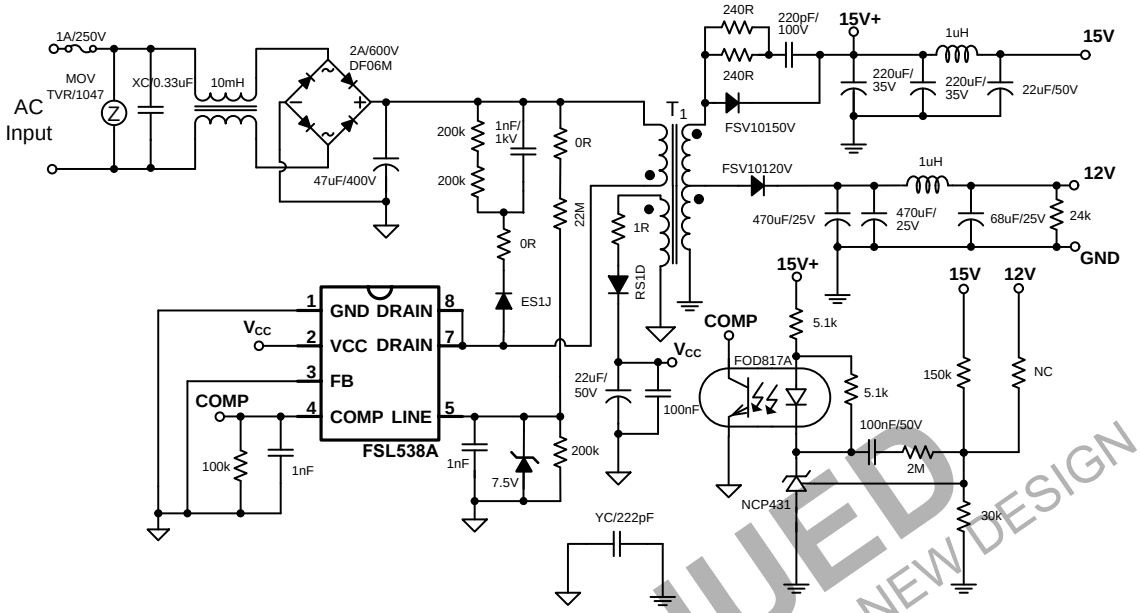


Figure 49. FSL538AFLYGEVB Schematic

REFERENCES

For more details on specific designs, please refer to below documents:

- AN−4148 Audible Noise Reduction Technique for FPS Applications
  https://www.onsemi.com/pub/Collateral/AN−4148.pdf.pdf
- AN−4137 Design Guidelines for Off-line Flyback Converters Using Power Switch
  https://www.onsemi.com/pub/Collateral/AN−4137.pdf.pdf
- AN−4140 Transformer Design Consideration for Offline Flyback Converters Using Power Switch
  https://www.onsemi.com/pub/Collateral/AN−4140.pdf.pdf
- EVBUM2650/D: 14.5 W auxiliary power for white goods and industrial equipment with FSL538HPG
  https://www.onsemi.com/pub/Collateral/EVBUM2650−D.PDF
- EVBUM2651/D: 15 W auxiliary power for white goods and industrial equipment with FSL538APG
  https://www.onsemi.com/pub/Collateral/EVBUM2651−D.PDF
- EVBUM2652/D: 8 W auxiliary power for white goods and industrial equipment with FSL518APG
  https://www.onsemi.com/pub/Collateral/EVBUM2652−D.PDF
- FSL5x8 Application note and Design tool
  https://www.onsemi.com/PowerSolutions/supportDoc.do?type=tools&rpn=FSL538

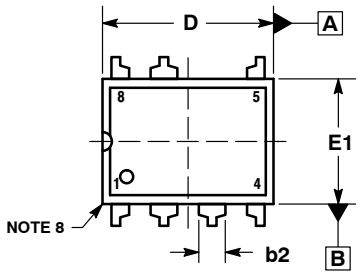
ORDERING INFORMATION

Device	Current Limit (A)	$R_{DS.ON,max}$ (Ω)	Package	Shipping†
FSL518HPG	0.46	8.0	PDIP−7 (Pb-Free)	Tube
FSL518HPLR2G	0.46	8.0	PDIP−7 GW (Pb-Free)	Tape & Reel
FSL518APG	0.61	8.0	PDIP−7 (Pb-Free)	Tube
FSL518APLR2G	0.61	8.0	PDIP−7 GW (Pb-Free)	Tape & Reel
FSL538HPG	0.66	4.6	PDIP−7 (Pb-Free)	Tube
FSL538HPLR2G	0.66	4.6	PDIP−7 GW (Pb-Free)	Tape & Reel
FSL538APG	0.86	4.6	PDIP−7 (Pb-Free)	Tube
FSL538APLR2G	0.86	4.6	PDIP−7 GW (Pb-Free)	Tape & Reel

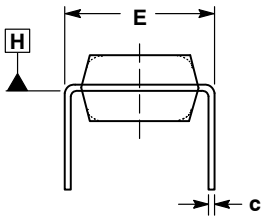
PDIP−7 (PDIP−8 LESS PIN 6)
CASE 626A
ISSUE C

DATE 22 APR 2015

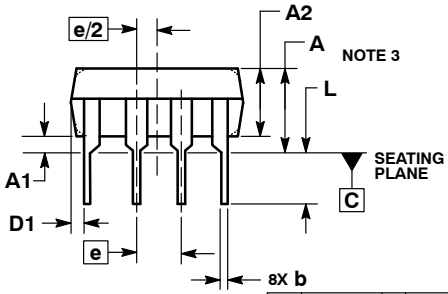
SCALE 1:1



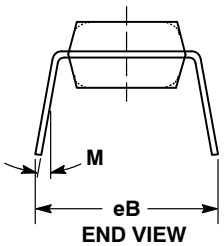
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW

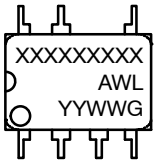


END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	**98AON11774D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**PDIP−7 (PDIP−8 LESS PIN 6)**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales