ON Semiconductor®

FDS6986AS

Dual Notebook Power Supply N-Channel PowerTrench® SyncFET™

General Description

The FDS6986AS is designed to replace two single SO-8 MOSFETs and Schottky diode in synchronous DC:DC power supplies that provide various peripheral voltages for notebook computers and other battery powered electronic devices. FDS6986AS contains two unique 30V, N-channel, logic level, PowerTrench MOSFETs designed to maximize power conversion efficiency.

The high-side switch (Q1) is designed with specific emphasis on reducing switching losses while the low-side switch (Q2) is optimized to reduce conduction losses. Q2 also includes an integrated Schottky diode using ON Semiconductor's monolithic SyncFET technology.

Features

- **Q2**: Optimized to minimize conduction losses
  Includes SyncFET Schottky body diode

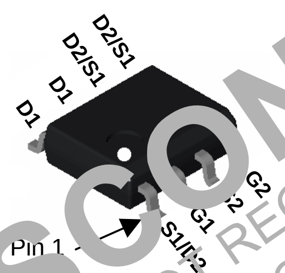
  7.9A, 30V $R_{DS(on)}$ = 20 mΩ @ V_{GS} = 10V

  $R_{DS(on)}$ = [illegible] mΩ @ V_{GS} = 4.5V

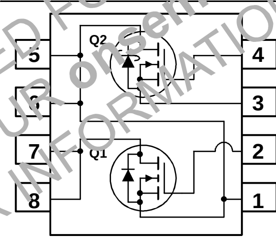
- **Q1**: Optimized for low switching losses
  Low gate charge ([illegible] nC typical)

  6.5A, 30V $R_{DS(on)}$ = 29 mΩ @ V_{GS} = 10V

  $R_{DS(on)}$ = 38 mΩ @ V_{GS} = 4.5V



SO-8



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Q2	Q1	Units
V_{DSS}	Drain-Source Voltage		30	30	V
V_{GSS}	Gate-Source Voltage		±20	±16	V
I_D	Drain Current - Continuous	(Note 1a)	7.9	6.5	A
	- Pulsed		30	20	
P_D	Power Dissipation for Dual Operation		2		W
	Power Dissipation for Single Operation	(Note 1a)	1.6		
		(Note 1b)	1		
		(Note 1c)	0.9		
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6986AS	FDS6986AS	13"	12mm	2500 units
FDS6986AS	FDS6986AS-NL (Note 4)	13"	12mm	2500 units

June-2024, Rev. 2

Publication Order Number:
FDS6986AS/D

Electrical Characteristics
T_A = 25°C unless otherwise noted

Off Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA V_{GS} = 0 V, I_D = 250 uA	Q2 Q1	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C I_D = 250 µA, Referenced to 25°C	Q2 Q1		31 23		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	Q2 Q1			500 1	µA
I_{GSS}	Gate-Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V V_{GS} = ±16 V, V_{DS} = 0 V	Q2 Q1			±100	nA

On Characteristics (Note 2)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, I_D = 1 mA $V_{DS} = V_{GS}$, I_D = 250 µA	Q2 Q1	1 1	1.7 1.9	3 3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C I_D = 250 uA, Referenced to 25°C	Q2 Q1		–[illegible]2 –[illegible]0		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 7.9 A V_{GS} = 10 V, I_D = 7.9 A, T_J = 125°C V_{GS} = 4.5 V, I_D = 7 A	Q2		17 25 22	20 32 28	mΩ
		V_{GS} = 10 V, I_D = 6.5 A V_{GS} = 10 V, I_D = 6.5 A, T_J = 125°C V_{GS} = 4.5 V, I_D = 6 A	Q1		21 32 32	29 49 38	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	Q2 Q1	30 20			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 7.9 A V_{DS} = 5 V, I_D = 6.5 A	Q2 Q1		25 15		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	Q2 Q1		550 720		pF
C_{oss}	Output Capacitance		Q2 Q1		180 120		pF
C_{rss}	Reverse Transfer Capacitance		Q2 Q1		70 60		pF
R_G	Gate Resistance	V_{GS} = 15mV, f = 1.0 MHz	Q2 Q1		3.2 1.2		Ω

Switching Characteristics (Note 2)

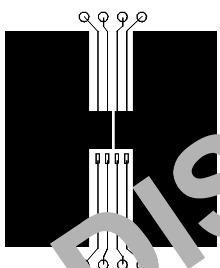
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10V, R_{GEN} = 6 Ω	Q2 Q1		9 10	18 19	ns
t_r	Turn-On Rise Time		Q2 Q1		6 4	12 8	ns
$t_{d(off)}$	Turn-Off Delay Time		Q2 Q1		25 24	40 39	ns
t_f	Turn-Off Fall Time		Q2 Q1		4 3	8 6	ns
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 4.5V, R_{GEN} = 6 Ω	Q2 Q1		11 10	20 20	ns
t_r	Turn-On Rise Time		Q2 Q1		15 9	26 18	ns
$t_{d(off)}$	Turn-Off Delay Time		Q2 Q1		15 13	26 23	ns
t_f	Turn-Off Fall Time		Q2 Q1		6 3	12 6	ns

Electrical Characteristics (continued) T_A = 25°C unless otherwise noted

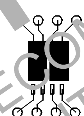
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Switching Characteristics (Note 2)							
$Q_{g(TOT)}$	Total Gate Charge, Vgs = 10V	Q2: V_{DS} = 15 V, I_D = 7.9 A Q1: V_{DS} = 15 V, I_D = 6.5 A	Q2 Q1		10 12	14 17	nC
Q_g	Total Gate Charge, Vgs = 5V		Q2 Q1		5.6 6.5	8 9	nC
Q_{gs}	Gate-Source Charge		Q2 Q1		2.0 2.3		nC
Q_{gd}	Gate-Drain Charge		Q2 Q1		1.5 2.1		nC
Drain–Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q2 Q1			3.0 1.3	A
T_{rr}	Reverse Recovery Time	I_F = 10 A, d_{iF}/d_t = 300 A/µs (Note 3)	Q2		15		ns
Q_{rr}	Reverse Recovery Charge				[illegible]		nC
T_{rr}	Reverse Recovery Time	I_F = 6.5 A, d_{iF}/d_t = 100 A/µs (Note [illegible])	Q1		20		ns
Q_{rr}	Reverse Recovery Charge				12		nC
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.3 A (Note 2) V_{GS} = 0 V, I_S = 1.[illegible] A (Note [illegible])	Q2 Q1		0.6 0.8	0.7 1.2	V

Notes:

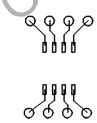
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) [illegible]°C/W when mounted on a 0.5in² pad of 2 oz copper



b) 125°C/W when mounted on a 0.02 in² pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

3. See "SyncFET Schottky body diode characteristics" below.

4. FDS6986AS-NL is a lead free product. FDS6986AS-NL marking will appear on the reel label.

Typical Characteristics: Q2

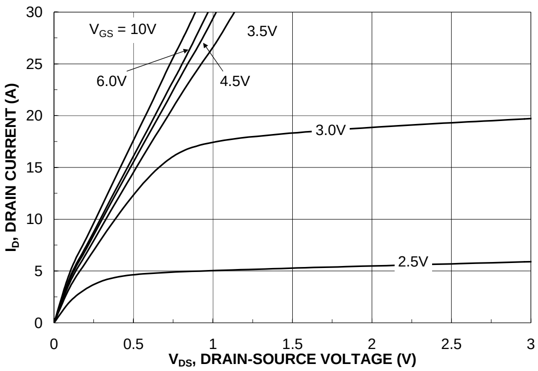


Figure 1. On-Region Characteristics.

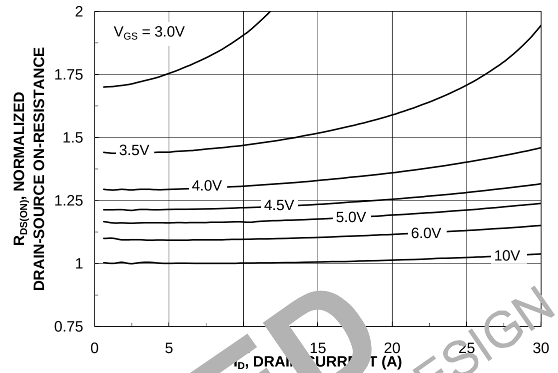


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

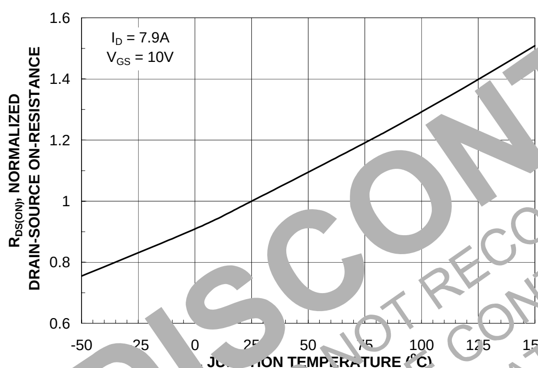


Figure 3. On-Resistance Variation with Temperature.

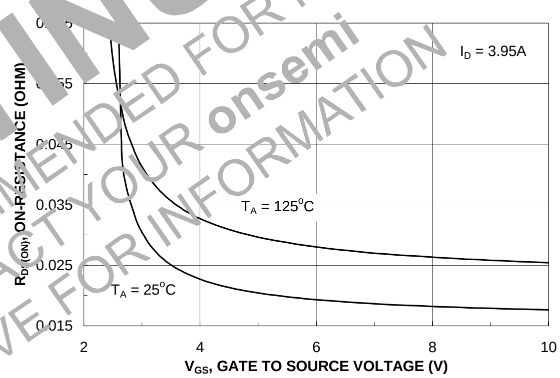


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

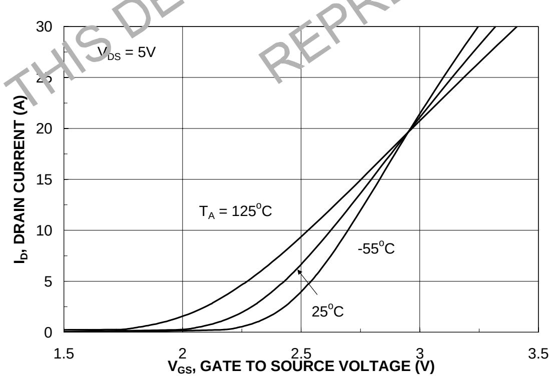


Figure 5. Transfer Characteristics.

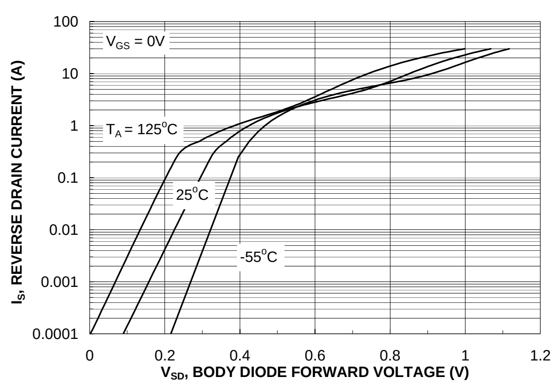


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q2

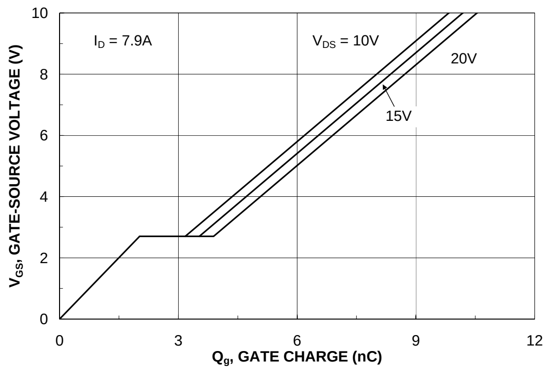


Figure 7. Gate Charge Characteristics.

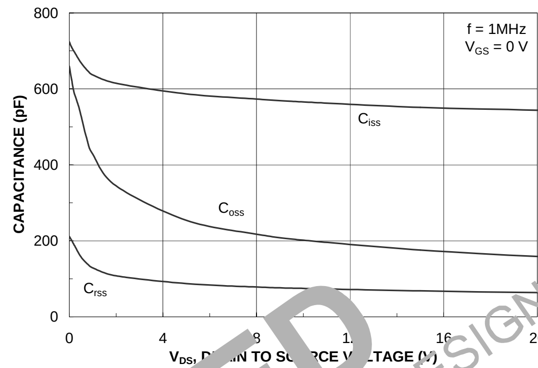


Figure 8. [Capacitance] Characteristics.

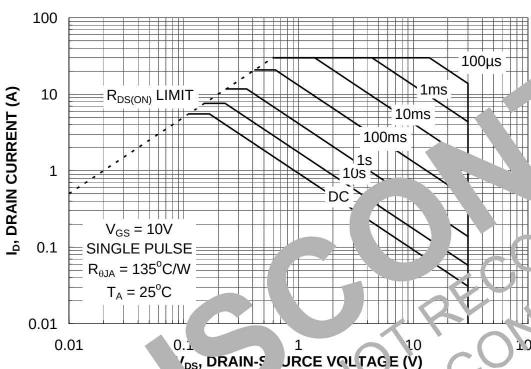


Figure 9. [Maximum Safe Operating Area.]

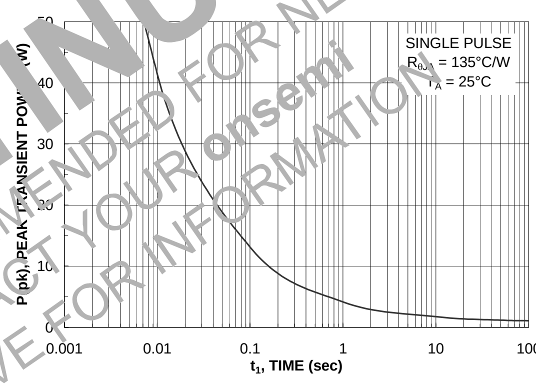


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics Q1

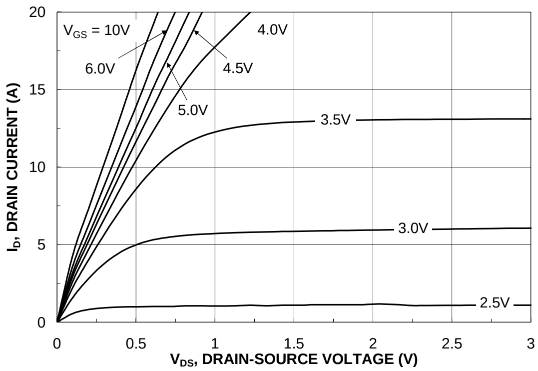


Figure 11. On-Region Characteristics.

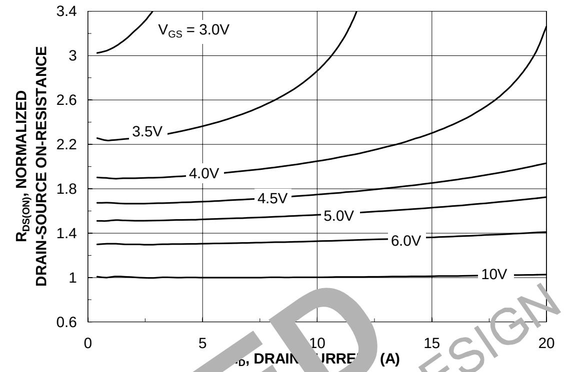


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

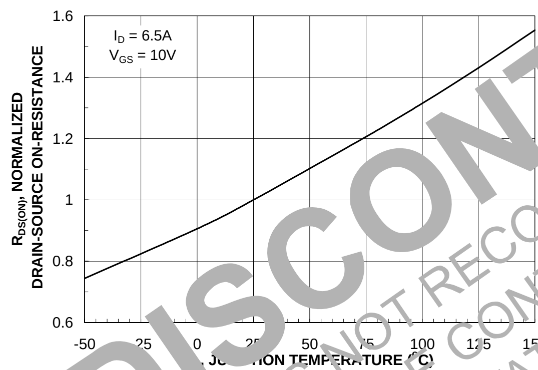


Figure 13. On-Resistance Variation with Temperature.

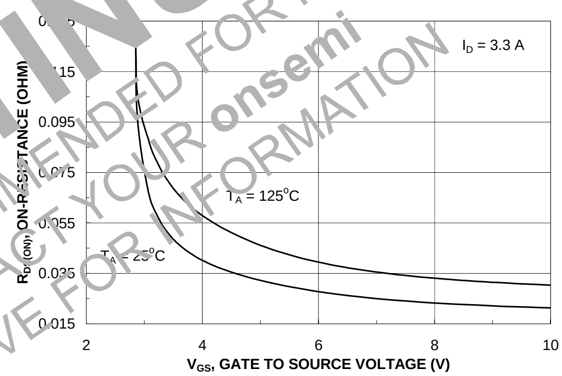


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

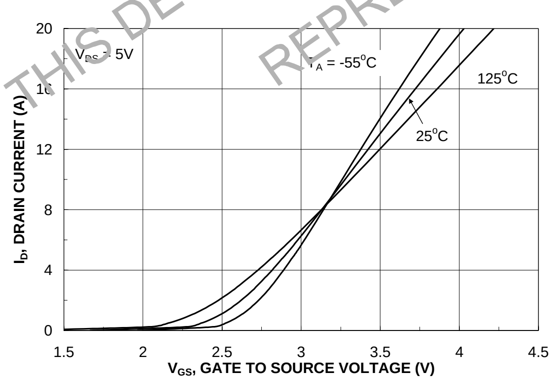


Figure 15. Transfer Characteristics.

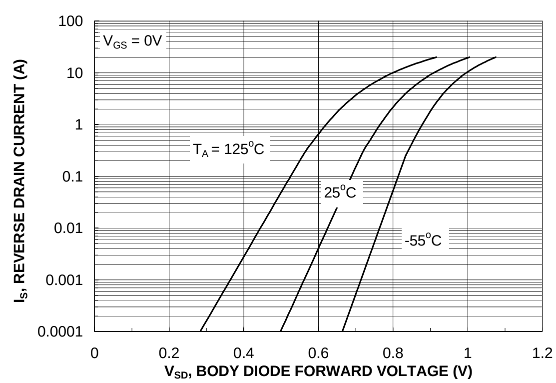


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics Q1

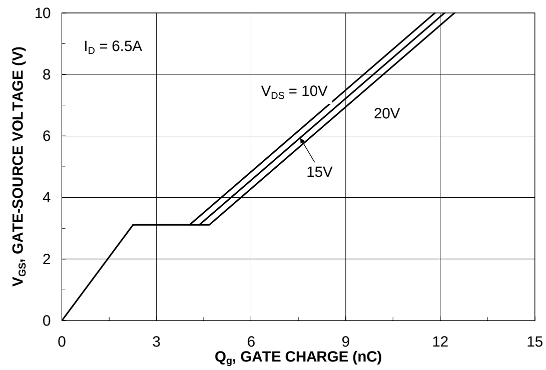


Figure 17. Gate Charge Characteristics.

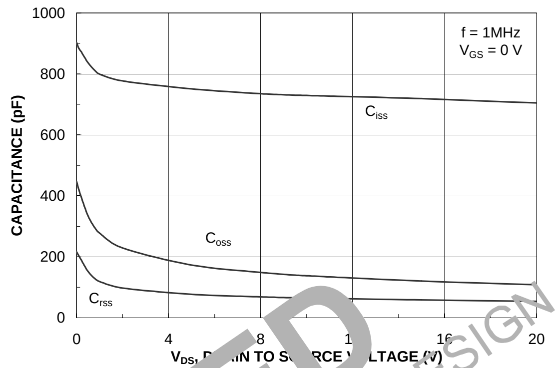


Figure 18. Capacitance Characteristics.

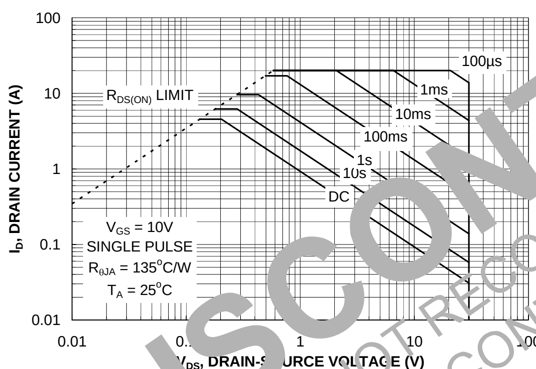


Figure 19. Maximum Safe Operating Area.

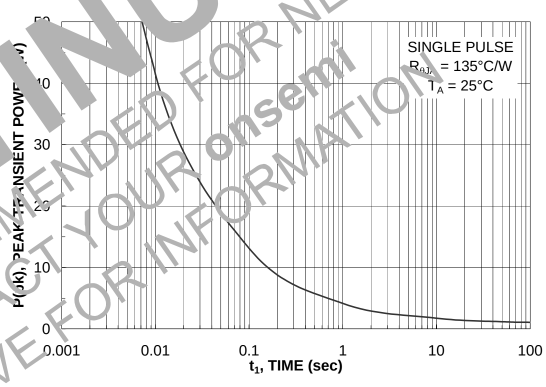


Figure 20. Single Pulse Maximum Power Dissipation.

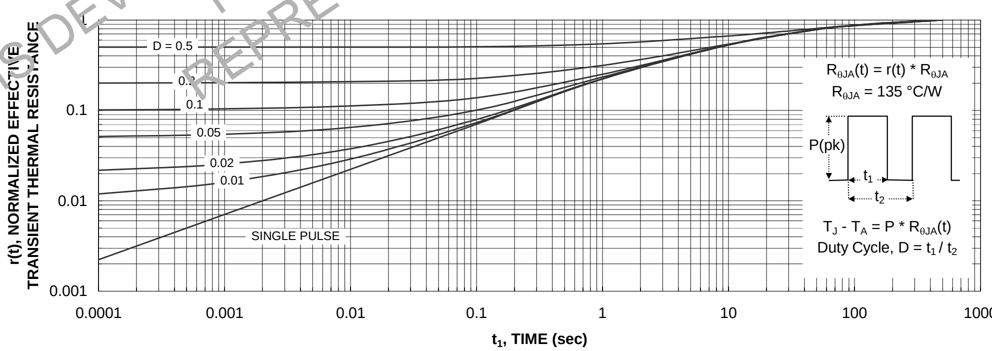


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

Typical Characteristics (continued)

SyncFET Schottky Body Diode Characteristics

ON Semiconductor's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 22 shows the reverse recovery characteristic of the FDS6986AS.

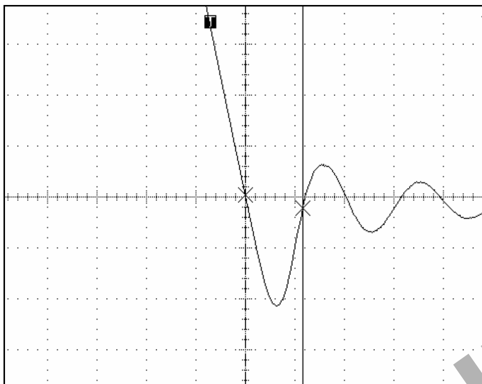


Figure 22. FDS6986AS SyncFET body diode reverse recovery characteristic.

For comparison purposes, Figure 23 shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET (FDS6690A).

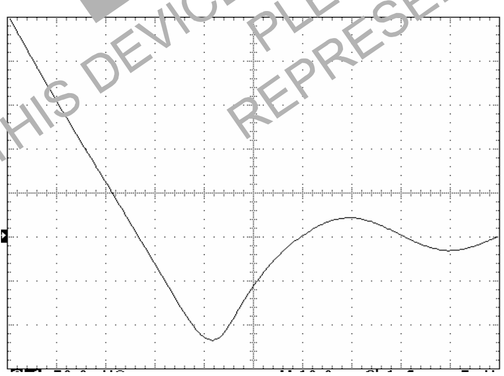


Figure 23. Non-SyncFET (FDS6690A) body diode reverse recovery characteristic.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

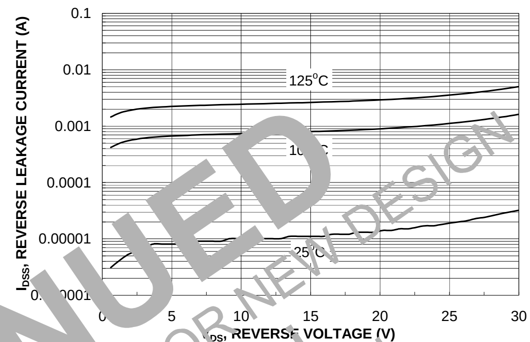


Figure 24. SyncFET body diode reverse leakage versus drain-source voltage and temperature.

Typical Characteristics

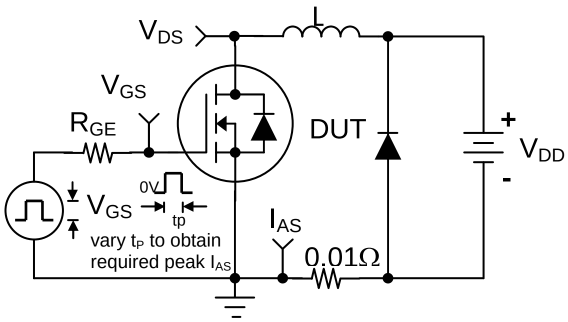


Figure 25. Unclamped Inductive Load Test Circuit

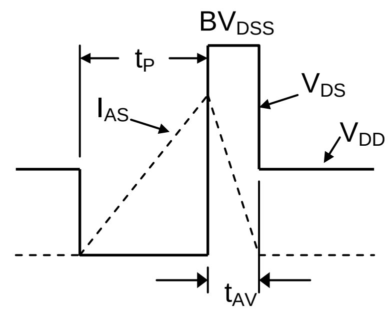


Figure 26. Unclamped Inductive Waveforms

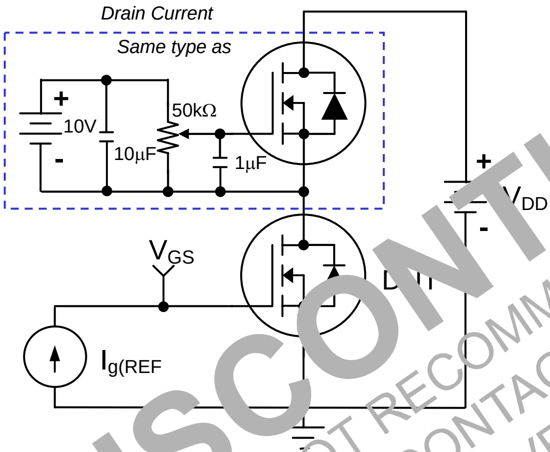


Figure 27. Gate Charge Test Circuit

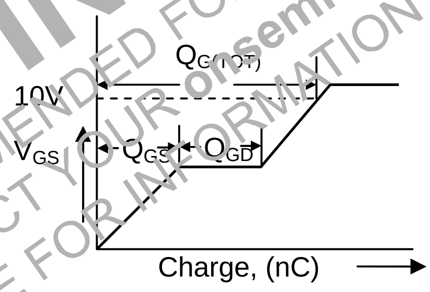


Figure 28. Gate Charge Waveform

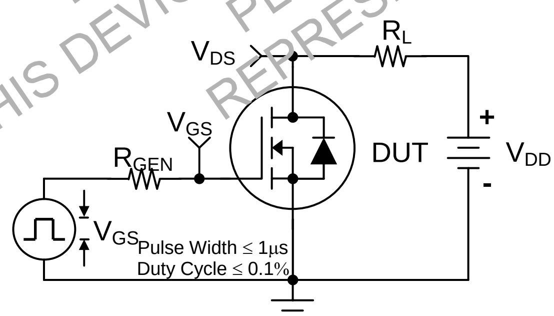


Figure 29. Switching Time Test Circuit

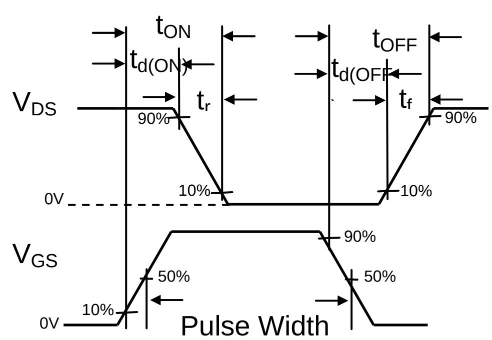


Figure 30. Switching Time Waveforms

PUBLICATION ORDERING INFORMATION

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Email: orderlit@onsemi.com

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