

# MOSFET – P-Channel, POWERTRENCH®

**-20 V, -4 A, 100 mΩ**

## FDC642P-F085, FDC642P-F085P

### Features

- Typ  $R_{DS(on)}$  = 52.5 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -4$  A
- Typ  $R_{DS(on)}$  = 75.3 mΩ at  $V_{GS} = -2.5$  V,  $I_D = -3.2$  A
- Fast Switching Speed
- Low Gate Charge (6.9 nC Typical)
- High Performance Trench Technology for Extremely Low  $R_{DS(on)}$
- SUPERSOT™ –6 Package: Small Footprint (72% Smaller than Standard SO–8); Low Profile (1 mm Thick)
- AEC–Q101 Qualified and PPAP Capable
- This Device is Pb–Free and is RoHS Compliant

### Applications

- Load Switch
- Battery Protection
- Power management

### MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

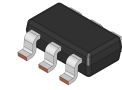
Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain to Source Voltage	-20	V
$V_{GS}$	Gate to Source Voltage	±8	V
$I_D$	Drain Current – Continuous ( $V_{GS} = 4.5$ V) – Pulsed	-4 -20	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 1)	72	mJ
$P_D$	Power Dissipation	1.2	W
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 14.1$  mH,  $I_{AS} = -3.2$  A

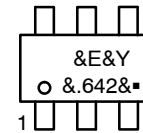
### THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	30	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, 1in <sup>2</sup> Copper pad Area	103	



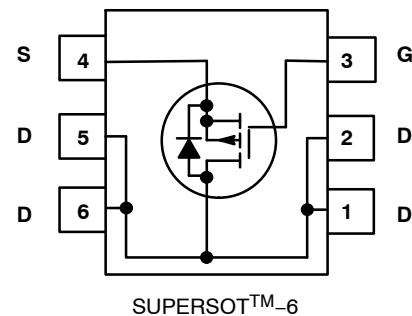
TSOT23 6-Lead  
CASE 419BL

### MARKING DIAGRAM



XXX = Specific Device Code  
&E = Space Designator  
&Y = Year of Production  
&. = Pin One Identifier  
▪ = Pb–Free Package

### PINOUT



### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FDC642P–F085, FDC642P–F085P

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

B <sub>V</sub> DSS	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	-20	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -16 V, V <sub>GS</sub> = 0 V	-	-	-1	μA
		V <sub>DS</sub> = -16 V, V <sub>GS</sub> = 0 V, T <sub>A</sub> = 150°C	-	-	-250	
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±8 V	-	-	±100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250 μA	-0.4	-0.7	-1.5	V
r <sub>DS(on)</sub>	Drain to Source On Resistance	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -4 A	-	52.5	65	mΩ
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -3.2 A	-	75.3	100	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = -4 A, T <sub>J</sub> = 125°C	-	72.7	105	
g <sub>FS</sub>	Forward Transconductance	V <sub>DD</sub> = -5 V, I <sub>D</sub> = -4 A	-	10	-	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -10 V f = 1 MHz	-	630	-	pF
C <sub>oss</sub>	Output Capacitance		-	160	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	65	-	pF
R <sub>g</sub>	Gate Resistance	f = 1 MHz	-	4.4	-	Ω
Q <sub>g(TOT)</sub>	Total Gate Charge at -4.5 V	V <sub>GS</sub> = 0 V to -4.5 V, V <sub>DD</sub> = -10 V, I <sub>D</sub> = -4 A	-	6.9	9.0	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	V <sub>DD</sub> = -10 V I <sub>D</sub> = -4 A	-	1.2	-	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		-	1.8	-	nC

### SWITCHING CHARACTERISTICS

t <sub>on</sub>	Turn-On Time	V <sub>DD</sub> = -10 V, I <sub>D</sub> = -1 A, V <sub>GS</sub> = -4.5 V, R <sub>GS</sub> = 6 Ω	-	-	23	ns
t <sub>d(on)</sub>	Turn-On Delay Time		-	7.3	-	ns
t <sub>r</sub>	Rise Time		-	5.5	-	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	23.2	-	ns
t <sub>f</sub>	Fall Time		-	9.6	-	ns
t <sub>off</sub>	Turn-Off Time		-	-	53	ns

### DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source to Drain Diode Voltage	I <sub>SD</sub> = -1.3 A	-	-	-1.25	V
		I <sub>SD</sub> = -0.65 A	-	-	-1.0	
t <sub>rr</sub>	Reverse Recovery Time	I <sub>SD</sub> = -1.3 A, dI <sub>SD</sub> /dt = 100 A/μs	-	17	22	ns
Q <sub>rr</sub>	Reverse Recovery Charge		-	5.6	7.3	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size <sup>†</sup>	Tape Width	Quantity
FDC642P	FDC642P–F085	SSOT–6	7"	8 mm	3000 Units
FDC642P	FDC642P–F085P	SSOT–6	7"	8 mm	3000 Units

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

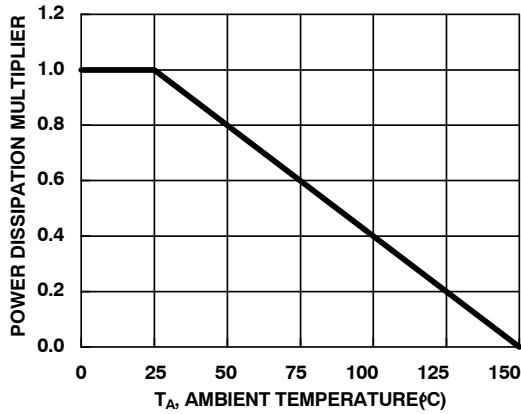


Figure 1. Normalized Power Dissipation vs. Ambient Temperature

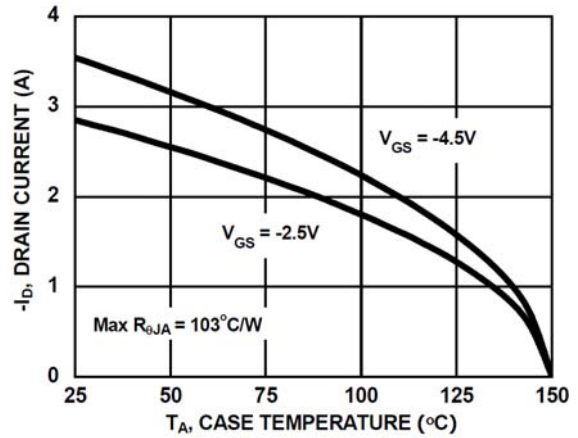


Figure 2. Maximum Continuous Drain Current vs. Ambient Temperature

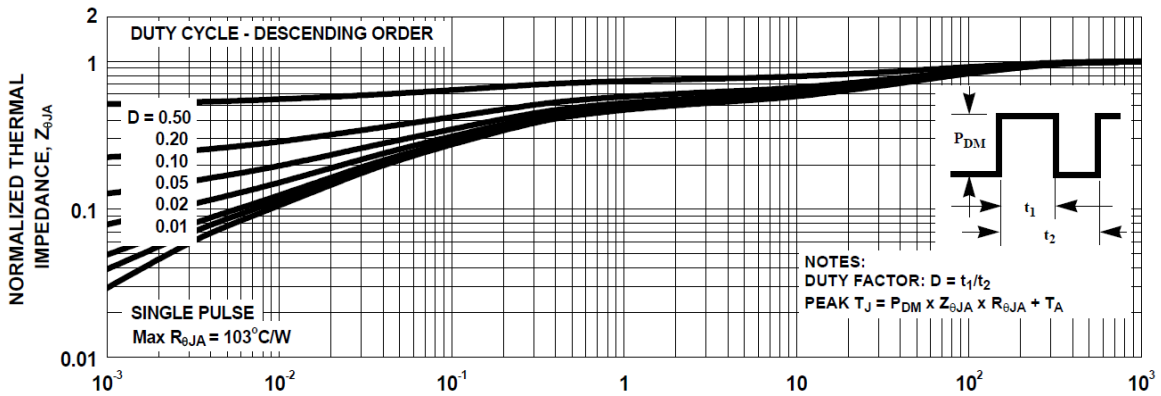


Figure 3. Normalized Maximum Transient Thermal Impedance

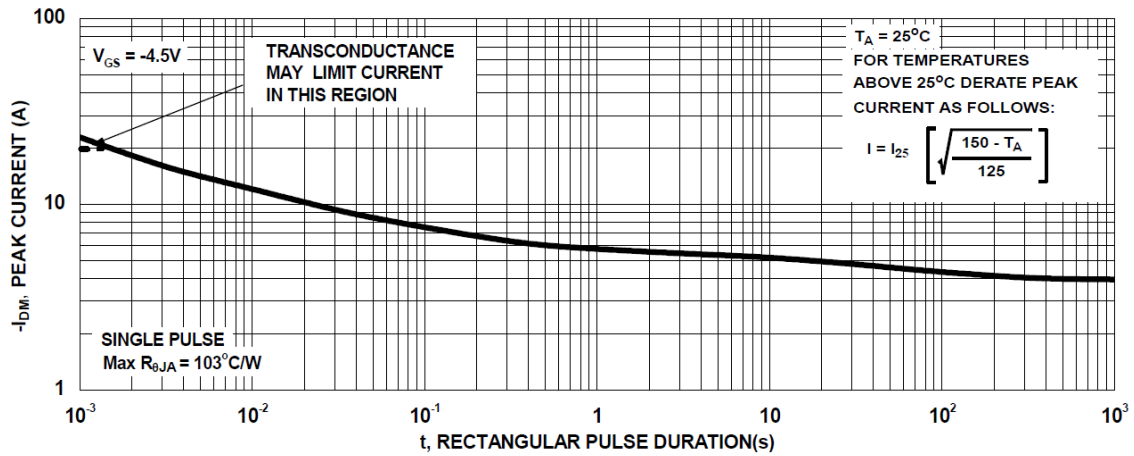


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

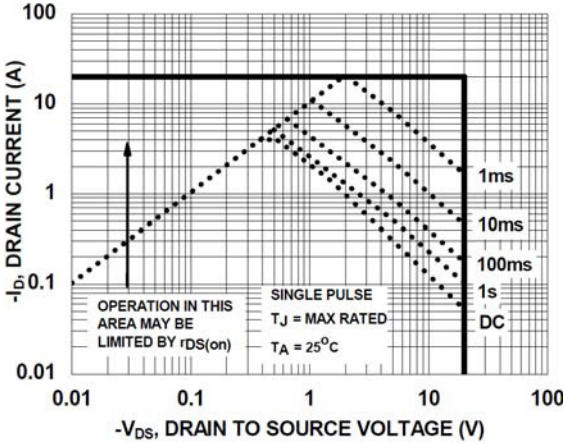


Figure 5. Forward Bias Safe Operating Area

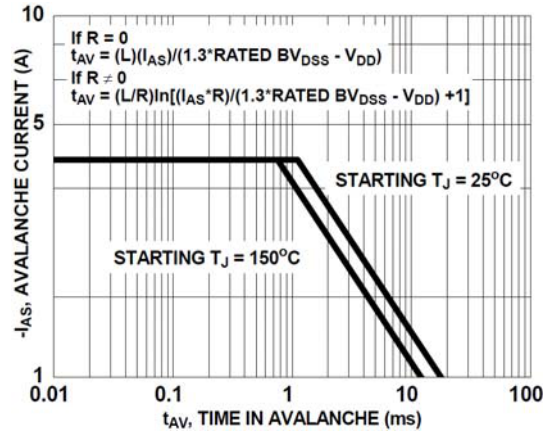


Figure 6. Unclamped Inductive Switching Capability

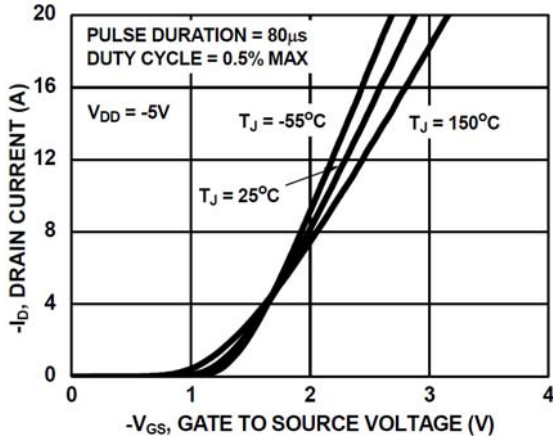


Figure 7. Transfer Characteristics

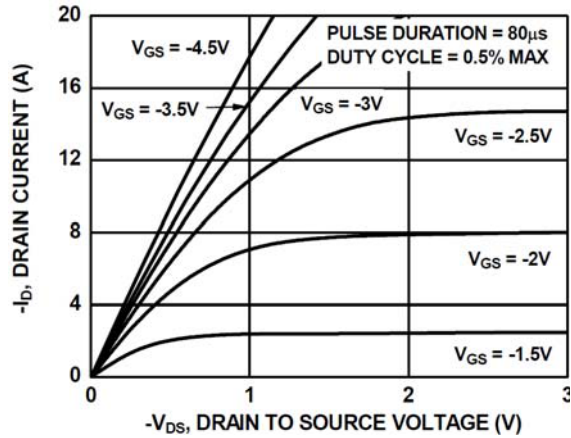


Figure 8. Saturation Characteristics

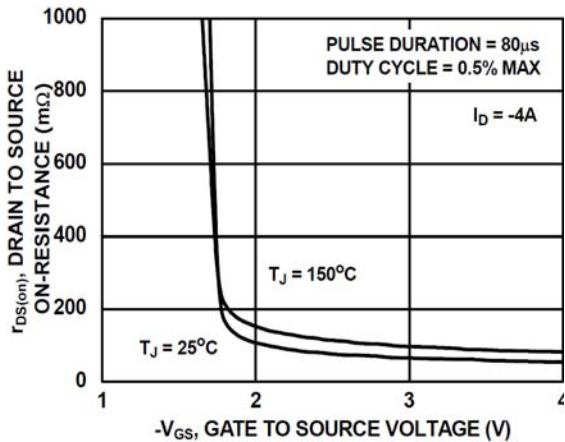


Figure 9. Drain to Source On-Resistance Variation vs. Gate to Source Voltage

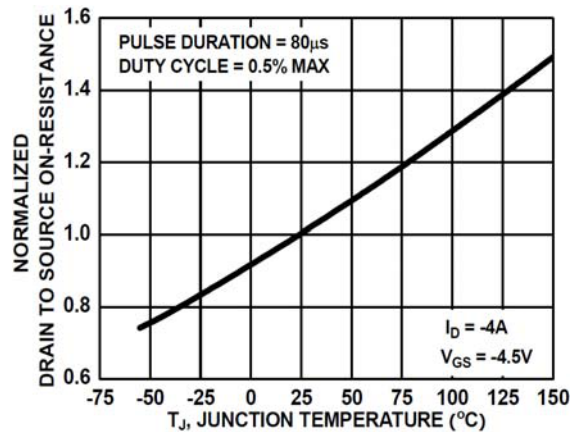


Figure 10. Normalized Drain to Source On-Resistance vs. Junction Temperature

# FDC642P-F085, FDC642P-F085P

TYPICAL CHARACTERISTICS  $T_J = 25^\circ\text{C}$  unless otherwise noted (continued)

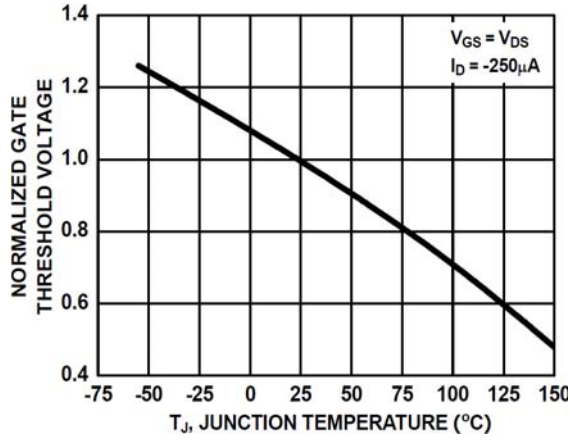


Figure 11. Normalized Gate Threshold Voltage vs. Junction Temperature

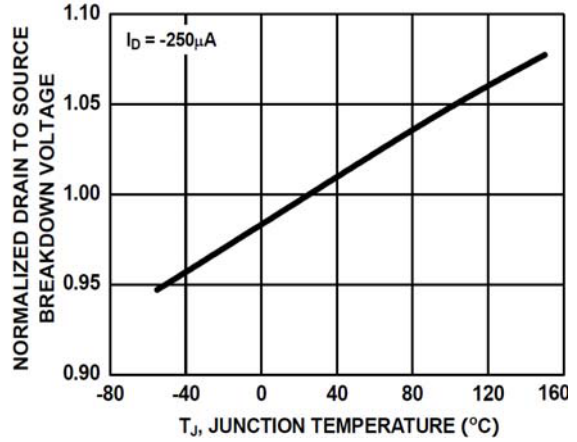


Figure 12. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

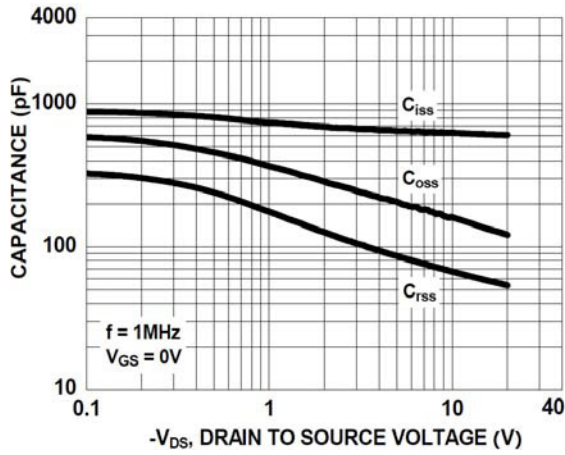


Figure 13. Capacitance vs. Drain to Source Voltage

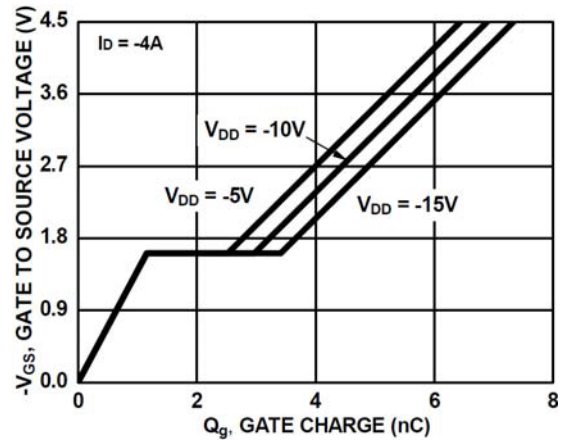


Figure 14. Gate Charge vs. Gate to Source Voltage

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

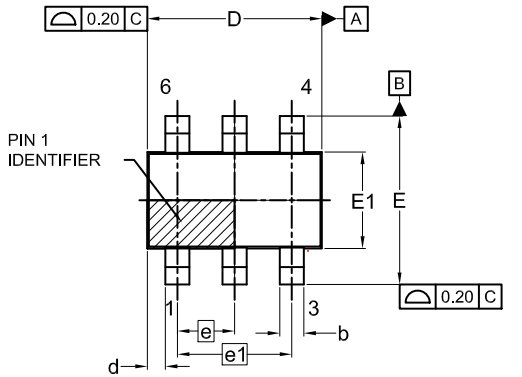
ON Semiconductor®



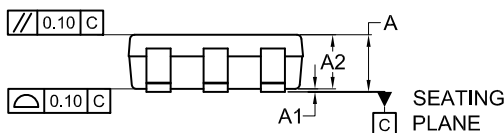
SCALE 2:1

### TSOT23 6-Lead CASE 419BL ISSUE A

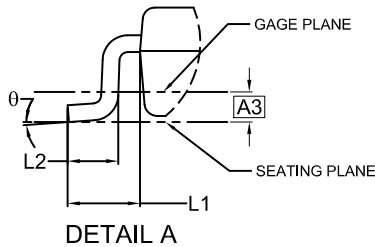
DATE 31 AUG 2020



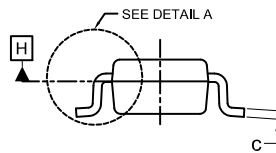
TOP VIEW



FRONT VIEW

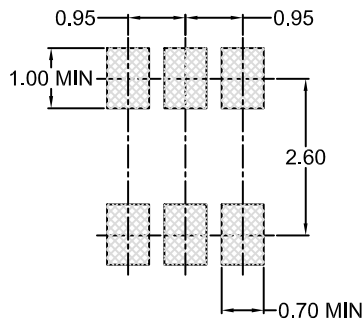


DETAIL A



SIDE VIEW

SYMM  
⌀



LAND PATTERN  
RECOMMENDATION

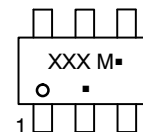
\*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3	0.25 BSC		
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d	0.30 REF		
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.95 BSC		
e1	1.90 BSC		
L1	0.60 REF		
L2	0.20	0.40	0.60
⊖	0°	--	10°

#### GENERIC MARKING DIAGRAM\*



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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