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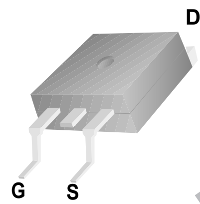
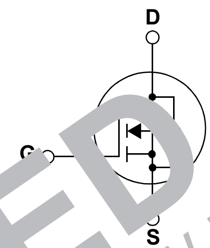
FDB9406-F085

N-Channel PowerTrench® MOSFET

40 V, 110 A, 1.8 mΩ





TO-263
FDB SERIES

Features

- Typ $R_{DS(on)}$ = 1.31mΩ at V_{GS} = 10V, I_D = 80A
- Typ $Q_{g(tot)}$ = 107nC at V_{GS} = 10V, I_D = 80A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electronic Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12V Systems

MOSFET Maximum Ratings T_J = 25°C unless otherwise noted.

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain to Source Voltage		40	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current - Continuous (V_{GS}=10) (Note 1)	T_C = 25°C	110	A
	Pulsed Drain Current	T_C = 25°C	See Figure4	
E_{AS}	Single Pulse Avalanche Energy	(Note 2)	174	mJ
P_D	Power Dissipation		176	W
	Derate above 25°C		1.18	W/°C
T_J, T_{STG}	Operating and Storage Temperature		-55 to + 175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case		0.85	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient	(Note 3)	43	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB9406	FDB9406-F085	D2-PAK(TO-263)	330mm	24mm	800 units

Notes:
1: Current is limited by bondwire configuration.
2: Starting T_J = 25°C, L = 0.045mH, I_{AS} = 88A, V_{DD} = 40V during inductor charging and V_{DD} = 0V during time in avalanche.
3: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2oz copper.

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Units
Off Characteristics							
B_{VDSS}	Drain-to-Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V		40	-	-	V
I_{DSS}	Drain-to-Source Leakage Current	V_{DS}=40V, V_{GS} = 0V	T_J = 25°C	-	-	1	μA
			T_J = 175°C(Note 4)	-	-	1	mA
I_{GSS}	Gate-to-Source Leakage Current	V_{GS} = ±20V		-	-	±100	nA
On Characteristics							
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA		2.0	2.8[illegible]	[illegible]	V
$R_{DS(on)}$	Drain-to-Source On Resistance	I_D = 80A, V_{GS}= 10V	T_J = 25°C	-	1.[illegible]	1.8[illegible]	mΩ
			T_J = 175°C(Note 4)		2.2	2.8[illegible]	mΩ
Dynamic Characteristics							
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		[illegible]	7710	-	pF
C_{oss}	Output Capacitance			[illegible]	201[illegible]	-	pF
C_{rss}	Reverse Transfer Capacitance			-	[illegible]40	-	pF
R_g	Gate Resistance	f = 1MHz		-	2.7	-	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10V	V_{GS} = 0 to 10V	V_{DD} = 32V, I_D = 80A	-	10[illegible]	138	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 2V		-	[illegible]	[illegible]	nC
Q_{gs}	Gate-to-Source Gate Charge			-	33		nC
Q_{gd}	Gate-to-Drain "Miller" Charge			-	18	-	nC

Switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
t_{on}	Turn-On Time	V_{DD} = 20V, I_D = 80A, V_{GS} = 10V, R_{GEN} = 6Ω	-	-	160	ns
$t_{d(on)}$	Turn-On Delay		-	32	-	ns
t_r	Rise Time		-	81	-	ns
$t_{d(off)}$	Turn-Off Delay		-	50	-	ns
t_f	Fall Time		-	23	-	ns
t_{off}	Turn-Off Time		-	-	93	ns
Drain-Source Diode Characteristics						
V_{SD}	Source-to-Drain Diode Voltage	I_{SD} = 80A, V_{GS} = 0V	-	-	1.25	V
t_{rr}	Reverse-Recovery Time	I_F = 80A, dI_{SD}/dt = 100A/μs, V_{DD}=32V	-	85	110	ns
Q_{rr}	Reverse-Recovery Charge		-	122	160	nC

Note:

4: The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

Typical Characteristics

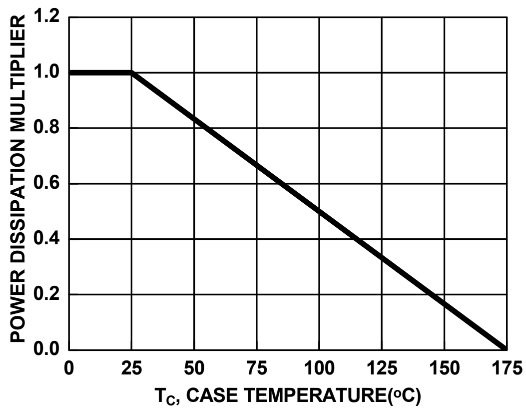


Figure 1. Normalized Power Dissipation vs. Case Temperature

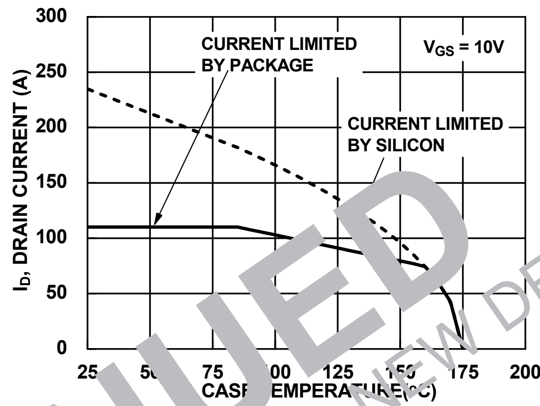


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

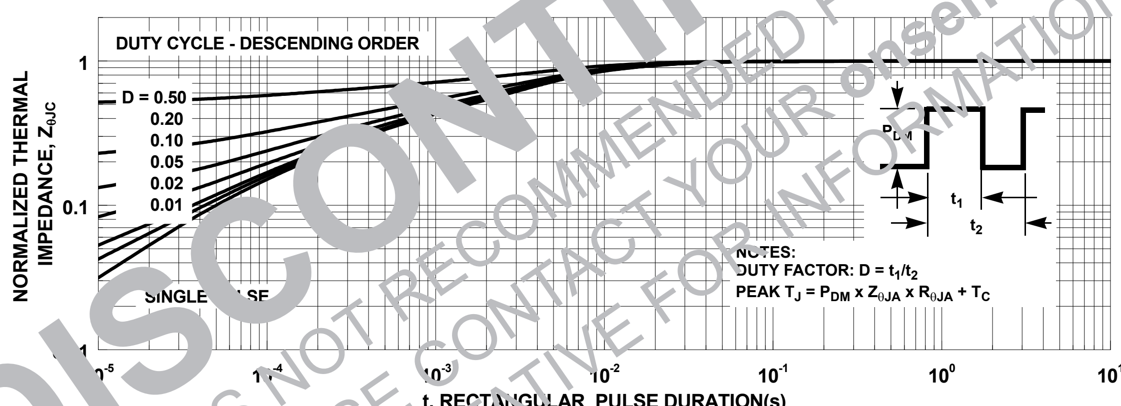


Figure 3. Normalized Maximum Transient Thermal Impedance

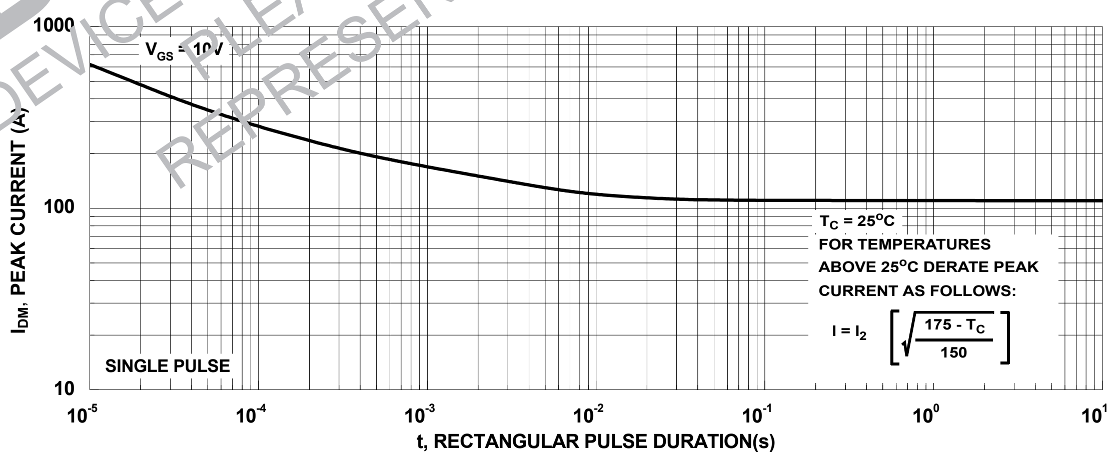


Figure 4. Peak Current Capability

Typical Characteristics

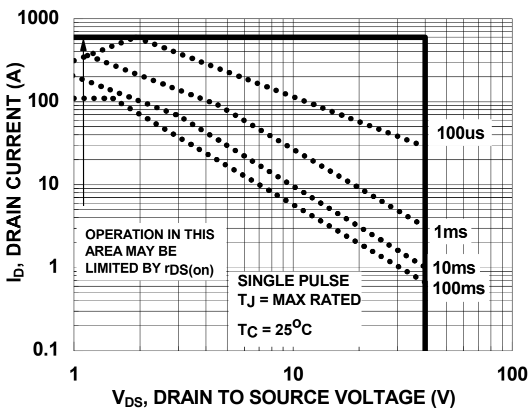
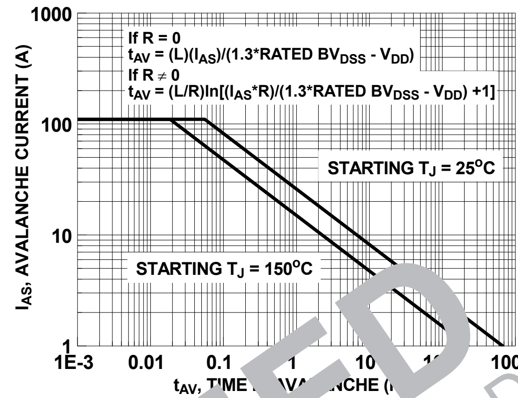


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

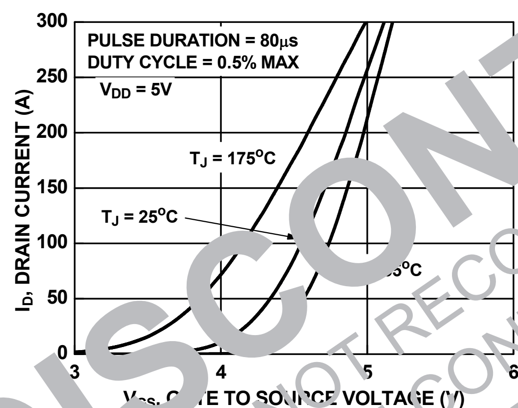


Figure 7. Transfer Characteristics

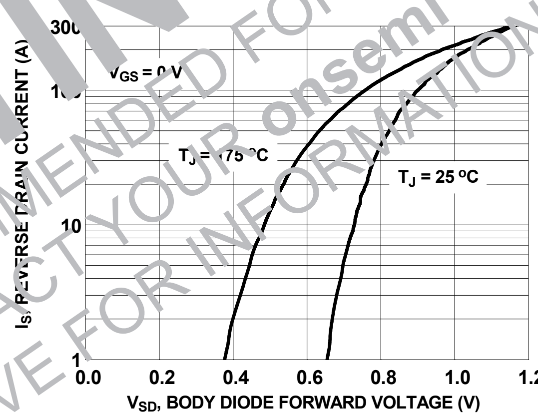


Figure 8. Forward Diode Characteristics

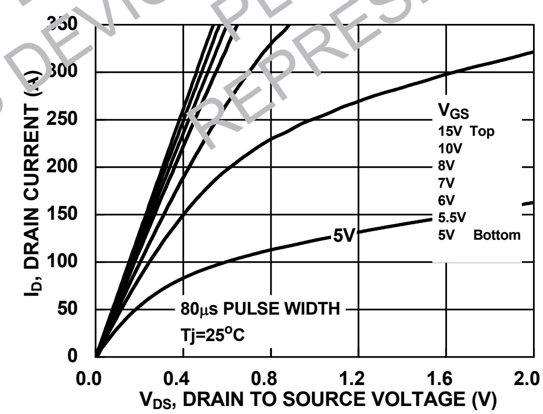


Figure 9. Saturation Characteristics

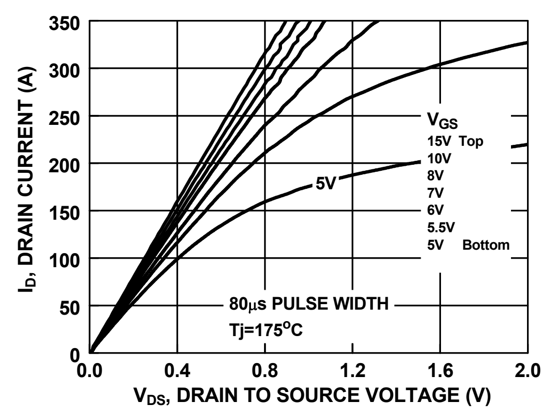


Figure 10. Saturation Characteristics

Typical Characteristics

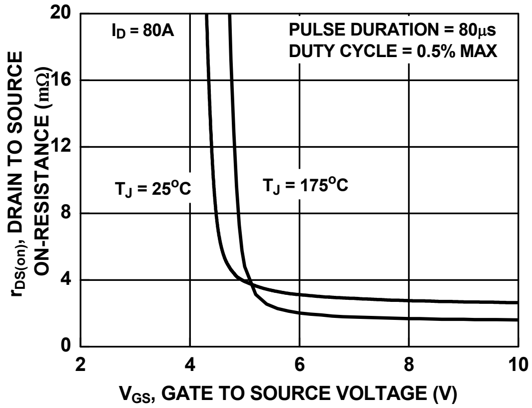


Figure 11. R_{DSON} vs. Gate Voltage

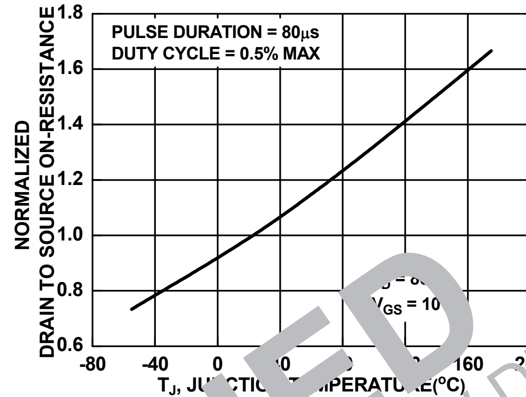


Figure 12. Normalized R_{DSON} vs. Junction Temperature

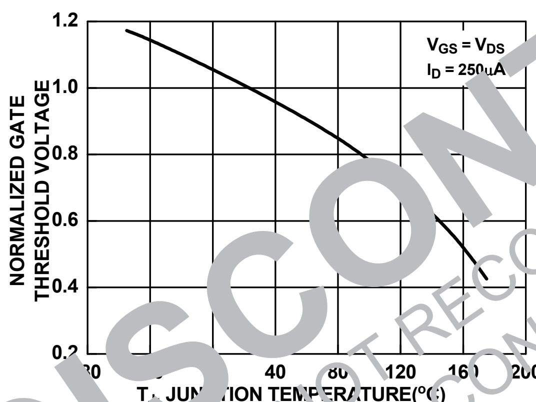


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

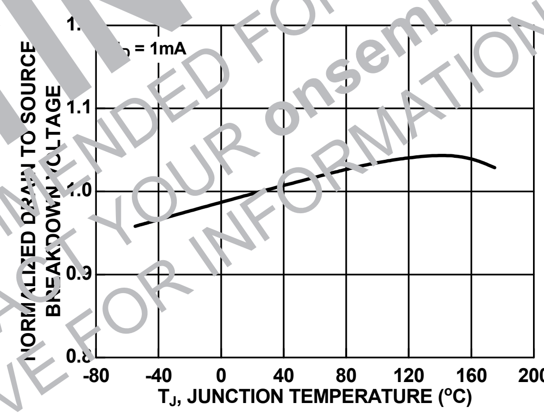


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

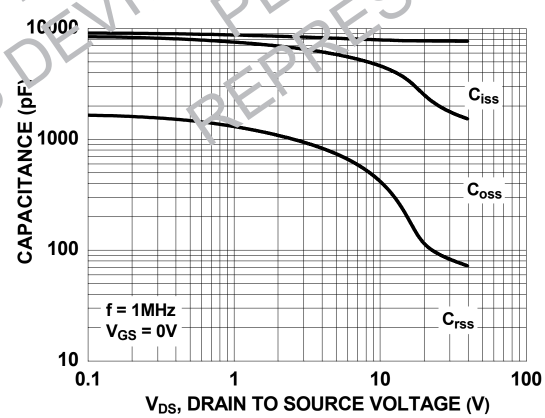


Figure 15. Capacitance vs. Drain to Source Voltage

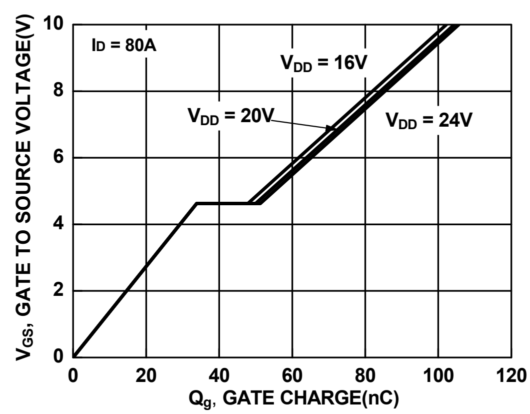


Figure 16. Gate Charge vs. Gate to Source Voltage

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