

N-Channel Shielded Gate POWERTRENCH[®] MOSFET

100 V, 1.7 mΩ, 268 A

FDB1D7N10CL7

Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

Features

- Max $R_{DS(on)}$ = 1.75 mΩ at $V_{GS} = 10$ V, $I_D = 100$ A
- Max $R_{DS(on)}$ = 1.7 mΩ at $V_{GS} = 12$ V, $I_D = 100$ A
- Max $R_{DS(on)}$ = 1.65 mΩ at $V_{GS} = 15$ V, $I_D = 100$ A
- Max $R_{DS(on)}$ = 4.4 mΩ at $V_{GS} = 6$ V, $I_D = 63$ A
- 50% Lower Q_{rr} than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- ESD Protection Level: HBM > 4 kV, CDM > 2 kV
- MSL1 Robust Package Design
- 100% UIL Tested

Applications

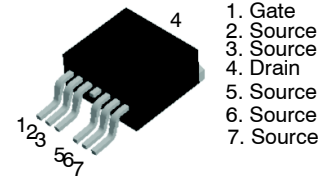
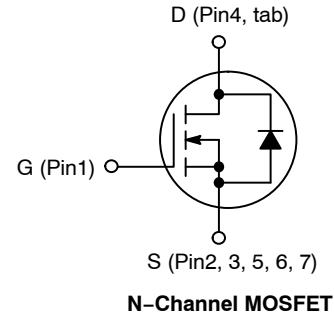
- Industrial Motor Drive
- Industrial Power Supply
- Industrial Automation
- Battery Operated Tools
- Battery Protection
- Solar Inverters
- UPS and Energy Inverters
- Energy Storage
- Load Switch

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, Unless otherwise specified)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous ($T_C = 25^\circ\text{C}$) (Note 5) Continuous ($T_C = 100^\circ\text{C}$) (Note 5) Pulsed (Note 4)	268	A
		190	
		1390	
E_{AS}	Single Pulsed Avalanche Energy (Note 3)	595	mJ
P_D	Power Dissipation $T_C = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$ (Note 1a)	250	W
		3.8	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	°C

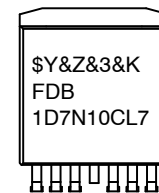
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

V_{DS}	I_D MAX	$r_{DS(on)}$ MAX
100 V	268 A	1.7 mΩ



**D2PAK7 (TO-263 7 LD)
CASE 418AY**

MARKING DIAGRAM



$\$Y$ = onsemi Logo
 $\&Z$ = Assembly Plant Code
 $\&3$ = Numeric Date Code
 $\&K$ = Lot Code
 FDB1D7N10CL7 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

FDB1D7N10CL7

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	0.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	40	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
--------	-----------	-----------------	-----	-----	-----	------

OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0 \text{ V}$	100	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C	–	57	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}$, $V_{GS} = 0 \text{ V}$	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0 \text{ V}$	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 700 \mu\text{A}$	2.0	3.1	4.0	V
$V_{GS(th)}/\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 700 \mu\text{A}$, referenced to 25°C	–	–9	–	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}$, $I_D = 100 \text{ A}$	–	1.5	1.75	m Ω
		$V_{GS} = 12 \text{ V}$, $I_D = 100 \text{ A}$	–	1.4	1.7	
		$V_{GS} = 15 \text{ V}$, $I_D = 100 \text{ A}$	–	1.33	1.65	
		$V_{GS} = 6 \text{ V}$, $I_D = 63 \text{ A}$	–	2.2	4.4	
		$V_{GS} = 10 \text{ V}$, $I_D = 100 \text{ A}$, $T_J = 150^\circ\text{C}$	–	2.65	3.1	
g_{FS}	Forward Transconductance	$V_{DS} = 5 \text{ V}$, $I_D = 100 \text{ A}$	–	237	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 50 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	–	8285	11600	pF
C_{oss}	Output Capacitance		–	5025	7035	pF
C_{rss}	Reverse Transfer Capacitance		–	50	80	pF
R_g	Gate Resistance		0.1	0.8	1.6	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50 \text{ V}$, $I_D = 100 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_{GEN} = 6 \Omega$	–	39	63	ns	
t_r	Rise Time		–	33	53	ns	
$t_{d(off)}$	Turn-Off Delay Time		–	85	136	ns	
t_f	Fall Time		–	36	58	ns	
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ V to } 10 \text{ V}$	$V_{DD} = 50 \text{ V}$, $I_D = 100 \text{ A}$	–	116	163	nC
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ V to } 6 \text{ V}$		–	74	104	nC
Q_{gs}	Gate to Source Gate Charge			–	37	–	nC
Q_{gd}	Gate to Drain "Miller" Charge			–	24	–	nC
Q_{oss}	Output Charge	$V_{DD} = 50 \text{ V}$, $V_{GS} = 0 \text{ V}$		–	333	–	nC

SOURCE-DRAIN DIODE CHARACTERISTICS

I_S	Continuous Drain to Source Diode Forward Current	–	–	268	A	
I_{SM}	Pulsed Drain to Source Diode Forward Current	–	–	1390	A	
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}$, $I_S = 100 \text{ A}$ (Note 2)	–	0.9	1.2	V

FDB1D7N10CL7

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
--------	-----------	-----------------	-----	-----	-----	------

SOURCE-DRAIN DIODE CHARACTERISTICS

t_{rr}	Reverse Recovery Time	$I_F = 50\text{ A}$, $di/dt = 300\text{ A}/\mu\text{s}$	–	63	101	ns
Q_{rr}	Reverse Recovery Charge		–	186	298	nC
t_{rr}	Reverse Recovery Time	$I_F = 50\text{ A}$, $di/dt = 1000\text{ A}/\mu\text{s}$	–	82	132	ns
Q_{rr}	Reverse Recovery Charge		–	869	1390	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
 - $40^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.
 - $62.5^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.
- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0 %.
- E_{AS} of 595 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 0.3\text{ mH}$, $I_{AS} = 63\text{ A}$, $V_{DD} = 90\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 91\text{ A}$.
- Pulsed Id please refer to Figure "Forward Bias Safe Operating Area" for more details.
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB1D7N10CL7	FDB1D7N10CL7	D2-PAK-7L	330 mm	24 mm	800 Units

FDB1D7N10CL7

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

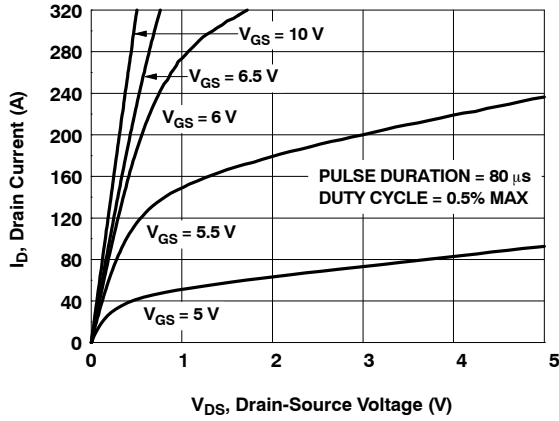


Figure 1. On-Region Characteristics

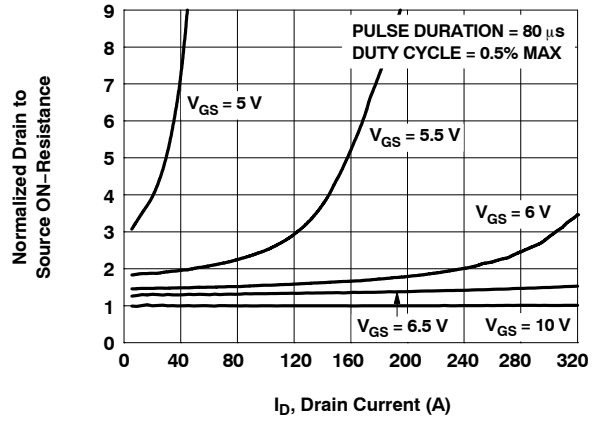


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

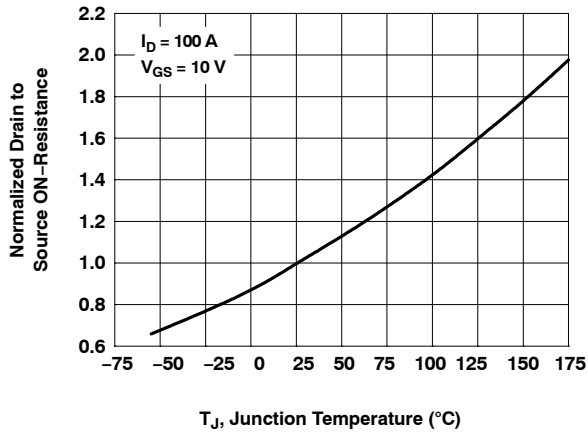


Figure 3. Normalized On-Resistance vs. Junction Temperature

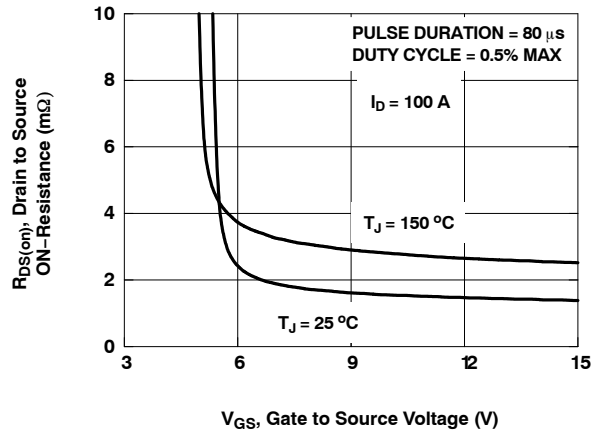


Figure 4. On-Resistance vs. Gate to Source Voltage

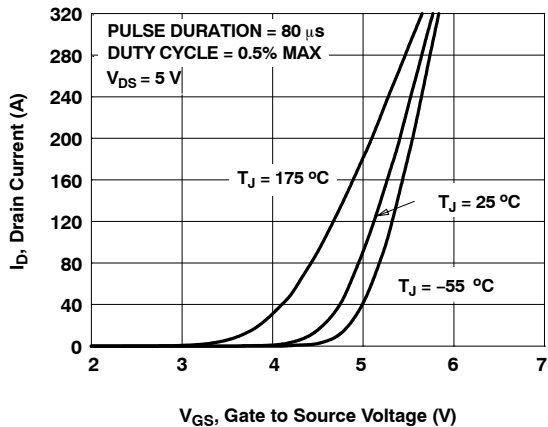


Figure 5. Transfer Characteristics

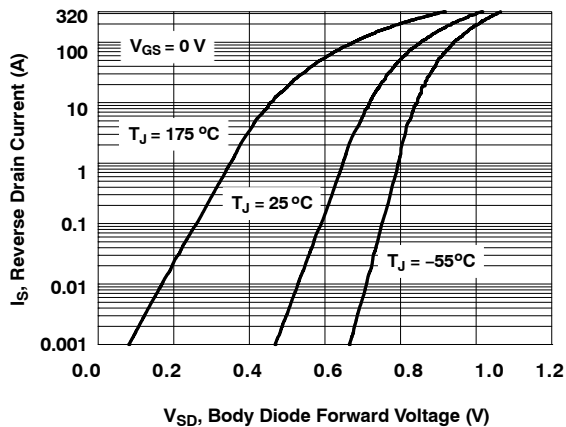


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

FDB1D7N10CL7

TYPICAL CHARACTERISTICS (Continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

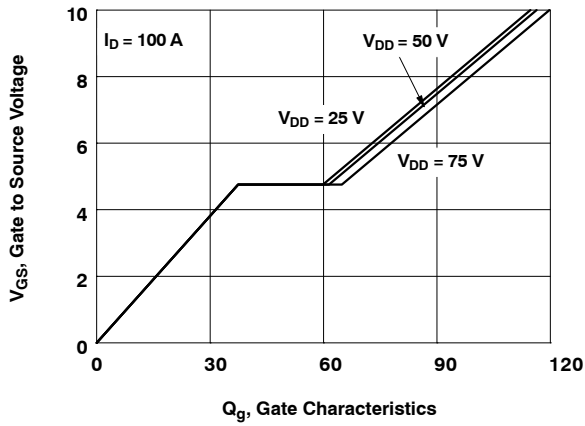


Figure 7. Gate Charge Characteristics

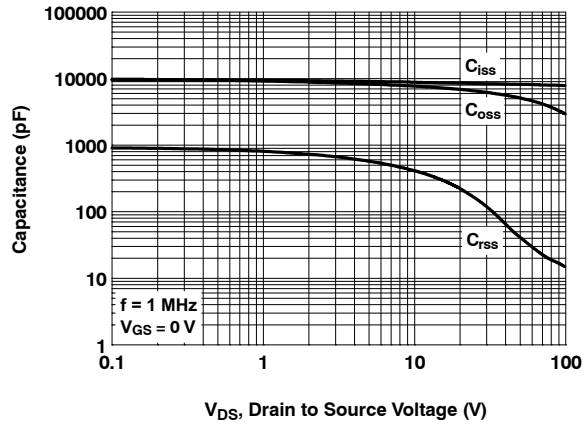


Figure 8. Capacitance vs. Drain to Source Voltage

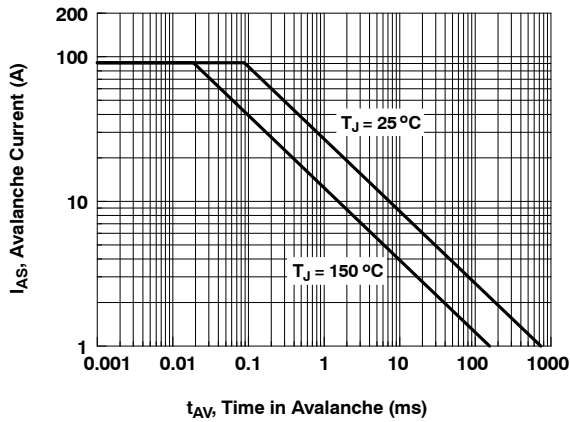


Figure 9. Unclamped Inductive Switching Capability

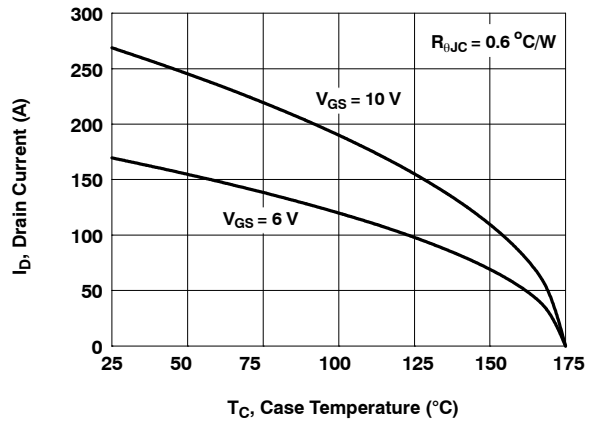


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

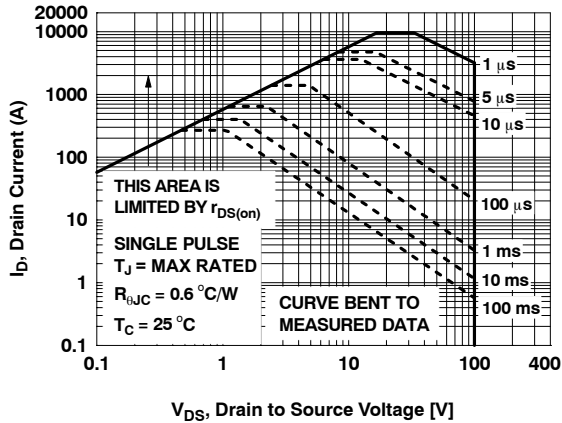


Figure 11. Forward Bias Safe Operating Area

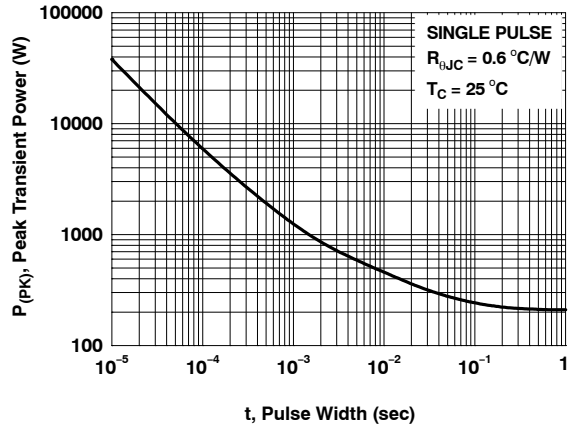


Figure 12. Single Pulse Maximum Power Dissipation

FDB1D7N10CL7

TYPICAL CHARACTERISTICS (Continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

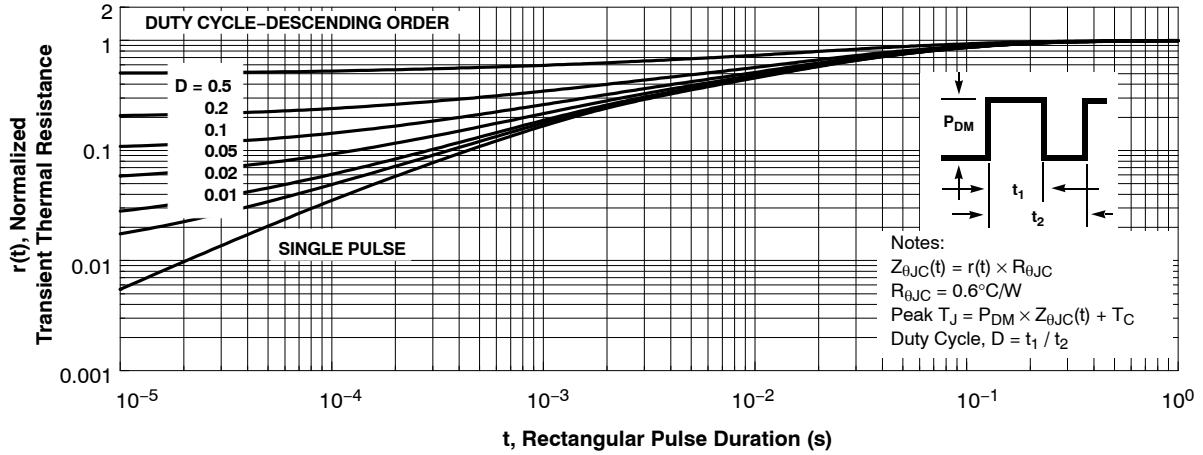


Figure 13. Normalized Max Junction to Case Transient Thermal Response Curve

POWERTRENCH is registered trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

MECHANICAL CASE OUTLINE

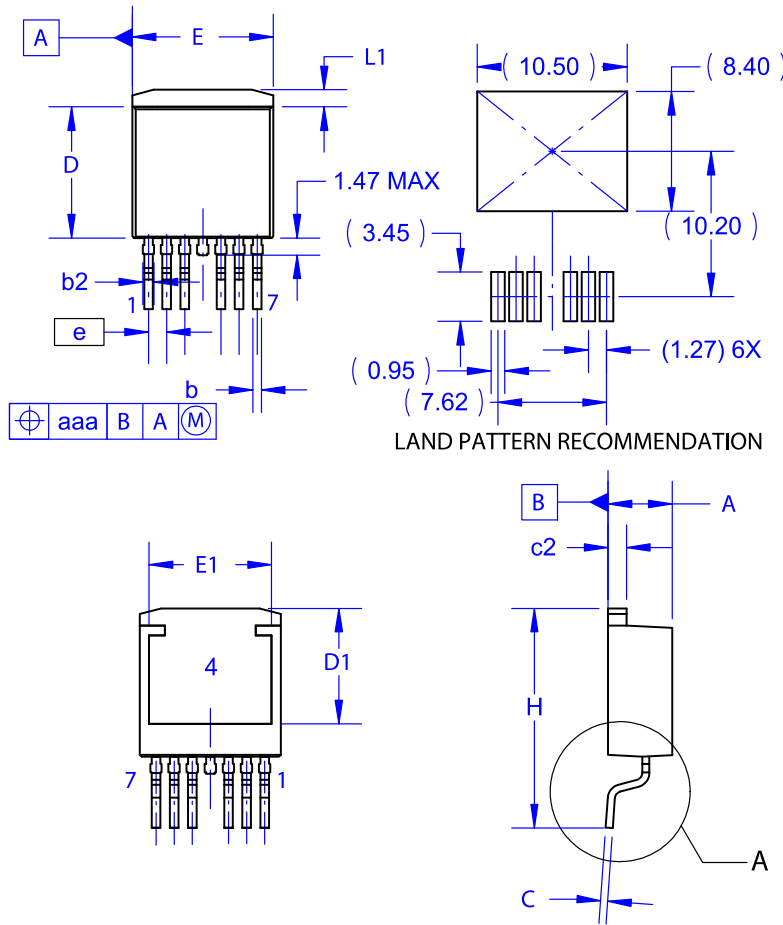
PACKAGE DIMENSIONS

ON Semiconductor®



D2PAK7 (TO-263 7 LD) CASE 418AY ISSUE C

DATE 15 JUL 2019



NOTES:

- A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. OUT OF JEDEC STANDARD VALUE.
- D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- F. LAND PATTERN RECOMMENDATION PER IPC-TO127P1524X465-8N.

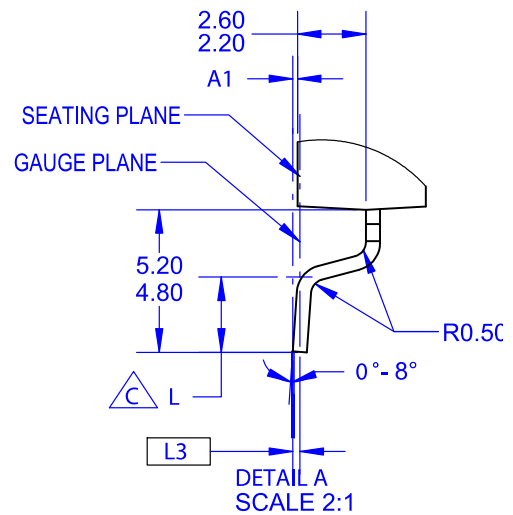
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	0.00	0.10	0.20
b2	0.70	0.80	0.90
b	0.50	0.60	0.70
c	0.40	0.50	0.60
c2	1.20	1.30	1.40
D	9.00	9.20	9.40
D1	7.70	~	~
E	9.70	9.90	10.20
E1	8.38	8.58	8.78
e	~	1.27	~
H	15.10	15.40	15.70
L	2.44	2.64	2.84
L1	1.00	1.20	1.40
L3	~	0.25	~
aaa	~	~	0.25

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



DOCUMENT NUMBER:	98AON13798G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	D2PAK7 (TO-263 7 LD)	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales