

# CAV93C76

## EEPROM Serial 8-Kb Microwire - Automotive Grade 1

### Description

The CAV93C76 is an EEPROM Serial 8-Kb Microwire Automotive Grade 1 device, which is configured as either registers of 16 bits (ORG pin at  $V_{CC}$  or Not Connected) or 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAV93C76 is manufactured using ON Semiconductor's advanced CMOS EEPROM floating gate technology. The device is designed to endure 1,000,000 program/erase cycles and has a data retention of 100 years. The device is available in 8-pin SOIC and TSSOP packages.

### Features

- Automotive AEC-Q100 Grade 1 ( $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ) Qualified
- High Speed Operation: 2 MHz
- 2.5 V to 5.5 V Supply Voltage Range
- Selectable x8 or x16 Memory Organization
- Self-timed Write Cycle with Auto-clear
- Software Write Protection
- Power-up Inadvertant Write Protection
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Sequential Read
- 8-pin SOIC and TSSOP Packages
- This Device is Pb-Free, Halogen Free/BFR Free and RoHS Compliant†

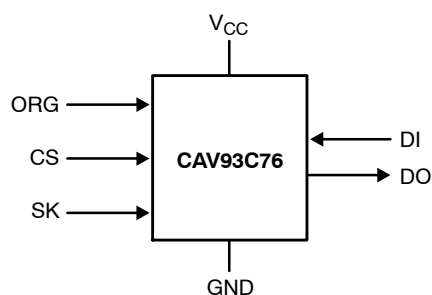


Figure 1. Functional Symbol

†For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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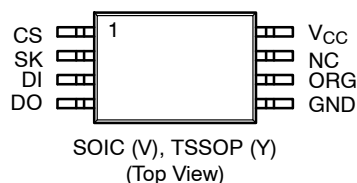


SOIC-8  
V SUFFIX  
CASE 751BD



TSSOP-8  
Y SUFFIX  
CASE 948AL

### PIN CONFIGURATION



### PIN FUNCTION

Pin Name	Function
CS	Chip Select
SK	Serial Clock Input
DI	Serial Data Input
DO	Serial Data Output
$V_{CC}$	Power Supply
GND	Ground
ORG	Memory Organization
NC	No Connection

**NOTE:** When the ORG pin is connected to  $V_{CC}$ , the x16 organization is selected. When it is connected to ground, the x8 organization is selected. If the ORG pin is left unconnected, then an internal pull-up device will select the x16 organization.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

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**Table 1. ABSOLUTE MAXIMUM RATINGS**

Parameters	Ratings	Units
Storage Temperature	-65 to +150	°C
Voltage on any Pin with Respect to Ground (Note 1)	-0.5 to +6.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The minimum DC input voltage is -0.5 V. During transitions, inputs may undershoot to -2.0 V for periods of less than 20 ns. Maximum DC voltage on output pins is  $V_{CC} + 0.5$  V, which may overshoot to  $V_{CC} + 2.0$  V for periods of less than 20 ns.

**Table 2. RELIABILITY CHARACTERISTICS** (Note 2)

Symbol	Parameter	Min	Units
$N_{END}$ (Note 3)	Endurance	1,000,000	Program / Erase Cycles
$T_{DR}$	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
3. Block Mode,  $V_{CC} = 5$  V, 25°C

**Table 3. D.C. OPERATING CHARACTERISTICS**

( $V_{CC} = +2.5$  V to +5.5 V,  $T_A = -40$ °C to +125°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Max	Units
$I_{CC1}$	Supply Current (Write)	Write, $V_{CC} = 5.0$ V		2	mA
$I_{CC2}$	Supply Current (Read)	Read, DO open, $f_{SK} = 2$ MHz, $V_{CC} = 5.0$ V		500	μA
$I_{SB1}$	Standby Current (x8 Mode)	$V_{IN} = GND$ or $V_{CC}$ CS = GND, ORG = GND		5	μA
$I_{SB2}$	Standby Current (x16 Mode)	$V_{IN} = GND$ or $V_{CC}$ CS = GND, ORG = Float or $V_{CC}$		3	μA
$I_{LI}$	Input Leakage Current	$V_{IN} = GND$ to $V_{CC}$		2	μA
$I_{LO}$	Output Leakage Current	$V_{OUT} = GND$ to $V_{CC}$ CS = GND		2	μA
$V_{IL1}$	Input Low Voltage	$4.5$ V $\leq V_{CC} < 5.5$ V	-0.1	0.8	V
$V_{IH1}$	Input High Voltage	$4.5$ V $\leq V_{CC} < 5.5$ V	2	$V_{CC} + 1$	V
$V_{IL2}$	Input Low Voltage	$2.5$ V $\leq V_{CC} < 4.5$ V	0	$V_{CC} \times 0.2$	V
$V_{IH2}$	Input High Voltage	$2.5$ V $\leq V_{CC} < 4.5$ V	$V_{CC} \times 0.7$	$V_{CC} + 1$	V
$V_{OL1}$	Output Low Voltage	$4.5$ V $\leq V_{CC} < 5.5$ V, $I_{OL} = 3$ mA		0.4	V
$V_{OH1}$	Output High Voltage	$4.5$ V $\leq V_{CC} < 5.5$ V, $I_{OH} = -400$ μA	2.4		V
$V_{OL2}$	Output Low Voltage	$2.5$ V $\leq V_{CC} < 4.5$ V, $I_{OL} = 1$ mA		0.2	V
$V_{OH2}$	Output High Voltage	$2.5$ V $\leq V_{CC} < 4.5$ V, $I_{OH} = -100$ μA	$V_{CC} - 0.2$		V

**Table 4. PIN CAPACITANCE** (Note 4)

Symbol	Test	Conditions	Min	Typ	Max	Units
$C_{OUT}$	Output Capacitance (DO)	$V_{OUT} = 0$ V			5	pF
$C_{IN}$	Input Capacitance (CS, SK, DI, ORG)	$V_{IN} = 0$ V			5	pF

4. These parameters are tested initially and after a design or process change that affects the parameter.

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**Table 5. POWER-UP TIMING** (Notes 6, 5)

Symbol	Parameter	Max	Units
$t_{PUR}$	Power-up to Read Operation	1	ms
$t_{PUW}$	Power-up to Write Operation	1	ms

5.  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated.

**Table 6. A.C. TEST CONDITIONS**

Input Rise and Fall Times	≤ 50 ns		
Input Pulse Voltages	0.4 V to 2.4 V	$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	
Timing Reference Voltages	0.8 V, 2.0 V	$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	
Input Pulse Voltages	$0.2 V_{CC}$ to $0.7 V_{CC}$	$2.5\text{ V} \leq V_{CC} \leq 4.5\text{ V}$	
Timing Reference Voltages	$0.5 V_{CC}$	$2.5\text{ V} \leq V_{CC} \leq 4.5\text{ V}$	
Output Load	Current Source $I_{OLmax}/I_{OHmax}$ ; $CL = 100\text{ pF}$		

**Table 7. A.C. CHARACTERISTICS**

( $V_{CC} = +2.5\text{ V}$  to  $+5.5\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Min	Max	Units
$t_{CSS}$	CS Setup Time	50		ns
$t_{CSH}$	CS Hold Time	0		ns
$t_{DIS}$	DI Setup Time	100		ns
$t_{DIH}$	DI Hold Time	100		ns
$t_{PD1}$	Output Delay to 1		0.25	μs
$t_{PD0}$	Output Delay to 0		0.25	μs
$t_{HZ}$ (Note 6)	Output Delay to High-Z		100	ns
$t_{EW}$	Program/Erase Pulse Width		5	ms
$t_{CSMIN}$	Minimum CS Low Time	0.25		μs
$t_{SKHI}$	Minimum SK High Time	0.25		μs
$t_{SKLOW}$	Minimum SK Low Time	0.25		μs
$t_{SV}$	Output Delay to Status Valid		0.25	μs
$SK_{MAX}$	Maximum Clock Frequency	DC	2000	kHz

6. This parameter is tested initially and after a design or process change that affects the parameter.

**Table 8. INSTRUCTION SET** (Note 7)

Instruction	Start Bit	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A10-A0	A9-A0			Read Address AN- A0
ERASE	1	11	A10-A0	A9-A0			Clear Address AN- A0
WRITE	1	01	A10-A0	A9-A0	D7-D0	D15-D0	Write Address AN- A0
EWEN	1	00	11XXXXXXXXXX	11XXXXXXXXXX			Write Enable
EWDS	1	00	00XXXXXXXXXX	00XXXXXXXXXX			Write Disable
ERAL	1	00	10XXXXXXXXXX	10XXXXXXXXXX			Clear All Addresses
WRAL	1	00	01XXXXXXXXXX	01XXXXXXXXXX	D7-D0	D15-D0	Write All Addresses

7. Address bit A10 for the 1,024x8 org. and A9 for the 512x16 org. are "don't care" bits, but must be kept at either a "1" or "0" for READ, WRITE and ERASE commands.

**Device Operation**

The CAV93C76 is a 8192-bit nonvolatile memory intended for use with industry standard microprocessors. The CAV93C76 can be organized as either registers of 16 bits or 8 bits. When organized as X16, seven 13-bit instructions control the read, write and erase operations of the device. When organized as X8, seven 14-bit instructions control the read, write and erase operations of the device. The CAV93C76 operates on a single power supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the device is a logical "1" start bit, a 2-bit (or 4-bit) opcode, 10-bit address (an additional bit when organized X8) and for write operations a 16-bit data field (8-bit for X8 organizations). The most significant bit of the address is "don't care" but it must be present.

**Read**

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAV93C76 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay ( $t_{PD0}$  or  $t_{PD1}$ ).

For the CAV93C76, after the initial data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the device will automatically increment to the next address and shift out the next data word in a sequential READ mode. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches the end of the address space, then loops back to address 0. In the sequential READ mode, only the initial data word is preceded by a dummy zero bit. All subsequent data words will follow without a dummy zero bit.

**Write**

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of  $t_{CSMIN}$ . The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAV93C76 can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before it is written into.

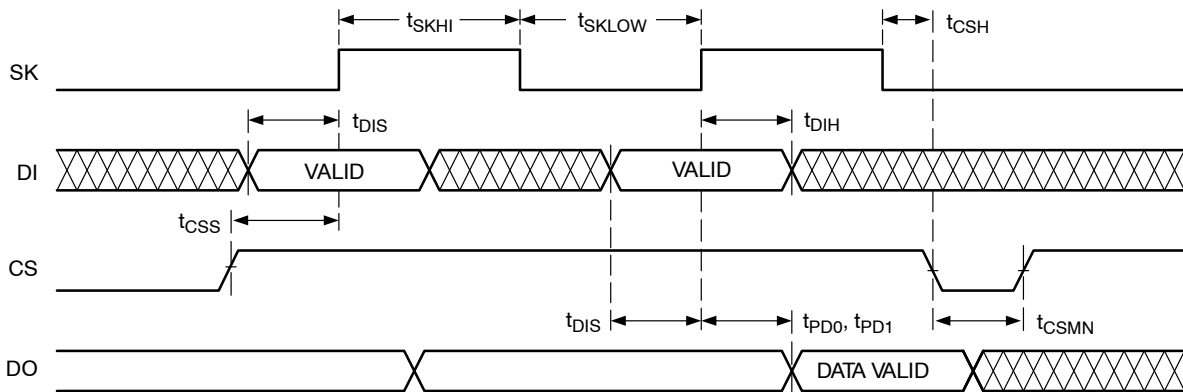
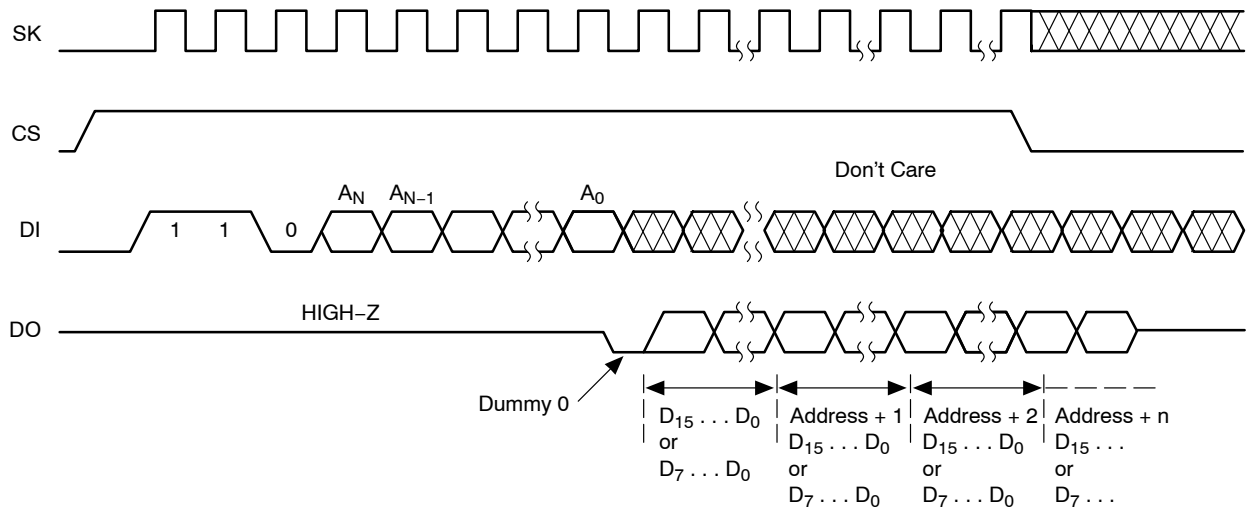
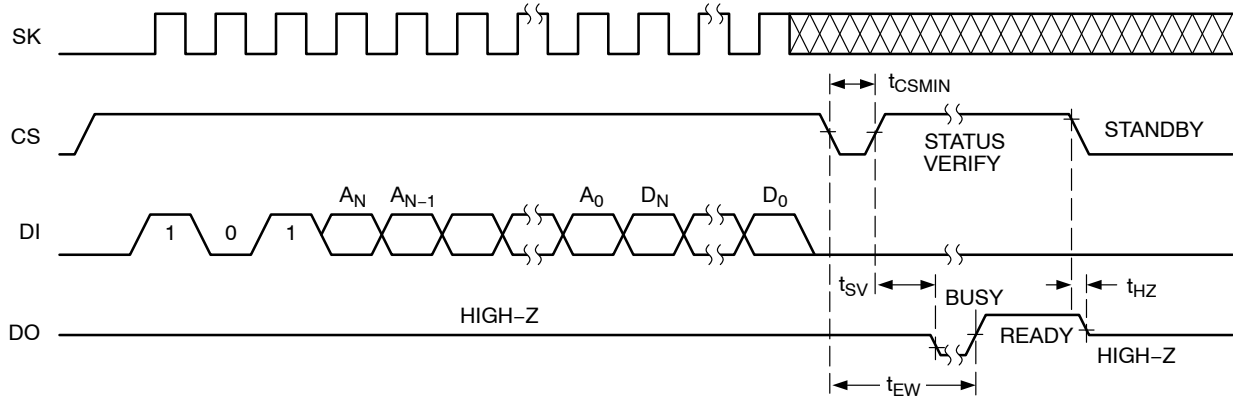


Figure 2. Synchronous Data Timing

# CAV93C76



**Figure 3. READ Instruction Timing**



**Figure 4. WRITE Instruction Timing**

**Erase**

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of  $t_{CSMIN}$ . The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAV93C76 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical “1” state.

**Erase/Write Enable and Disable**

The CAV93C76 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAV93C76 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

**Erase All**

Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of  $t_{CSMIN}$ . The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAV93C76 can be

determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical “1” state.

**Write All**

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of  $t_{CSMIN}$ . The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAV93C76 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

*Note 1: After the last data bit has been sampled, Chip Select (CS) must be brought Low before the next rising edge of the clock (SK) in order to start the self-timed high voltage cycle. This is important because if CS is brought low before or after this specific frame window, the addressed location will not be programmed or erased.*

**Power-On Reset (POR)**

The CAV93C76 incorporates Power-On Reset (POR) circuitry which protects the device against malfunctioning while  $V_{CC}$  is lower than the recommended operating voltage.

The device will power up into a read-only state and will power-down into a reset state when  $V_{CC}$  crosses the POR level of ~1.3 V.

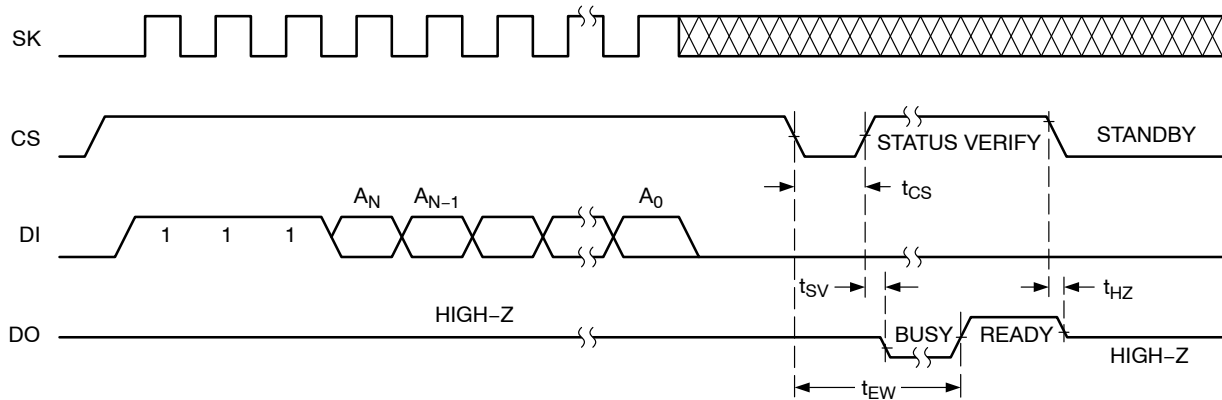


Figure 5. ERASE Instruction Timing

# CAV93C76

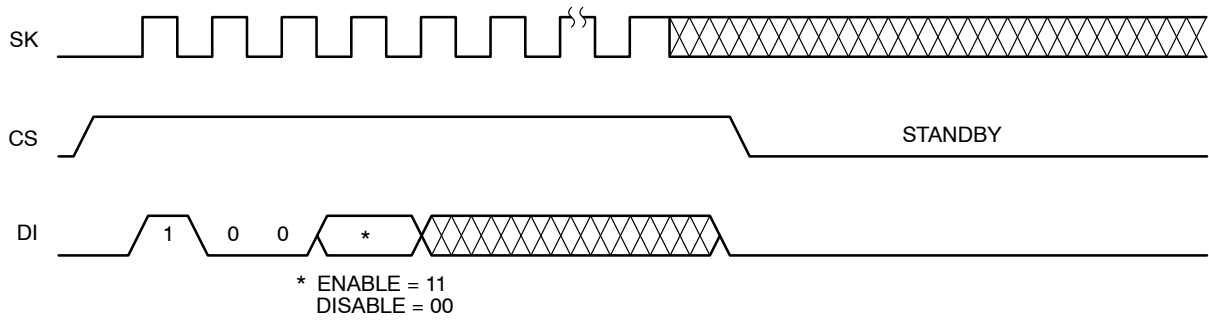


Figure 6. EWEN/EWDS Instruction Timing

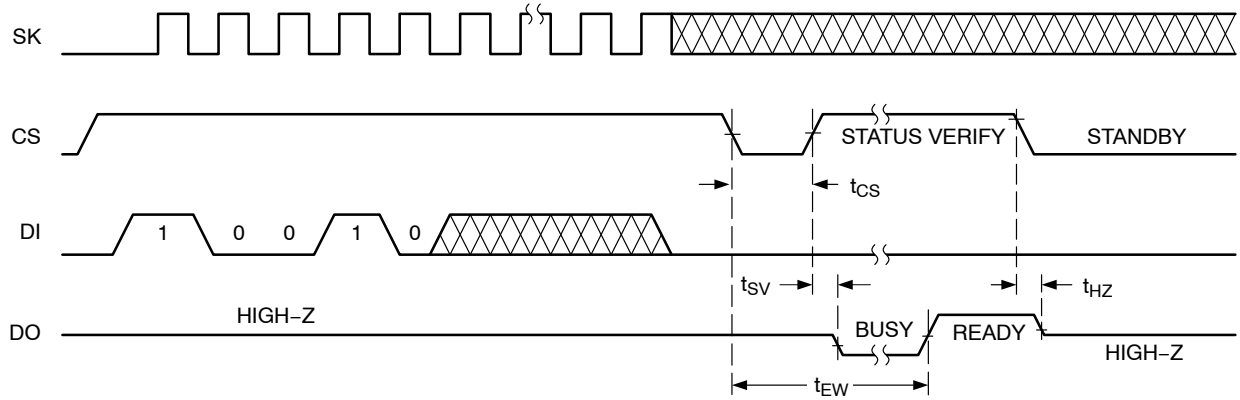


Figure 7. ERAL Instruction Timing

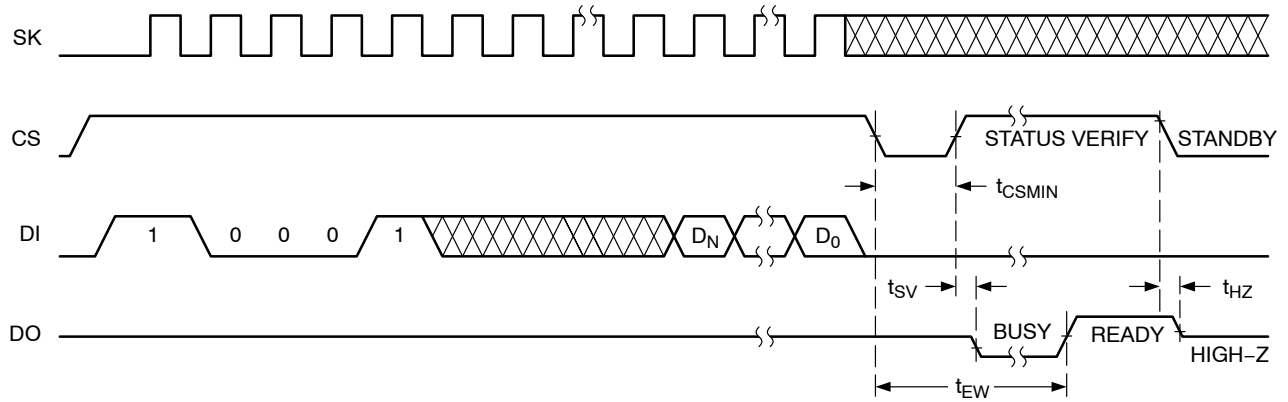


Figure 8. WRAL Instruction Timing

# CAV93C76

## ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Lead Finish	Shipping†
CAV93C76VE-GT3	93C76D	SOIC-8, JEDEC	-40°C to +125°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAV93C76YE-GT3	M76D	TSSOP-8	-40°C to +125°C	NiPdAu	Tape & Reel, 3,000 Units / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

8. All packages are RoHS-compliant (Lead-free, Halogen-free).

9. The standard lead finish is NiPdAu.

10. For additional package and temperature options, please contact your nearest ON Semiconductor sales office.

11. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at [www.onsemi.com](http://www.onsemi.com)

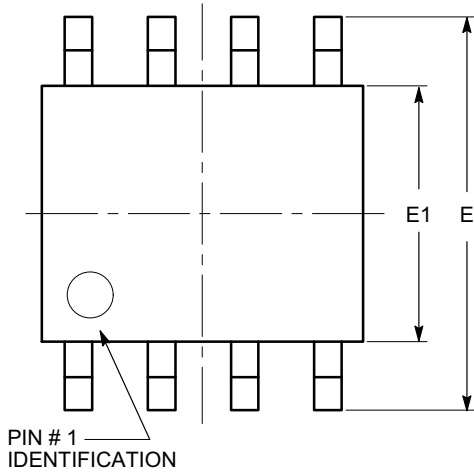


**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**



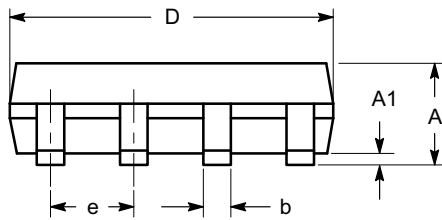
**SOIC-8, 150 mils**  
**CASE 751BD**  
**ISSUE O**

DATE 19 DEC 2008

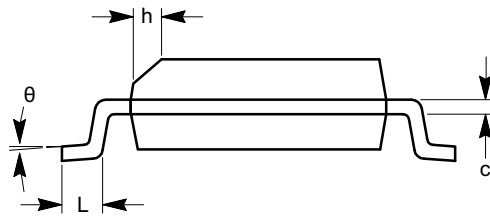


**TOP VIEW**

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
$\theta$	0°		8°



**SIDE VIEW**



**END VIEW**

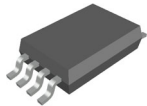
**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

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<b>DESCRIPTION:</b>	<b>SOIC 8, 150 MILS</b>	<b>PAGE 1 OF 1</b>

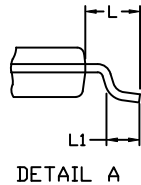
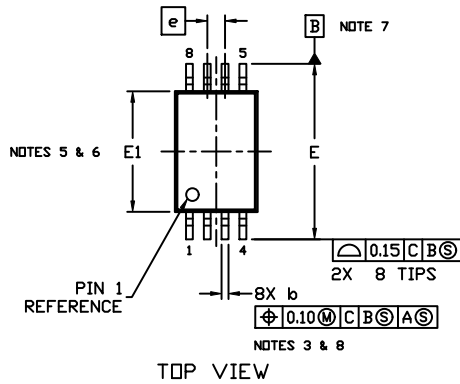
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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



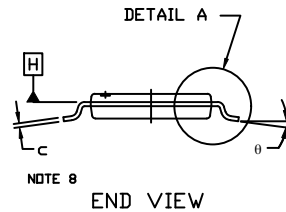
**TSSOP8, 4.4x3.0, 0.65P**  
CASE 948AL  
ISSUE A

DATE 20 MAY 2022



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5, 2009..
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION **b** DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL NOT BE 0.15 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION **D** DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
5. DIMENSION **E1** DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS **D** AND **E1** ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM **H**.
7. DATUMS **A** AND **B** ARE TO BE DETERMINED AT DATUM **H**.
8. DIMENSIONS **b** AND **c** APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP..
9. **A1** IS DEFINED AS THE LOWEST VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY..



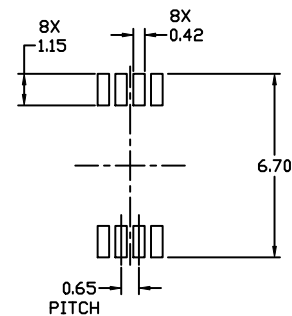
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.05	---	0.15
A2	0.80	0.90	1.05
b	0.19	---	0.30
c	0.09	---	0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.70
θ	0°	---	8°

**GENERIC MARKING DIAGRAM\***



- XXX = Specific Device Code
- Y = Year
- WW = Work Week
- A = Assembly Location
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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<b>DESCRIPTION:</b>	<b>TSSOP8, 4.4X3.0, 0.65P</b>	<b>PAGE 1 OF 1</b>

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