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Automotive Power Delivery Solutions for Xilinx Zynq® UltraScale+ MPSoC



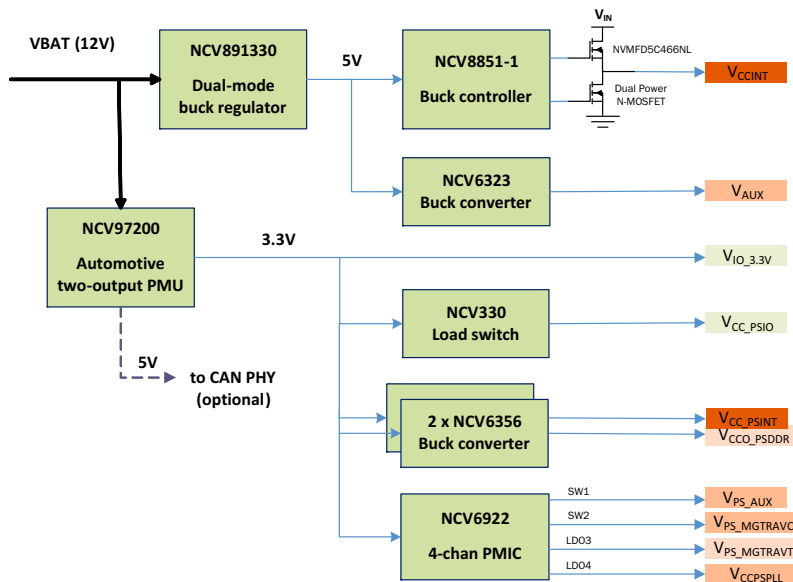
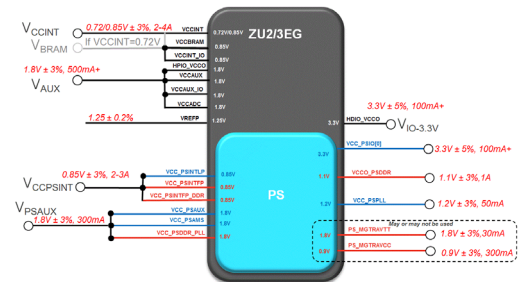
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SUMMARY

The goal of this Application Note is to present automotive power delivery solutions for Xilinx's Zynq UltraScale+, a family of programmable MPSoCs that can enable development of safety-critical Advanced Driver Assistance Systems (ADAS) and Autonomous Driving (AD) systems. The Xilinx Automotive XA Zynq UltraScale+ MPSoC family is qualified according to AEC-Q100 test specifications with full ISO 26262 ASIL C level certification. A basic description of devices in the family can be found at [UltraScale Architecture and Product Data Sheet: Overview](#) (DS890). Even for designs centered on a single family of devices, power management requirements are diverse and often unique to a customer design. As a result, no single power management proposal can provide an optimal solution. This Application Note covers a couple of different applications and proposes alternative power delivery architectures to accommodate variations in the requirements from different designs. This approach allows more optimized solutions that balance out design goals such as PCB area, BOM cost, power efficiency, and scalability. All individual devices fully adhere to the AEC-Q100 automotive quality management process for grade 1 or 2. The proposed architectures are also compatible up to ASIL C and ASIL D levels of Functional Safety, which can be achieved with the addition of appropriate monitoring and controlling functions.

APPLICATION NOTE



APPLICATIONS INFORMATION

Power Domains and Sequencing

A Zynq UltraScale+ MPSoC consists of the two major underlying blocks Processor System (PS) and Programmable Logic (PL) in isolated power domains. PS acts as one standalone SoC and is able to boot and support all its own features without powering on the PL.

PS has two internal power domains, the low-power domain (LPD) must operate before the full-power domain (FPD) can function. However, LPD and FPD can be powered simultaneously. PL has a single power domain referred to as PLPD.

As a highly integrated MPSoC, the Zynq UltraScale+ can require 10 or more independent rails split between PS and PL, the exact number and currents depending on the device complexity and application. To achieve minimum current draw and ensure proper power-up, there are constraints in the order the power rails should be powered on and off within the power domains LPD, FPD, and PLPD. An explanation of the recommended power supply sequencing can be found at [Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics](#) (DS925).

As a first guidance, the block diagrams in this Application Note show the rails classified into the four different color-coded groups below for power-on time sequence, following recommendations from DS925.



Figure 1. Color Code for Sequencing

The green “no spec” group includes power rails for which no sequencing information is available and whose time sequence is considered non-critical. The recommended power-off sequence is the reverse of the power-on sequence above to achieve minimum current draw.

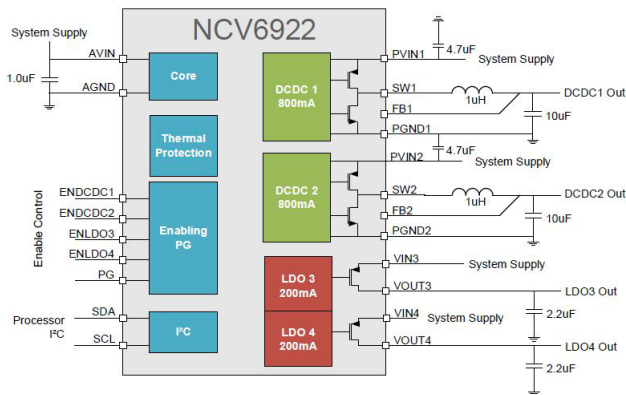


Figure 2. Individual Enable Control

The desired sequencing can be generated by an external control circuitry or MCU that monitors the power rails and

generates appropriate enable signals to the regulators. Each power rail should be controlled by an individual enable signal. For example (Figure 2), the PMIC NCV6922 has enable signals dedicated to each one of its DC/DC converters and LDO regulators.

Functional Safety Considerations

In safety-critical applications the correct MPSoC operation can be judged key to the system safety. In those cases power management failures potentially impacting operation must be detected and controlled by appropriate circuitry to comply with the ISO 26262 norms and required ASIL level.

The key point is to formally specify in which ways the power delivery circuit can impact the correct operation of the MPSoC, as well as the other supplied peripherals, by writing clear Technical Safety Requirements (TSR) at a system level. Those TSRs should in principle be derived from the system-level Safety Goal(s) and rippled down through the different components within the system. Therefore, they depend on the specific application and Zynq UltraScale+ device. As an example, these are some possible TSRs that may be needed:

- TSR1–X: Correct voltage levels (i.e. $\pm 3\%$ on the main rails and 5% on others) shall be supplied to the MPSoC
- TSR2: Correct start-up sequence shall be performed
- TSR3: Required shutdown sequence shall be performed

A high-level solution capable of meeting these TSRs is presented at the end of this Application Note.

Power Requirements – Applications #1 and #2

Two example applications are provided along with typically required power rails and currents. Application #1 is representative of ZU2EG and ZU3EG devices and can, for instance, be used in smart sensors. Application #2 covers ZU5EG, ZU6EG, and ZU7EG devices, appropriate for more complex applications, such as sensor fusion. Consult DS925 for additional information on the DC and AC switching characteristics.

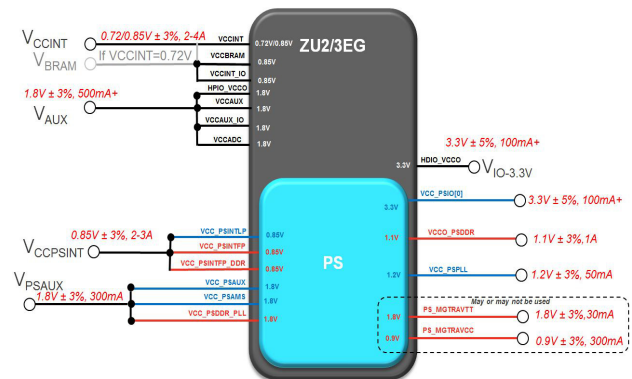


Figure 3. Application #1 Power Rails

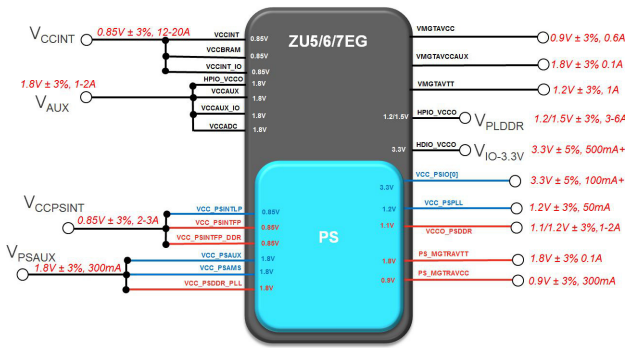


Figure 4. Application #2 Power Rails

It is convenient to split the power rails between the PS and PL power domains for design modularity and to allow sequencing to be properly separated and controlled. The tables below summarize voltage, current, and power requirements for PS and PL.

It can be readily seen in Figure 5 that requirements for the PS domain are quite similar for Application #1 and Application #2, which allows a single solution to cover both applications. On the other hand, the PL domain in Figure 6 shows dramatic differences in the number of power rails and currents for each application. That requires distinct architectural solutions and scalability to cover a wide spectrum of applications.

V _(RAIL)	Application #1			Application #2		
	Voltage	Current	P(max)	Voltage	Current	P(max)
CC_PSINT	0.85V	2-3A	2.55W	0.85V	2-3A	2.55W
CCO_PSDDDR	1.1V	1-2A	2.20W	1.1/1.2V	1-2A	2.20W
CC_PSIOR	3.3V	100mA+	0.33W+	3.3V	500mA+	1.65W+
PSAUX	1.8V	300mA	0.54W	1.8V	300mA	0.54W
PS_MGTRAVCC	0.9V	300mA	0.27W	0.85V	300mA	0.26W
PS_MGTRAVTT	1.8V	60mA	0.11W	1.8V	100mA	0.18W
CC_PSPLL	1.2V	50mA	0.06W	1.2V	50mA	0.06W

Figure 5. Power Rails in PS

V _(RAIL)	Application #1			Application #2		
	Voltage	Current	P(max)	Voltage	Current	P(max)
CCINT	0.72-0.85V	2-4A	3.40W	0.85V	12-20A	17.00W
PLDDR				1.2-1.5V	3-6A	9.00W
AUX	1.8V	500mA+	0.90W+	1.8V	1-2A	3.60W
MGTAVTT				1.2V	1A	1.20W
MGTAVCC				0.9V	600mA	0.54W
IO_3.3V	3.3V	100mA+	0.33W+	3.3V	100mA+	0.33W+
MGTAVCCAUX				1.8V	100mA	0.18W

Figure 6. Power Rails in PL

Pre-regulation Schemes

Solutions proposed in this Application Note assume a 12 V automotive battery (V_{BAT}) as the primary power source. There is need for a first pre-regulation stage generating an intermediate voltage (e.g., 5 V or 3.3 V), followed by regulators/controllers for the individual rails. The designer should check the minimum operating V_{BAT} before selecting the intermediate voltage and pre-regulation. Choice for the pre-regulation is dictated in part by the total required power. In low-power applications, such as Application #1, a single step-down (“buck”) regulator may suffice.

One of the choices for pre-regulator is the NCV97200, a two-output Automotive PMU developed primarily for ASIL B systems. As such, it has features that may be useful with ASIL Decomposition in some applications:

- Switcher for optional 5 V @ 400 mA IVN supply (CAN physical layer)
- Window watchdog to monitor incoming signal from microcontroller
- Window output monitoring for under & overvoltage (both outputs)
- Independent bandgaps for supplies regulation and monitoring

Its primary switcher can deliver up to 2.5 A at 3.3 V, which does not provide enough power for most Zynq US+ applications. It is, however, usually adequate to cover the power needs of the PS rails.

An alternative is the dual-mode buck regulator NCV891330. It doesn’t have the additional features as in the NCV97200 but it can output 3.0 A at 5 V, or about 80% extra power. That may be enough to power both PS and PL rails in simpler cases, such as Application #1. As power increases, a second regulator may be added and pre-regulation for PS and PL rails can be split.

Finally, with total power in the range of tens of watts, a buck controller is advantageous and allows easy scalability. Adequate devices are the NCV891930 and the NCV881930, the former switching at 2 MHz and the latter allowing lower switching losses and higher power at a nominal 410 kHz switching frequency. A multiphase controller further expands scalability and efficiency for V_{CCINT} (PL), a rail where current in the range of 20 A may be required.

Application #1

With total power usually under 15 W, Application #1 requires no more than one or two buck regulators for pre-regulation. Two alternative solutions are proposed.

In cases where application can benefit from one or more of the NCV97200 features, that device can be used to pre-regulate at the least the PS rails. Figure 7 shows a dual pre-regulator configuration where an NCV891330 provides the additional power required for the PL rails.

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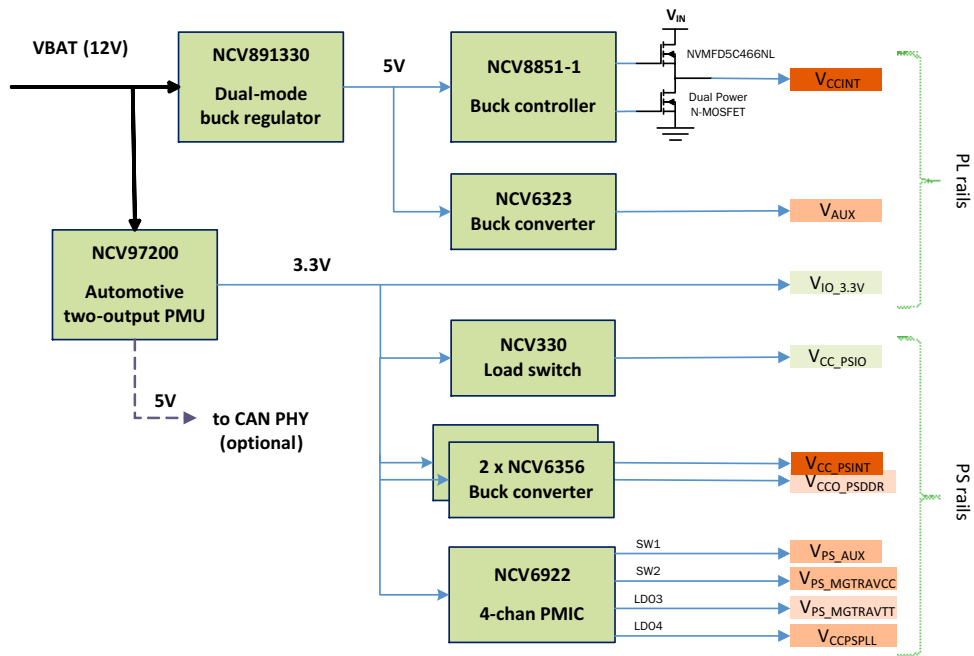


Figure 7. Application #1 with Dual Pre-Regulation

If features in the NCV97200 are not required, a single pre-regulator based on the NCV891330 can be used to power all rails in both PS and PL, decreasing PCB area and BOM cost in comparison to the previous configuration. That solution is shown in Figure 8 below.

The individual rails are generated from the 5 V or 3.3 V intermediate voltage provided by pre-regulation through low-voltage regulators/controllers. Some of them are isolated and other ones are grouped together into the NCV6922 PMIC.

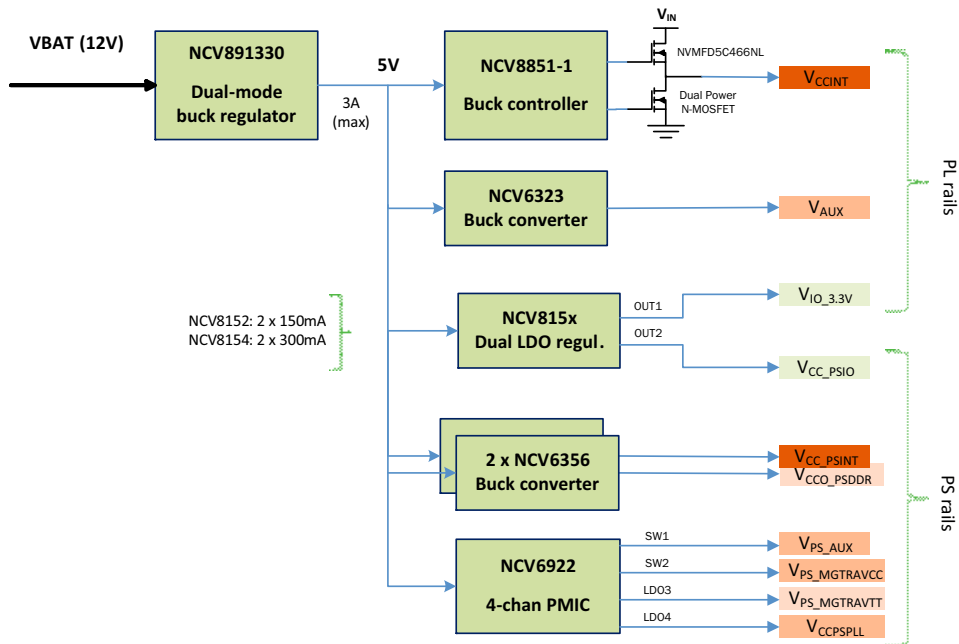


Figure 8. Application #1 with Single Pre-Regulation

Application #2

The higher total power required in Application #2, together with the variety in the number of power rails and currents in the PL domain, recommend that the PS and PL rails are generated from two separate intermediate voltages.

The PS rails can be handled by either the NCV97200 or by the NCV891330, depending on the system functional requirements. Those options are depicted in Figure 9 and Figure 10, respectively. Note again that the latter solution can deliver more power.

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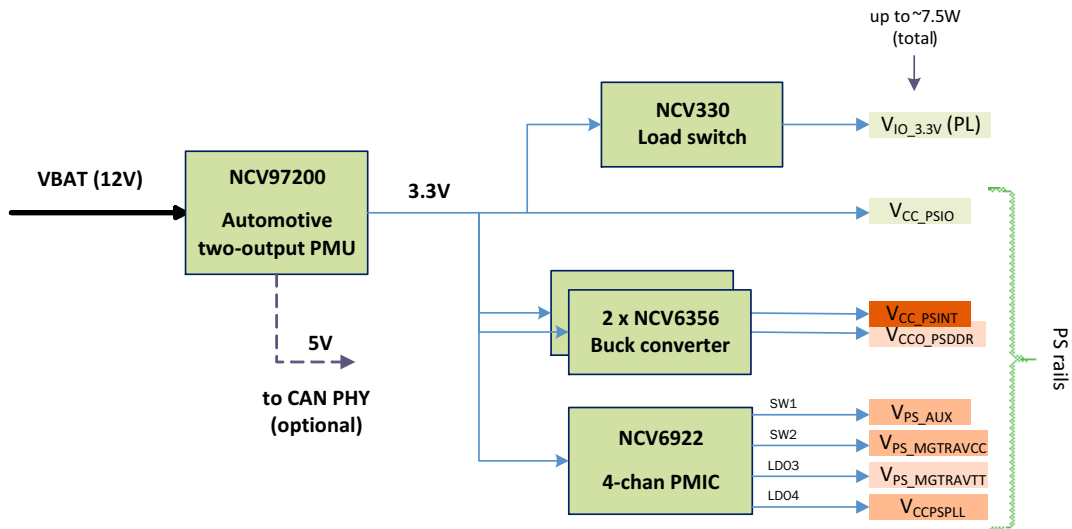


Figure 9. PS Rails in Application #2 with NCV97200

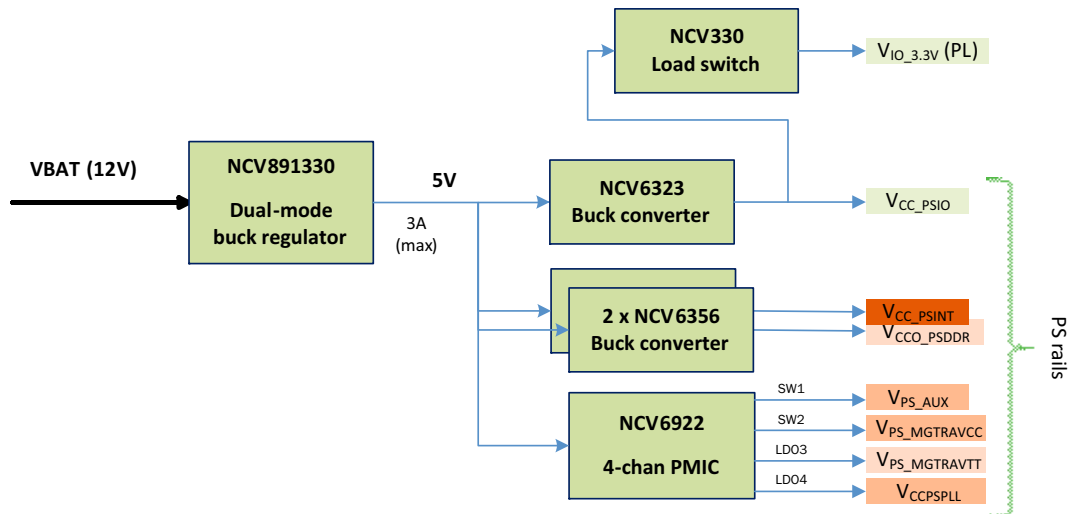


Figure 10. PS Rails in Application #2 with NCV891330

The PL rails should be powered by a buck controller, either the NCV891330 or the NCV881930, depending on the total power and switching frequency requirements. This is shown in Figure 11.

The individual rails are generated from a 5 V intermediate voltage through low-voltage regulators/controllers or PMIC. The NCV6922 PMIC offers two spare outputs that

may be used to power peripherals in the system (MCUs, memories, etc.).

Any additional power requirements can be met by a wide variety of voltage regulators, controllers, and DDR termination regulators found at the ON Semiconductor Power Management portfolio.

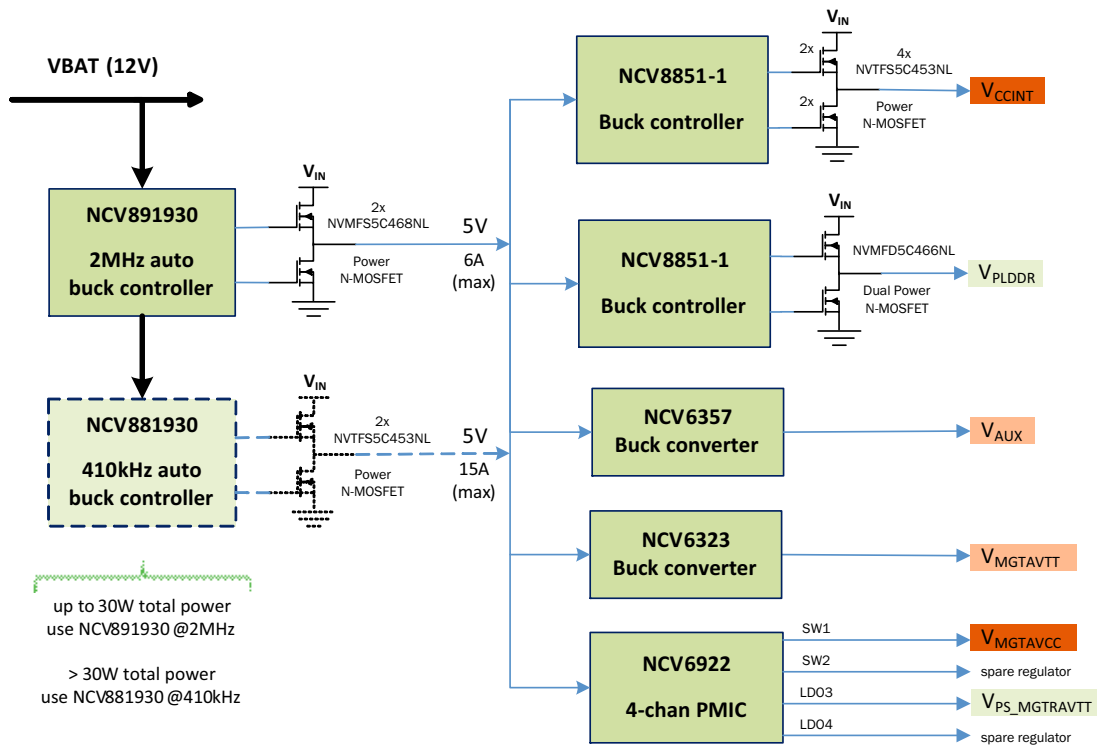


Figure 11. PL Rails in Application #2

Scalability

BOM cost and efficiency can be optimized by an adequate choice of the switches driven by the pre-regulation buck controllers. The power MOSFETs shown are proposed for Application #2, depending on the required output current. Devices for other current conditions can be researched at the ON Semiconductor MOSFET parametric table. The companion MOSFETs to the NCV8851-1 post-controllers (rails V_{CCINT} and V_{PLDDR}) should also be dimensioned for the actual load currents.

Current scalability can be further expanded by using a multiphase controller, a solution widely adopted for rails such as V_{CCINT} , which has to cover a wide range of current over the spectrum of applications. As shown in Figure 12, successive phases can be activated as the need for current increases, keeping near-optimal efficiency. Figure 13 shows use of the NCV81276 multiphase buck controller with up to four FDMF5833_F085 Dr.MOS smart power stages, allowing for easy current scalability. Dynamic Phase Management is also possible for optimal efficiency by tracking variable load currents.

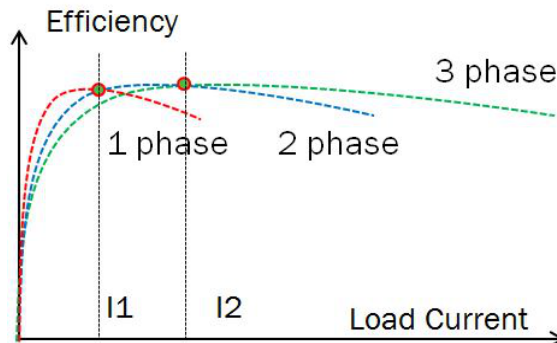


Figure 12. Efficiency Optimization with Multiphase

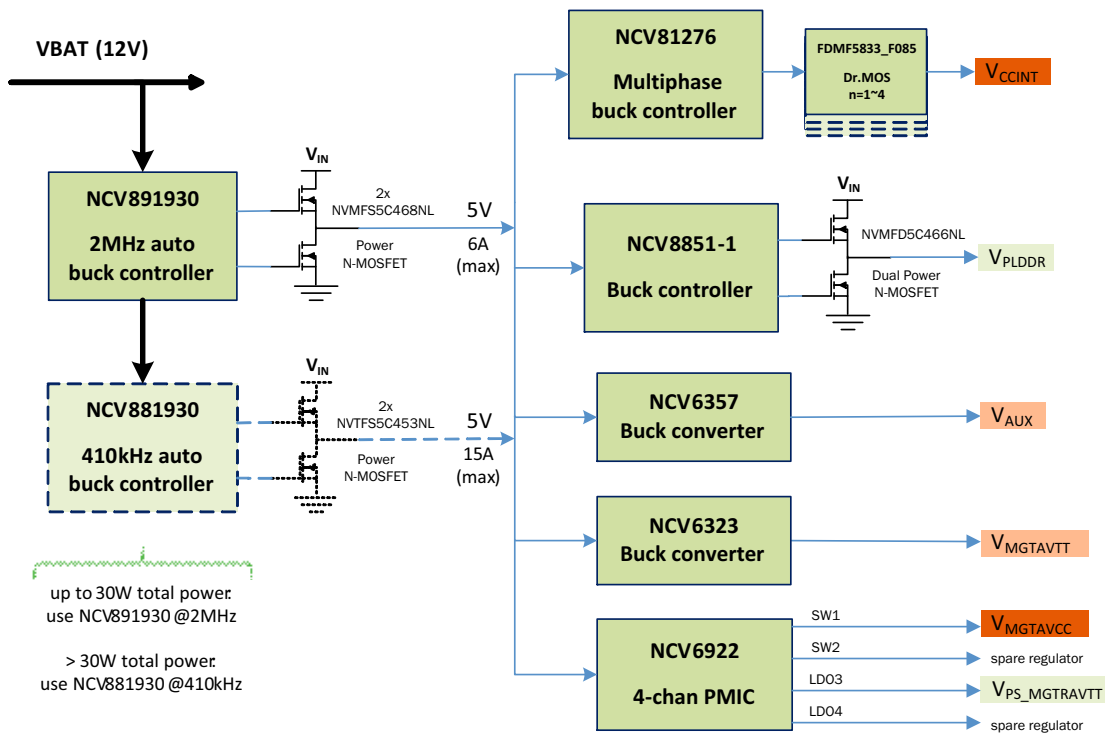


Figure 13. Multiphase for V_{CCINT} in Application #2

System Solution for Functional Safety

The Xilinx Automotive XA Zynq UltraScale+ MPSoC family is currently qualified to ISO 26262 ASIL C. That should also be the Functional Safety requirement at the system level for many of its applications, although ASIL D is also possible. An exact system solution for Functional Safety depends on a number of factors and is out of the scope of this Application Note. As such, only general guidelines to achieve ASIL C will be provided along with the underlying assumptions.

First, the safety requirements have to be clearly defined to allow work on the architecture of the safety mechanisms. In order to achieve ASIL C metrics at system level, it's very likely that most or all power rails will need to be covered through a continuous monitoring safety mechanism.

It is possible to use automotive-qualified devices without ASIL level (QM devices), by adding external monitoring devices to the system. That is done according to the "ASIL Decomposition", where redundant and independent safety requirements are assigned to the regulation devices and to the monitoring devices.

Figure 14 shows an example where a monitoring device supplied through the battery was selected to keep the regulation and monitoring independent. It also shows that

a monitoring device developed according to at least ASIL C is required. Other schemes for redundancy and decomposition could alternatively be used.

It is worth noting that in some cases the Safety MCU could be used as the monitoring device. In any case, care should be taken with the speed requirements, so that the safe state can be reached quickly enough to satisfy the Fault Tolerant Time Interval (FTTI) at the system level.

The "Monitor Device" in the example will do the sequential power-up of the rails, as well as the monitoring. At the previous section "Functional Safety considerations", sequencing was defined to be safety critical under TSR2, so it would be important that both sequencing and monitoring are sufficiently independent to avoid common failure modes. This can be done through two separate devices, or through a single device with two independent islands for sequencing and monitoring. Similar reasoning can also be applied to the shut-down sequence.

Last but not least, QM level devices developed on an automotive-qualified flow in a robust technology were selected for the voltage generation. Their high reliability figures are fundamental to keep real probability of failure under the acceptable Probabilistic Metric for random Hardware Failures (PMHF).

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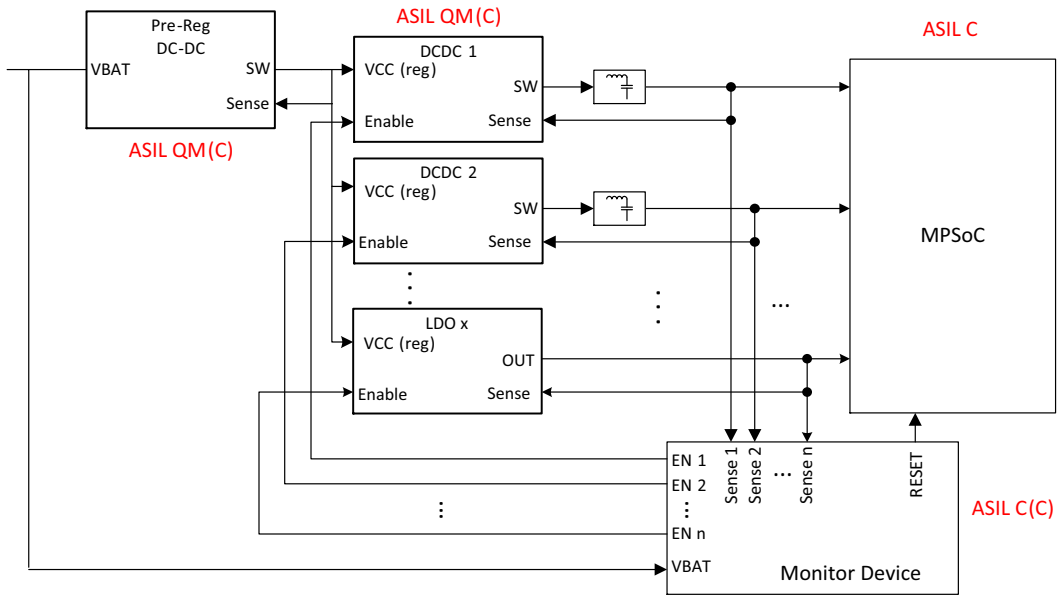



Figure 14. Block Diagram for ASIL C Decomposition

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