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Implementing a 12 V / 240 W Power Supply with the NCP4303B, NCP1605 and NCP1397B

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APPLICATION NOTE

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Overview

The following document describes a 12 V / 20 A output switch mode power supply (SMPS) intended for use as an ATX power supply main converter or as an All−In−One PC power supply. The reference design circuit consists of a double sided 135 x 200 mm printed circuit board with a height of only 35 mm. An overview of the entire SMPS architecture is provided in Figure 1. Careful consideration was given to optimizing performance while minimizing the total solution cost.

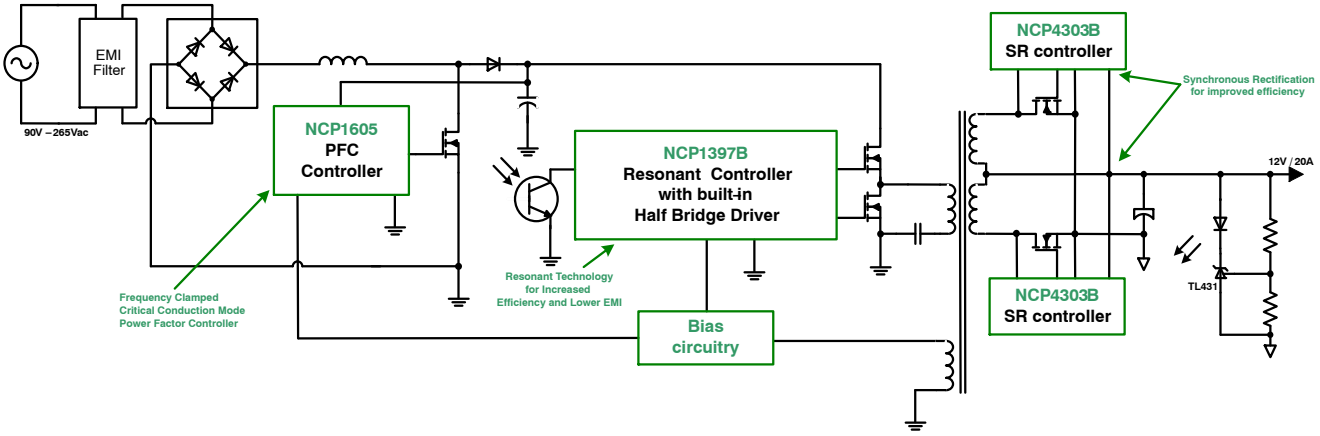

Figure 1. Demoboard Block Diagram

Architecture Overview

The circuit utilizes the NCP1605 for an active power factor correction front end. This stage provides a well regulated PFC output voltage that allows optimization of the downstream converter. The NCP1605 controller operates using a Frequency Clamped Critical conduction Mode control technique. The SMPS stage uses a Half Bridge Resonant LLC topology since it improves efficiency, reduces EMI signature and provides better transformer utilization compared to conventional topologies. The NCP1397B controller is used to control the Half Bridge Resonant LLC converter. To maximize efficiency of the LLC power stage, Synchronous Rectification (SR) has been implemented on the secondary side. The NCP4303B SR controller is used to achieve accurate turn−on and turn−off of the SR MOSFETs.

In summary, the architecture selected for this reference design allows system optimization so that the maximum efficiency is achieved without significantly increasing the component cost and circuit complexity.

Demoboard Specification

Most of today's computing applications like ATX PC, game consoles and All−in−one PC use 12 V as the main power rail. This voltage is then further decreased to 5 V and 3.3 V by DC/DC step down converters. Because nearly all power passes through the 12 V output, it is critical that the efficiency of the main power stage be optimized. Most designs today utilize an LLC topology for the power stage to provide high efficiency at a reasonable cost. The LLC power stage provides inherently high efficiency results thanks to zero voltage switching (ZVS) on the primary side and zero current switching (ZCS) on the secondary side. Efficiency however decreases for higher output currents as the secondary RMS current reaches a high level. The solution for these losses on the secondary side is to use synchronous rectification instead of conventional rectifiers (Schottky diode). Consideration was also give to optimizing light and no load efficiency, which is particularly important in All−in−one PC SMPS that usually do not utilize an additional standby power supply.

Based on the above considerations, the following is the required specifications of the SMPS reference design:

Table 1. DEMOBOARD SPECIFICATION

Requirement	Min	Max	Unit
Input voltage (ac)	90	265	V
Output voltage (dc)	–	12	V
Output current	0	20	A
Total output power	0	240	W
Consumption for a 500 mW output load in STBY mode	–	1.7	W
Consumption for a 100 mW output load in STBY mode	–	1.2	W
No load consumption SR operating	–	870	mW
No load consumption SR turned off, no bypass Shottky used	–	1	W
Load regulation		20	mV

The NCP4303A/B provides the following beneficial features for SR implementation in an LLC power stage:

Precise Zero Current Detection with Adjustable Threshold

The NCP4303 SR controller provides a default Zero Current Detection (ZCD) threshold of 0 mV. A 100 μA current source on the CS input allows the customer to decrease this basic ZCD threshold by using a resistor in series with the CS input. The turn−off current threshold can therefore be precisely adjusted down to 0 A to maximize the SR MOSFET conduction time. The result is optimized system efficiency.

Typically 40 ns Turn−off Delay from Current Sense Input to Driver Output

Once the CS input detects that the secondary current has reached zero, it is necessary to turn−off the SR MOSFET as fast as possible. The extremely low 40 ns propagation delay of the NCP4303 assures that the SR MOSFET will be turned−off quickly, avoiding reverse current flow back into the transformer winding from the secondary filtering capacitor.

Automatic Parasitic Inductance Compensation Input

The high secondary RMS current in the LLC stage has a high di(t)/dt product that can induce a high error voltage on the parasitic inductances of the SR MOSFET package (TO220 for instance). Parasitic error voltages shift the drain to source voltage and affect the accuracy of the ZCD system. As a result, the SR MOSFET is turned−off prematurely and efficiency is decreased. NCP4303 offers a method to compensate for this effect via a special input that offsets the ZCD comparator threshold with a compensation voltage. Thanks to this feature, the ZCD comparator can perform precise detection independent of the secondary current di(t)/dt product. This technique allows the use of standard leaded SR MOSFETs, which can reduce assembly process costs (SMT MOSFETs usually require a more expensive PCB and soldering).

Current Sense Pin Capability of 200 V

The high voltage capability of the CS pin allows for direct connection to the SR MOSFET drain. This avoids the use of a high impedance series resistor which would delay the CS signal.

Disable Input to Enter Standby or Low Consumption Mode

The trigger/disable input integrates two functions: 1st it can be used to turn−off the SR MOSFET in Continuous Current Mode applications (like CCM flyback).

2nd it can be used to switch the controller into standby mode. The SR standby mode decreases SMPS power consumption when the output is not loaded. Parallel Schottky diodes can be used for conduction in this mode rather than the SR MOSFETs.

Adjustable Minimum On and Off Times Independent of V_{CC} Level

Due to the various impedances in the application (parasitic inductances and capacitances) spurious ringing can occur after the SR MOSFET is turned on or off. To overcome controller false switching due to this parasitic ringing, the NCP4303 utilizes adjustable minimum on and off times. The driver state cannot be changed during these minimum periods. The duration of the minimum on time and minimum off time can be adjusted independently of each other and independent of the IC V_{cc} level.

5 A / 2.5 A Peak Current Sink / Source Drive Capability

The SR MOSFETs for high current applications usually feature high input capacitance. The strong sink driver capability of the NCP4303 decreases the turn−off time and thus allows for optimized conduction time of the SR MOSFET.

Operating Voltage Range Up to 30 V

The NCP4303 V_{CC} input can be connected directly to the application output voltage without any additional pre−regulation. This feature simplifies driver implementation and reduces application cost.

Gate Driver Clamp of Either 12 V (NCP4303A) or 6 V (NCP4303B)

Some of today's SR MOSFETs provide low channel resistance for lower gate voltages (< 6 V). Thus it is beneficial to clamp the driver voltage at a lower level and reduce driving losses. This technique helps to maintain high efficiency, especially under medium and light load conditions. On the other hand, some MOSFETs still require higher gate voltage. NCP4303A provides 12 V gate driver clamp for these cases. Please refer to the datasheet for more

information and a detailed description of the NCP4303A/B SR controller.

Detailed Demoboard Description

A complete schematic of the demoboard is shown in Figure 58. As mentioned above, the SMPS is composed of three blocks. The PFC front stage accepts input voltages from 90 V ac / 60 Hz up to 265 V ac / 50 Hz and converts it to 395 Vdc nominal. The second block is the LLC power stage that converts the bulk voltage to 12 V / 20 A output. The third block is the synchronous rectification which replaces conventional Schottky rectifiers.

PFC Front Stage

The input voltage passes through an EMI filter (Figure 2), which protects the distribution network against noise generated by the SMPS. The EMI filter is composed of capacitors CY_1, CY_2, C_{33}, C_{47}, current compensated choke L_{15} and differential mode chokes L_{12}, L_{13}. Varistor R_{48} protects the SMPS from surges passed from the mains. Filtered ac voltage is rectified by a bridge rectifier B_1 and connected to the PFC power stage.

To minimize the risk of electrical shock after unplugging the power supply, X2 capacitor discharge circuitry is required. Usually safety resistors are used to perform this function. Such a solution however brings some disadvantages. The discharge time increases to unacceptable levels for higher X2 capacitor values. The power loss in the discharge resistors needs to be increased in order to decrease X2 capacitor discharge time. As a result, the no load consumption of the application suffers. To avoid this, a special discharge circuitry has been implemented in this design to minimize X2 capacitor discharge time, without impacting no load consumption. This circuit is composed of charge pump R_{19}, R_{43}, R_{53}, D_8, D_{10}, D_{11}, C_{14}, C_{30}, C_{31}, transistors Q_6, Q_8, discharge resistors R_{16}, R_{22} and auxiliary bias circuitry R_1, R_{21}, C_1, D_1. When the application is plugged into the mains, the charge pump provides voltage to the Q_8 MOSFET gate and keeps it turned−on. The drain of MOSET Q_8 pulls down the base of the transistor Q_6, which disconnects discharge resistors R_{16}, R_{22} from the HV input to improve no load efficiency. When the SMPS is disconnected from the mains, the charge pump no longer delivers any current and MOSFET Q_8 is turned−off. The auxiliary voltage remains on capacitor C_1 and therefore transistor Q_6 is turned−on and resistors R_{16} and R_{22} discharge the X2 capacitors via the bridge rectifier. The discharge time is shorter than one second. The power consumption of this circuitry is about 6.5 mW for 230 Vac input, a savings of about 86 mW compared to the standard solution with equivalent discharge time. Implementation of the proposed X2 capacitor discharge circuitry also helps to reduce conducted EMI emission because the SMPS designer is less limited by X2 capacitor size vs. discharge time ratio.

The rectified AC line is connected to the PFC front end stage (Figure 3). The PFC stage modulates input current to achieve a high power factor and also to prepare a pre−regulated voltage for the LLC power stage.

Energy is stored in coil L_7 when the MOSFET Q_4 is turned−on. The energy stored in coil L_7 during on time is added to the rectified voltage on capacitor C_{15} when MOSFET Q_4 is turned−off. The bulk capacitors C_{16} and C_{17} are thus charged through diode D_5. Bulk voltage is divided down by resistors R_{17}, R_{28}, R_{34}, R_{46} and R_{63}. The emitter follower Q_{10} is implemented to allow the use of a high impedance divider, which decreases the SMPS standby consumption. The output voltage from this emitter follower is used for two proposes: 1st to prepare skip mode function of the PFC stage and 2nd to provide the LLC controller with information about the bulk voltage (i.e. is it sufficient for operation of the LLC stage or not).

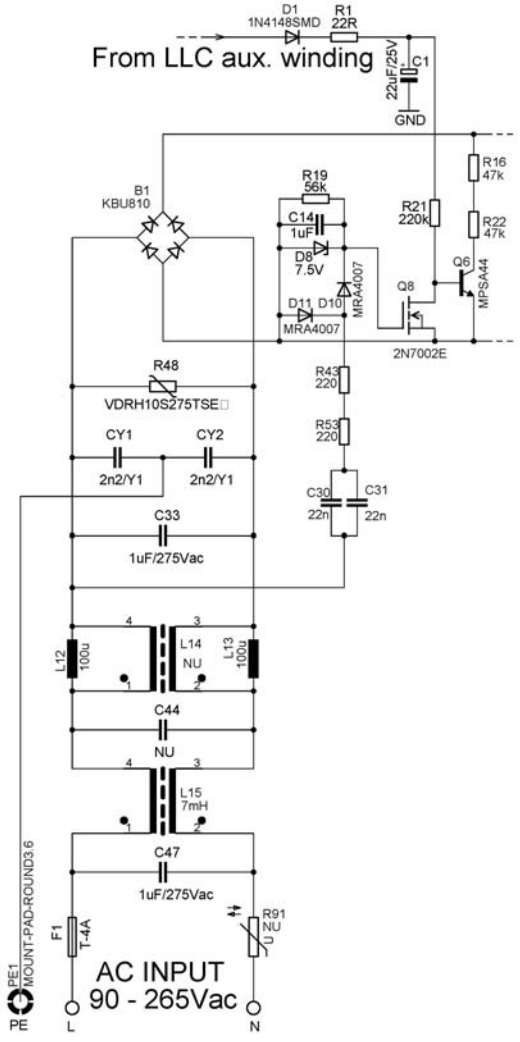

Figure 2. EMI Filter with X2 Capacitor Discharge Circuitry

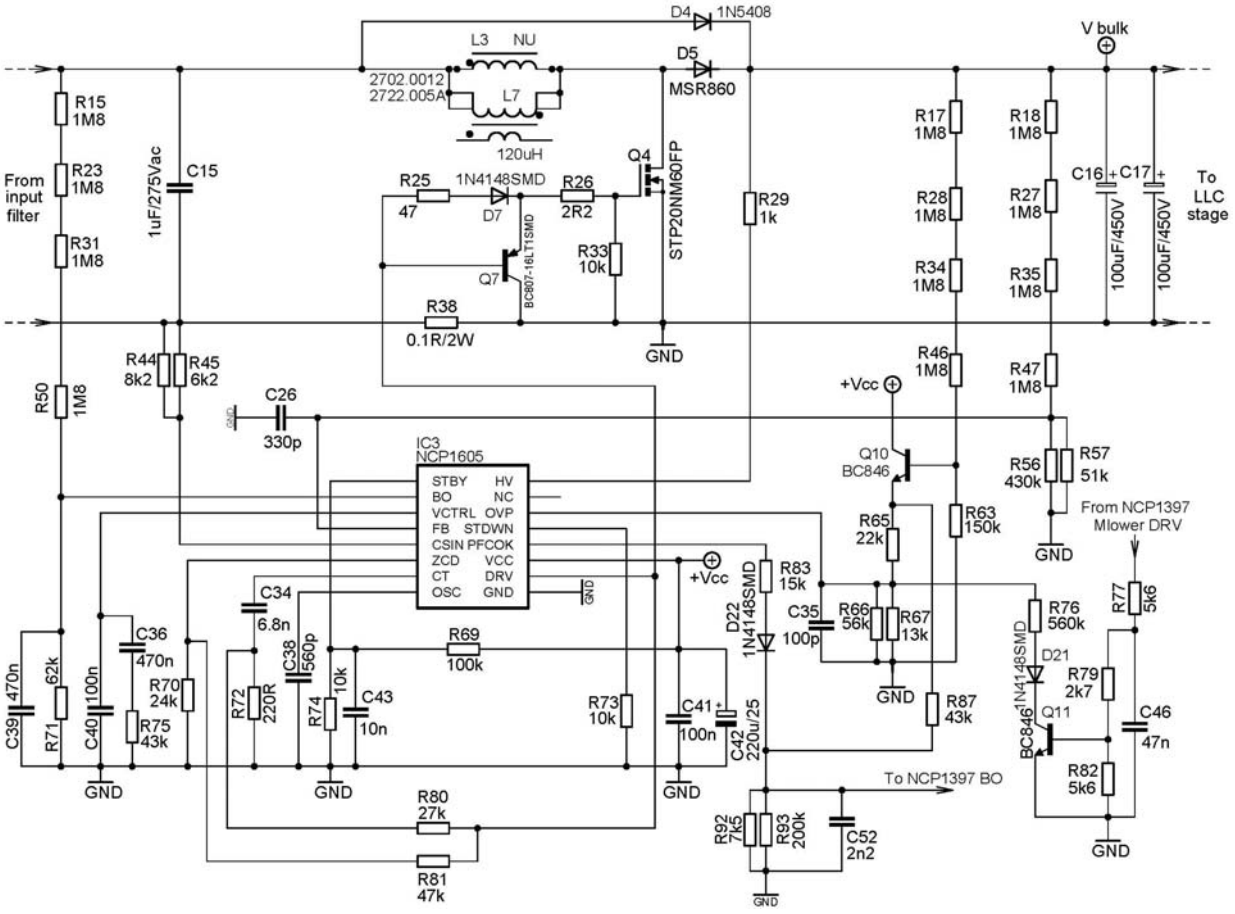

Figure 3. The PFC Stage Connection

The NCP1605 PFC controller features a skip mode function with thresholds that are fixed to the feedback (FB) regulation level. However, the bulk voltage ripple during skip mode would be too high for the LLC topology. Thus, in this design, the PFC skip mode is implemented via the PFC controller OVP input using external bipolar transistor Q_{11}. The operating frequency of the LLC stage increases when output load diminishes. The LLC stage enters skip mode and disables drivers when load further drops. Transistor Q_{11} is thus turned−off and resistor R_{76} is disconnected. The PFC OVP pin voltage thus increases above OVP threshold and PFC stage operation is interrupted. The output voltage then naturally drops and the LLC stage recovers operation – the Q11 is turned−on again and PFC stage operation is re−enabled as well because resistor R_{76} pulls down the OVP pin. With this method, the PFC is forced to periodically recharge the bulk capacitor during light load and no load conditions – the PFC skip mode with adjustable bulk voltage ripple is thus implemented. Because the skip mode is implemented externally via the OVP pin rather than via the standby input, it is necessary to bias the STBY pin above 0.3 V using resistor divider R_{69}, R_{74}.

Voltage from the Q_{10} transistor emitter is also divided down by divider R_{87}, R_{92}, R_{93} and used to control LLC stage operation via the NCP1397 brown out input. During the PFC stage startup there is no voltage available on the PFC_OK pin of IC_3 – the LLC stage thus can not start operation. The PFC_OK pin increases to 5 V after the PFC stage reaches regulation level. Current that is sourced by PFC_OK pin voltage and R_{83} resistor is added to the current flowing out from resistor R_{87} and together they create a voltage drop on resistors R_{92}, R_{93}. The LLC stage controller uses this network to protect the application when the bulk voltage drops below the adjusted threshold.

The PFC output voltage is regulated according to information provided to the FB pin. Output voltage is divided down by resistor divider R_{18}, R_{27}, R_{35}, R_{47}, R_{56}, R_{57} and connected to the FB pin. Filtering capacitor C_{26} is used because this is a high impedance divider. The bulk voltage compensation network is composed of capacitors C_{36}, C_{40} and resistor R_{75}. This network also performs soft start when the PFC stage is turned on.

The NCP1605 uses negative current sensing to limit the maximum coil current and to detect the core reset. Current flowing through PFC coil L_7 creates a negative voltage on the current sense resistor R_{38}. The PFC controller sources current out of the CS pin in order to maintain a null CS pin voltage. As a result, the CS pin current is directly proportional to the coil current. Resistors R_{44}, R_{45} are inserted to adjust the CS pin current. When the current

flowing through inductor L_7 and switch Q_4 is higher than the maximum current limit level, the CS pin current increases above the OPC threshold (250 uA) and the driver is turned off. The CS input is also used to detect coil demagnetization for zero current detection. The zero current detection prevents the MOSFET from turning on when current flows through the coil. As long as there is no coil current, the NCP1605 operates at a frequency determined by the internal oscillator and external capacitor C_{38}. Zero current detection circuitry sensitivity is adjusted by resistor R_{70} and R_{81}.

To protect the PFC from sudden drops in the line voltage, the controller monitors the rectified line voltage via brownout divider R_{15}, R_{23}, R_{31}, R_{50}, R_{71} and C_{39}.

The driver output is connected to MOSFET Q_4 via resistors R_{25}, R_{26} and diode D_7 to regulate turn−on speed. Transistor Q_7 is used to speed up the MOSFET turn−off time and thus reduce turn−off losses.

Please refer to the application note AND8281/D for detailed information on the PFC stage design and operation.

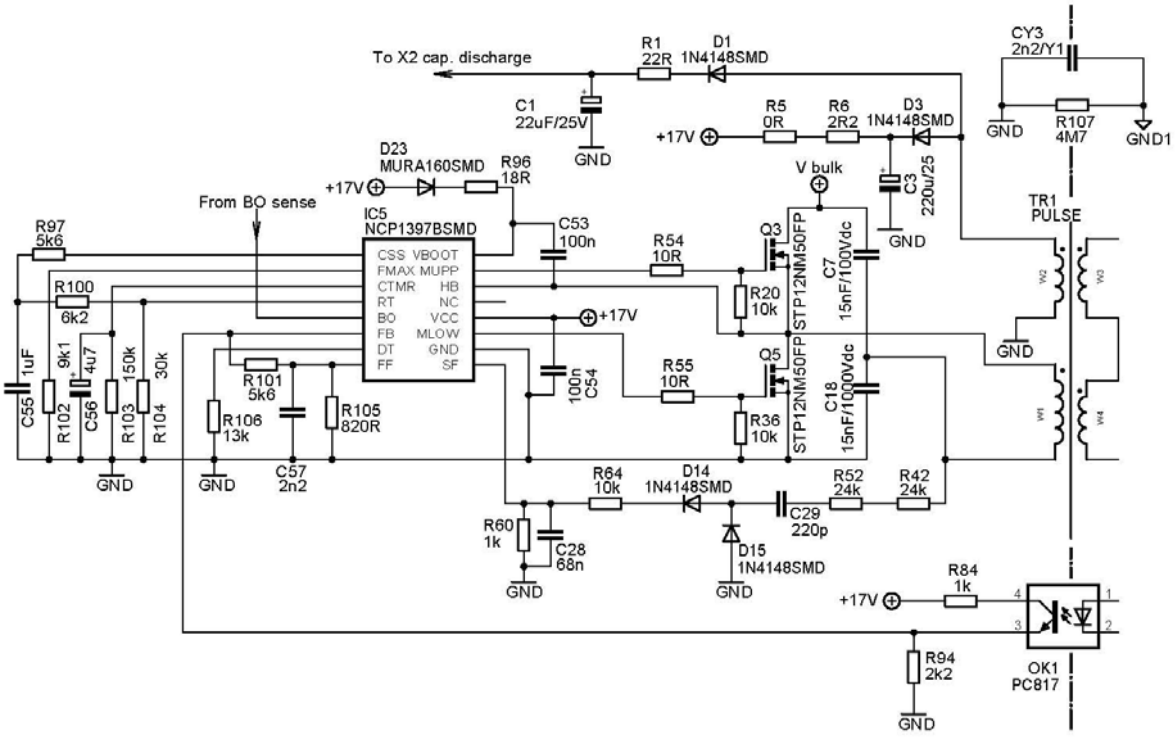

Figure 4. The LLC Stage Primary Side Connection

LLC Power Stage Primary Side

Primary Side Power Loop Connection

The PFC stage prepares a regulated voltage on bulk capacitors C_{16} and C_{17} for the downstream LLC stage (refer to Figure 3). The LLC stage power loop is closed through Q_3 and Q_5, transformer TR_1 and resonant capacitors C_7, C_{18} (Figure 4). The NCP1397 LLC controller features a 600 V high−side driver and is capable of driving the HB power stage directly without the use of a driver transformer. Resistors R_{54} and R_{55} are used to suppress ringing and control EMI noise on the power MOSFET gates. Bootstrap capacitor C_{53} provides the energy required for controlling the high side MOSFET. When Q_5 is turned−on, the HB pin voltage drops and bootstrap capacitor C_{53} is charged through resistor R_{96} and high−voltage diode D_{23}. At turn−on and after any restart, the LLC controller turns on MOSFET Q_5 first to charge up the bootstrap capacitor.

The PFC and LLC controllers are powered from the auxiliary winding W_4 of transformer TR_1. The PFC controller charges up the V_{CC} capacitors C_3, C_{42} first when the demoboard is plugged into the mains. Once the PFC stage starts operation and the bulk voltage is within the nominal operating range, the LLC stage is enabled. The auxiliary winding also provides bias voltage for the X2 capacitor discharge circuitry via diode D_1, resistor R_1 and capacitor C_1. The X2 capacitor discharge circuitry is described in the PFC Stage section (refer to page 3).

FB Loop and Skip Mode:

The minimum operating frequency of the LLC converter is set by resistor R_{104} (refer to Figure 5). The maximum operating frequency is set by resistor R_{102}. The LLC stage

will reach maximum operating frequency during no load conditions.

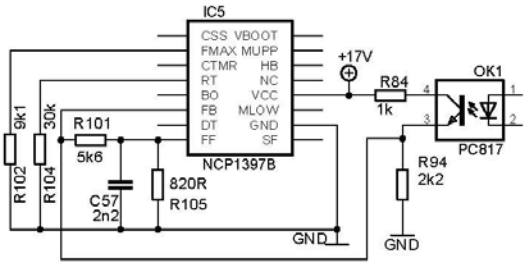

Figure 5. The Primary FB Loop and Skip−Mode Circuitry Connection

Feedback is provided by optocoupler OK_1. The optocoupler current adjusts the FB voltage applied to the LLC controller. The LLC stage operating frequency is thus modulated to assure output voltage regulation. Resistor R_{84} is used to limit the maximum voltage excursion on the FB pin in case the LLC controller goes out of the regulation range (like during skip mode or transient loading).

The skip mode function improves the efficiency of the power supply by omitting switching cycles during light load or no load conditions. The skip mode is implemented using the Skip/Disable pin of the LLC controller. The FB pin voltage increases when the load diminishes. Once the load is too low, the LLC stage is not able to maintain regulation because the operating frequency can not increase further (F_{max} clamp – resistor R_{102}). The FB voltage then goes above the V_{fb_max} limit of 5.3 V. The resistor divider R_{101} and R_{105} provides the FB pin voltage to the Skip/Fault input. The output drivers are thus automatically turned−off and the device begins to skip switching cycles. For efficient skip mode, the FB voltage should overshoot from 50% to 70% (depends on FB loop response time) of its nominal regulation level. The FB voltage divider R_{101} = 5.6 kΩ and R_{105} = 820 Ω was used to allow V_{fb} to swing between 5 – 7.5 V. This setup provides 20 mV pk−pk output voltage ripple during no load conditions.

Overload and Short Circuit Protection, Soft−Start:

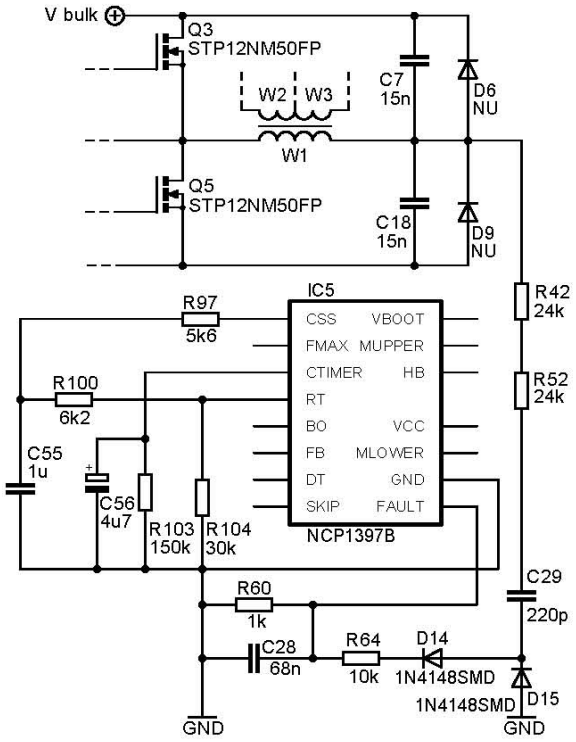

Figure 6. The Output Overload and/or Short Protection Schematic

The Over Current Protection (OCP) is implemented in this design to protect the application from overload conditions. The primary current is sensed indirectly by monitoring the resonant capacitor voltage via the charge pump formed by resistors R_{42}, R_{52}, R_{64}, capacitor C_{29} and diodes D_{14}, D_{15} (refer to Figure 6). The charge pump output is loaded by resistor R_{60} and filtered by capacitor C_{28}. The Soft Start capacitor discharge switch on pin 1 is turned−on once the Fault pin voltage reaches the V_{Ref_fault} threshold (1.04 V). The LLC stage operating frequency is thus automatically increased as the Soft−Start capacitor voltage drops and higher current flows out from the R_t pin. The frequency shift naturally reduces the primary current and protects the primary MOSFETs against damage. Also at this time, the I_{timer1} current source is activated on pin 3 and it begins charging external timing capacitor C_{56}. If the overload condition lasts for longer than the time constant set by I_{timer1} current and timer pin components (C_{56}, R_{103}), the controller enters protection mode and output drivers are disabled. Once the timer capacitor C_{56} is discharged to 1 V, by resistor R_{103}, the application attempts to restart with a Soft Start period. The application can also resume operation with a V_{CC} reset if the LLC controller V_{CC} drops prior to the C_{56} discharging down to 1 V.

The fault timer duration is too long to protect the application against damage due to a short circuit on the

secondary side (output terminals short or secondary transformer winding short). To protect against this possibility, there is a second OCP comparator monitoring the fault pin voltage. When the frequency shift (via Soft Stat pin and resistors R_{97}, R_{100}) is no longer sufficient to keep the primary current limited, the resonant capacitor voltage increases up to such a level that the fault input voltage reaches the V_{ref_OCP} threshold (1.55 V). The application then latches off and protects the power stage components from damage. The circuit remains latched until the V_{CC} is cycled down below V_{CC_reset} and then back above the V_{CC_on} threshold.

The primary current level that will activate the overload protection is given by the maximum secondary current transformed to the primary side and also by the transformer magnetizing current. The RMS value of primary current can be approximately calculated using Equation 1.

$$I_{Primary\_rms} \approx \approx \sqrt{\frac{1}{8}\left(I_{out\_max}^2 \cdot \pi^2 \cdot G_{nom}^{\ 2} + \frac{V_{bulk\_nom}^{\ 2}}{24 \cdot L_m^{\ 2} \cdot f_{op\_ovld}^{\ 2}}\right)} \quad \text{(eq. 1)}$$

Where:

I_{out_max} − is the maximum output current of the LLC stage (23 A)

G_{nom} – is the nominal LLC stage gain (G_{nom} = 0.062 – refer to Page 13)

V_{bulk_nom} − is the nominal bulk voltage

L_m – is the primary magnetizing inductance (715 μH)

f_{op_ovld} − is the operating frequency during overload conditions (78 kHz)

The above equation is an accurate approximation for applications operating at resonant frequency. Accuracy decreases for applications operated far below or above series resonant frequency. The most accurate approach is to measure primary RMS current either from simulation or directly in the application. For the application at hand, the primary RMS current level is 1.68 A when output power is 276 W (i.e. 115% of nominal output power). The primary current flows through the resonant capacitor and creates an ac voltage V_{Cs_ac} that is given by Equation 2.

$$V_{Cs\_ac} = \frac{I_{Primary\_rms}}{2 \cdot \pi \cdot f_{op\_ovld} \cdot C_s} = = \frac{1.68}{2 \cdot 3.14 \cdot 78 \cdot 10^3 \cdot 30 \cdot 10^{-9}} = 114\ \text{Vac} \quad \text{(eq. 2)}$$

Where:

C_s – is the resonant capacitor value i.e. C_7+C_{18}

The DC offset, that is present on the resonant capacitor, is not transferred to the Fault pin as the charge pump cannot handle DC voltages.

A critical failure (like short circuit) can cause the resonant capacitor voltage to swing above the nominal bulk voltage. High peak current can then flow through the charge pump diodes D_{14}, D_{15}. The series resistors R_{42}, R_{52} limit the charge pump diode current to a safe level. The total series resistance can be approximately calculated using Equation 3.

$$R_s = \frac{V_{Cs\_peak}}{I_{f\_limit}} = \frac{1 \cdot 10^3}{20 \cdot 10^{-3}} = 50\ \text{k}\Omega \quad \text{(eq. 3)}$$

Where:

R_s– Is the total series resistance to be used (R_{42}+R_{52})

V_{Cs_peak} − is the peak resonant capacitor voltage

I_{f_limit} − is the maximum forward current of D_{14}, D_{15}

The final application uses a series resistance of $R_s = R_{42} + R_{52}$ = 48 kΩ. The load resistance of 1 kΩ (R_{60}) has been implemented to assure good noise immunity on the Fault input. When the fault input voltage has reached the 1.04 V threshold, the 1st fault comparator is activated. The filtering capacitor C_{28} needs to be low capacitance to assure fast OCP system response. However, this means there will be a ripple present in the fault input voltage. To avoid any issues, the average output voltage of the OCP sensing network has been selected at least 10% below the 1st fault comparator threshold ($V_{OCP\_sense\ out}$ = 0.9 * V_{Ref_fault}). Additional series resistor R_{64} allows fine overload threshold adjustment if needed. The charge pump capacitor value can be calculated using Equation 4.

$$C_{29} = \frac{1}{2 \cdot \pi \cdot f_{op\_ovld} \cdot \sqrt{\left|2 \cdot \left(\frac{V_{Cs\_ac} \cdot R_{60}}{\pi \cdot V_{ref\_faul} \cdot 0.9} - \frac{\left(R_{60}+R_{64}\right)}{2}\right)^2 - \left(R_{42} + R_{52}\right)^2\right|}} = 214.6\ \text{pF} \quad \text{(eq. 4)}$$

Where:

V_{Ref_fault} – is the 1st fault comparator threshold voltage

A charge pump capacitor with standard value (C_{29} = 220 pF) is used in the final application.

As aforementioned, the filtering capacitor C_{28} affects the OCP system response time and precision. The filtering capacitance should be selected in such a way that the time constant R_{60} − C_{28} is at least 5 times higher than the operating period of the converter (Equation 5).

$$C_{28} = \frac{5}{f_{op\_ovid} \cdot R_{60}} = \frac{5}{78 \cdot 10^3 \cdot 1000} \approx 68\ \text{nF} \quad \text{(eq. 5)}$$

The total power loss generated in the series combination of resistors R_{42}, R_{52} needs to be verified (Equation 6).

$$P_{Rs} = \left(\frac{\pi \cdot V_{ref\_fault} \cdot 0.9}{\sqrt{2} \cdot R_{60}}\right)^2 \cdot R_s = 0.208\ \text{W} \quad \text{(eq. 6)}$$

As already mentioned, the first fault comparator threshold is reached when the overload conditions occur. The Soft−Stat capacitor discharge switch is activated and the operating frequency of the converter is automatically increased, limiting the primary current. The series resistor R_{97} = 5.6 kΩ is used on the Soft−Start input to overcome erratic oscillations during transition between normal and overload operating modes. This resistor also decreases the maximum operating frequency during the overload conditions to 150 kHz.

A startup frequency of 200 kHz has been chosen for this design to limit the primary current during the Soft−Start phase. The startup frequency is given by the total current sourced from the R_t pin during startup. When the application starts up both the PFC and LLC controllers reach operating V_{CC} voltage. The LLC controller is disabled via brownout input until the PFC stage output reaches regulation level. The Soft Start capacitor discharge switch is active during this time period as well as the R_t pin reference voltage source. The soft start capacitor thus charges to the voltage that is given by the R_t pin reference voltage (2.3 V) and resistor divider composed of resistors R_{97}, R_{100}. The Soft−Start capacitor initial voltage can be calculated using Equation 7.

$$V_{SS\_start} = 2.3 \cdot \frac{R_{97}}{R_{97} + R_{100}} = \frac{5.6}{5.6 + 6.2} = 1.1\ V \qquad \text{(eq. 7)}$$

The internal resistance of the Soft start switch can be neglected as it's value is small at 100 Ω. When the LLC controller reaches operating V_{CC} prior to the BO_OK signal, the startup frequency can be calculated using the serial and parallel combination of resistors R_{97}, R_{100} and R_{104}. The total R_t pin resistance during Soft−Start is calculated using Equation 8.

$$R_{Rt\_start} = \frac{R_{104} \cdot \left(R_{97} + R_{100}\right)}{R_{104} + R_{97} + R_{100}} \qquad \text{(eq. 8)}$$

For a 200 kHz startup frequency, a R_{Rt_star} value of 8.47 kΩ is required (refer to the NCP1397A/B datasheet − f_{op} vs. $R_{Rt\ chart}$).

The value of resistor R_{100} can be calculated by rearranging Equation 8 to Equation 9.

$$R_{100} = \frac{R_{Rt\_start} \cdot R_{104} + R_{Rt\_start} \cdot R_{97} - R_{97} \cdot R_{104}}{R_{104} - R_{Rt\_start}} = 6.2\ k\Omega \qquad \text{(eq. 9)}$$

The Soft−Start capacitor value is given by the required output voltage ramp−up time. The Soft−Start capacitor, C_{55} = 1 μF, in combination with R_{100} resistor provide output voltage ramp−up time of 18 ms.

During an overload condition, the fault timer is activated to turn−off the application after a programmed time period. This technique prevents the SMPS from thermal damage. If the overload condition disappears before the timer expires, the controller doesn't interrupt operation. The fault timer duration is given by capacitor C_{56}, resistor R_{103} and C_{timer} pin charging current I_{timer1}. The fault timer capacitor charging time can be calculated using Equation 10. The charging period should be selected such that there is enough margin for the Soft−Start period and transient overloading. A fault period of 100 ms has been used in this design.

$$T_{fault} = -R_{103} \cdot C_{56} \cdot \ln\left(1 - \frac{V_{timer(on)}}{R_{103} \cdot I_{timer1}}\right) = \qquad \text{(eq. 10)}$$

$$= -150 \cdot 10^3 \cdot 4.7 \cdot 10^{-6} \cdot \ln\left(1 - \frac{4}{150 \cdot 10^3 \cdot 175 \cdot 10^{-6}}\right) =$$

$$= 117\ ms$$

Where:

$V_{timer(on)}$ − is the fault timer upper threshold

I_{timer1} − is the timer pin charging current

The off−time period of the fault timer is given by Equation 11 when the LLC controller V_{CC} stays at sufficient level (i.e. above V_{CC_off}).

$$T_{off} = R_{103} \cdot C_{56} \cdot \ln\left(\frac{V_{timer(on)}}{V_{timer(off)}}\right) = \qquad \text{(eq. 11)}$$

$$= 150 \cdot 10^3 \cdot 4.7 \cdot 10^{-6} \cdot \ln\left(\frac{4}{1}\right) = 977\ ms$$

Where:

$V_{timer(off)}$ − is the fault timer lower threshold

The recovery time should be selected with respect to the thermal stress of the power stage components. The timer duration is determined by the V_{CC} capacitor discharge time in this design. This is because the primary controller supply voltage naturally drops when the LLC stage is turned−off. In this application, the SMPS recovery time is 1.8 s.

The PCB design features options for over current protection diodes D_6, D_9. Protection diodes, when implemented, limit the maximum resonant capacitor voltage excursion to V_{bulk} level. The primary current is thus naturally limited to a safe level. The use of protection diodes when making changes to the demoboard circuitry is recommended. The OCP diodes can be removed again after the modified system is verified to be working correctly.

LLC Power Stage Secondary Side

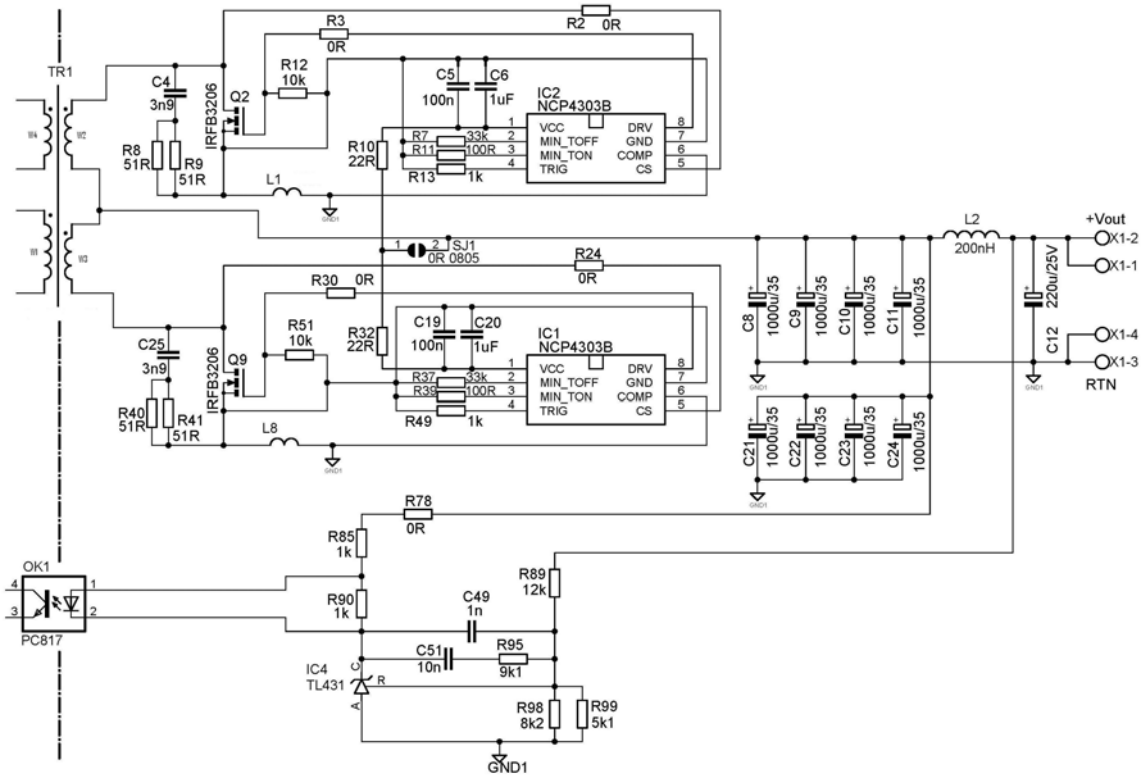

Figure 7. The LLC Secondary Side Schematic

The secondary side uses synchronous rectification with a center tapped transformer configuration in order to provide high efficiency full wave rectification (Figure 7). The SR MOSFETs Q_2, Q_9 are connected in series with secondary windings W_2, W_3, inductors L_1, L_8, filtering capacitor bank C_8−C_{11}, C_{21}−C_{24}. Standard TO−220 package SR MOSFETs have been selected for the application because they reduce manufacturing costs. However, the parasitic inductances of the SR MOSFET package create an error voltage that increases the turn off current threshold. The shift in turn off threshold results in a less than optimal conduction period, reducing the efficiency. In order to avoid this unwanted shift, the NCP4303 features a package parasitic inductance compensation technique. The technique requires the use of a small compensation inductance (L_1, L_8). The secondary current creates a voltage on the compensation inductance and dynamically offsets the ZCD comparator threshold via the COMP input. This method assures maximum conduction time of the SR MOSFET and therefore increases efficiency. The compensation inductor is formed by a square loop of copper wire with diameter of ϕ = 1.2 mm (refer to Figure 66). The compensation inductance value is approximately 4 nH.

SR controllers IC_1, IC_2 are powered from the application output. Resistors R_{10}, R_{32} together with decoupling capacitors C_5, C_6, C_{19} and C_{20} form RC filters to smooth current spikes created during SR driver turn−on. The current sense input monitors the SR MOSFET drain voltage to determine when to turn on and off the SR MOSFET. The NCP4303 driver is connected directly to the SR MOSFET without any external gate resistor in order to minimize turn−off delay. No ringing or EMI issues related to driver current occur assuming a proper layout is used i.e. driver circuitry loop area is minimized.

The power losses related to the SR MOSFET gate driving can be calculated using Equation 12.

$$P_{DRV} = V_{CC} \cdot V_{clamp} \cdot C_{g\_ZVS} \cdot f_{sw\_max} \quad \text{(eq. 12)}$$

Where:

V_{CC} − is the NCP4303 supply voltage (V_{out} in this case)

V_{clamp} − is the driver clamp voltage

C_{g_ZVS} − is the gate to source capacitance of the SR MOSFET in ZVS mode

f_{sw_max} − is the maximum switching frequency of the application

The SR MOSFET conduction losses can be calculated from the secondary RMS current and channel resistance for a given gate voltage (Equation 13).

$$P_{COND} = \left(I_{out} \frac{\cdot \pi}{4}\right)^2 \cdot R_{DS(on)@Vgs\_clamp} \quad \text{(eq. 13)}$$

Where:

I_{out} − is the output current

$R_{DS(on)@Vgs\_clamp}$ – is the SR MOSFET channel resistance for the given driver voltage clamp level

The body diode conduction time and related losses can be significantly reduced due to the NCP4303 compensation capability. If the body diode losses are neglected, the total losses of the SR system can be approximated by summing the driving and conduction losses and then multiplying by the number of SR MOSFETs (Equation 14).

$$P_{SR} = 2 \cdot \left(P_{COND} + P_{DRV}\right) \quad \text{(eq. 14)}$$

The SR MOSFET selection has been made with both cost and efficiency considerations. Another important step is selecting which NCP4303 driver clamp version to use (6 V or 12 V). The choice can be made using the above equations. The theoretical power losses calculated for a SR system using IRFB3206 MOSFETs and two different gate driver clamp voltages can be seen in Figure 8.

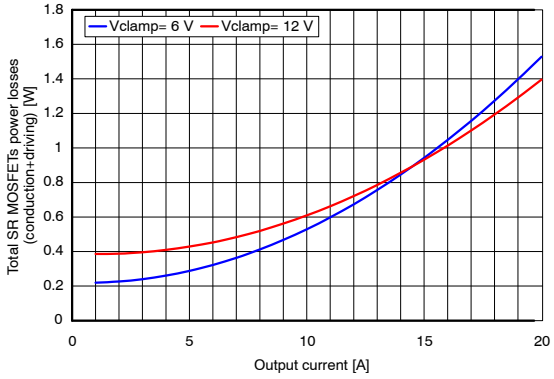

Figure 8. Theoretical Losses of the IRFB3206 SR MOSFET as a Function of Output Current

Figure 8 shows that theoretically calculated losses increase for output current lower than 14 A when 12 V gate driver clamp is used. The maximum efficiency requirement is specified at 50% of full load by the 80 PLUS® program. Therefore the NCP4303B (6 V gate drive clamp) has been selected due to it's improved efficiency at light to medium load.

The power dissipation within the IC package needs to be considered in order to avoid overheating issues. Losses related to the driving of the SR MOSFET gate can be calculated using Equation 15.

$$P_{DRV\_IC} = \frac{1}{2} \cdot C_{g\_ZVS} \cdot V_{clamp}{}^2 \cdot f_{SW} \cdot \left(\frac{R_{drv\_low\_eq}}{R_{drv\_low\_eq} + R_{g\_int}}\right) + C_{g\_ZVS} \cdot V_{clamp} \cdot f_{SW} \cdot \left(V_{CC} - V_{clamp}\right) + \frac{1}{2} \cdot C_{g\_ZVS} \cdot V_{clamp}{}^2 \cdot f_{SW} \cdot \left(\frac{R_{drv\_high\_eq}}{R_{drv\_high\_eq} + R_{g\_int}}\right) = 76 \text{ mW} \quad \text{(eq. 15)}$$

Where:

$R_{drv\_low\_eq}$ – is the SR driver low side switch equivalent resistance (1.55 Ω)

$R_{drv\_high\_eq}$ – is the SR driver high side switch equivalent resistance (7 Ω)

R_{g_int} – is the internal gate resistance of the SR MOSFET

Power losses related to the SR controller internal consumption are given by Equation 16.

$$P_{ICC} = V_{CC} \cdot I_{CC} = 35 \text{ mW} \quad \text{(eq. 16)}$$

Where:

I_{CC} – is the NCP4303 driver supply current for C_{load} = 0 nF and maximum operating frequency (refer to the NCP4303 datasheet for the I_{CC} versus f_{op} chart)

The DIE temperature is given by the thermal resistance from junction to ambient, total power dissipation of the SR controller, and ambient temperature (Equation 17).

$$T_{DIE} = \left(P_{DRV\_IC} + P_{ICC}\right) \cdot R_{\theta JA} + T_A = = (0.076 + 0.035) \cdot 180 + 60 = 80^\circ C \quad \text{(eq. 17)}$$

Where:

$R_{\theta JA}$ – is the IC thermal resistance from junction to ambient

T_A – is the ambient temperature (worst case when the board is fully loaded)

High DIE temperature could appear in applications with high operating frequencies. Additional copper heat sinking in the PCB or a thermal conductor between the SR controller and SMPS package should be used to maintain DIE temperature below the maximum ratings.

The snubber networks R_8, R_9, R_{40}, R_{41}, C_4 and C_{25} dampen the voltage ringing that occurs on the SR MOSFET drain when the secondary winding voltage reverses. The ringing frequency is given by the secondary leakage inductance $L_{sec,leak}$ and output capacitance C_{oss} of the SR MOSFET. The snubber resistance should be equal to the characteristic impedance of the ringing circuitry in order to effectively dampen the oscillations Reference 9, (Equation 18).

$$R_{snubber} = \sqrt{\frac{L_{sec,leak}}{C_{OSS}}} \quad \text{(eq. 18)}$$

Where:

$R_{snubber}$ – is the snubber resistance

$L_{sec,leak}$ – is the secondary leakage inductance

C_{oss}–is the SR MOSFET output capacitance

The snubber capacitance $C_{snubber}$ must be larger than the SR MOSFET output capacitance, but small enough to minimize dissipation in the snubber resistor. The snubber capacitance is generally chosen to be at least 3 to 4 times higher than the value of the parasitic resonant capacitor.

$$C_{snubber} = 3 \rightarrow 4 \cdot C_{OSS} \quad \text{(eq. 19)}$$

The NCP4303 minimum on time and off time generators protect against unwanted switching that could be triggered by ringing on the ZCD comparator. Resistors R_{11}, R_{39} set the minimum on time period. The minimum on time period is selected based on the maximum operating frequency of the LLC stage as well as the secondary current waveform.

During light load conditions, the secondary current oscillation can cause unwanted SR MOSFET switching. A minimum on time of 1.1 μs is needed to prevent this behavior. The required value of min Ton adjust resistors can be calculated using Equation 20.

$$R_{T\_on\_min} = \frac{T_{on\_min} - 4.66 \cdot 10^{-8}}{9.82 \cdot 10^{-11}} = \quad \text{(eq. 20)}$$

$$= \frac{1.1 \cdot 10^{-6} - 4.66 \cdot 10^{-8}}{9.82 \cdot 10^{-11}} \approx 11\ k\Omega$$

Where:

$R_{T\_on\_min}$ –is the minimum on time adjust resistor

The minimum off time period is given by resistors R_7, R_{37}. To prevent issues when the application operates at minimum frequency, the minimum off time should be set to as long as possible. However, the minimum off time value is limited by the maximum operating frequency clamp. In our case, the minimum switching period of the LLC stage is 9.1 μs. Thus the minimum off time period is selected to be 3.9 μs in order to provide a long minimum off time with some margin for the minimum switching period. The minimum off time adjust resistor value can by calculated using Equation 21.

$$R_{T\_off\_min} = \frac{T_{off\_min} - 5.4 \cdot 10^{-8}}{9.56 \cdot 10^{-11}} = \quad \text{(eq. 21)}$$

$$= \frac{3.9 \cdot 10^{-6} - 5.4 \cdot 10^{-8}}{9.56 \cdot 10^{-11}} \approx 39\ k\Omega$$

Where:

$R_{t\_off\_min}$ –is the minimum off time adjust resistor

If the LLC converter uses a very wide operating frequency range, it is beneficial to modulate the minimum off time period. The modulation is possible using a resistor connected from the SR MOSFET drain to the opposite SR controller min Toff pin. When the drain voltage is at a high level, current is injected into the min T_{off} pin. The internal capacitance charging current is thus decreased and the minimum off time period increases. Please refer to the NCP4303 datasheet for more information on how to modulate the minimum off time period.

The NCP4303 features a trigger input that can be used to implement synchronous rectification systems in CCM applications. Additionally, the trigger input can be used to disable the IC and activate a low consumption standby mode. The demoboard layout features optional circuitry (refer to complete schematic – page 31) that allows the customer to implement a primary triggering signal. Normally this is not need in LLC applications as the NCP4303 features a low propagation delay from the CS input to the DRV output. The trigger circuitry option is implemented to allow the customer to test the trigger input functionality.

The no load consumption of the application can be reduced by implementing parallel Schottky diodes across the SR MOSFETs and turning the SR system into sleep mode during light load. The demoboard provides a control input that can be used for this purpose. The external SR standby on/off circuitry can be implemented by monitoring output current.

It is critical to assure correct layout of the SR system to avoid issues with the zero current detection circuitry. Please refer to the NCP4303 datasheet for layout considerations and more information on how the ZCD and the compensation systems work.

The secondary filtering capacitor bank RMS current during full load series resonant frequency operation can be calculated using Equation 22.

$$I_{Cf\_RMS} = I_{out\_nom} \cdot \sqrt{\frac{\pi^2}{8} - 1} = 20 \cdot 0.483 = 9.7\ A \quad \text{(eq. 22)}$$

Where:

I_{out_nom} – is the nominal output current

Filtering capacitors must be used in parallel to handle the total RMS current. Low impedance type capacitors have been used in this design. The total equivalent series resistance (ESR) of the capacitor bank is 2.25 mΩ. The output voltage ripple related to the filtering capacitor bank is composed from two components:

1st the ESR related ripple (Equation 23) and
2nd the ripple related to the capacitor bank capacitance (Equation 24).

$$V_{Cf\_ripple\_pk-pk} = ESR \cdot I_{rect\_peak} = 2.2 \cdot 10^{-3} \cdot \cdot \frac{\pi}{2} \cdot 20 = 69\ mV \quad \text{(eq. 23)}$$

Where:

I_{rect_peak} – is the peak current through the secondary

$$V_{out\_ripple\_cap\_pk-pk} = \frac{I_{out\_nom}}{2 \cdot \sqrt{3} \cdot \pi \cdot f_{op\_nom} \cdot C_f} \cdot \quad \text{(eq. 24)}$$

$$\cdot (\pi - 2) = \frac{20}{2 \cdot \sqrt{3} \cdot 80 \cdot 10^3 \cdot 8 \cdot 10^{-3}} \cdot (\pi - 2) = 10\ mV$$

Where:

f_{op_nom} – is the nominal operating frequency

C_f – is the total capacitance of the capacitor bank

The capacitive component of the output ripple is negligible in this case because of the total filtering capacitance value.

The power losses that are created by the filtering capacitor bank ESR can be calculated using Equation 25.

$$P_{Cf\_ESR} = \left(I_{out\_nom} \cdot \sqrt{\frac{\pi^2}{8} - 1}\right)^2 \cdot ESR = \quad \text{(eq. 25)}$$

$$= \left(20 \cdot \sqrt{\frac{\pi^2}{8} - 1}\right)^2 \cdot 2.25 \cdot 10^{-3} = 0.21\ mW$$

The PCB secondary side layout can significantly affect current distribution among the filtering capacitors. Ideally, the secondary layout should result in an equal distribution of

filtering capacitor connection series parasitic impedances (refer to Figure 9). If mismatched, capacitors with lower series impedance within the bank handle a higher current, which results in decreased life time.

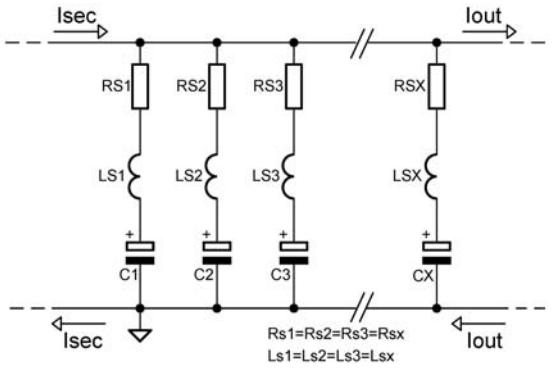

Figure 9. Ideal Configuration of the Capacitor Bank

The capacitor bank provides the bulk of filtering for the secondary currents, but it does not fully filter out narrow glitches produced when the secondary winding reverses. Thus an additional LC filter (L_2, C_{12}) has been implemented. The resonant frequency of this filter should be as low as possible but on the other hand it can affect system loop gain if selected too close to the crossover frequency. A resonant frequency of 24 kHz has been selected for this design. The filter inductor of 200 nH features a low DC resistance, which helps keep efficiency high at medium and full load conditions. A filtering capacitor C_{12} of 220 uF (low impedance type) has been implemented. The filter provides higher peaking around the resonant frequency when a low ESR capacitor is used. On the other hand, if a capacitor with too high of ESR is used, the output voltage drop during fast transient loading increases. The additional LC filter also reduces output voltage ripple at nominal operating frequency and full load conditions by −10 dB.

The output voltage regulation is assured by IC_4. Divider R_{89}, R_{98} and R_{99} provides the regulator IC with output voltage information. Resistor R_{85} limits the maximum current that can pass through optocoupler OK_1. Resistor R_{90} bypasses the optocoupler and provides a bias path for IC_4. The compensation network is composed of resistor R_{95} and capacitors C_{49}, C_{51}. Please refer to application note AND8327/D to learn how to calculate the compensation network. The Bode plot of the full loaded LLC stage is shown in Figure 10.

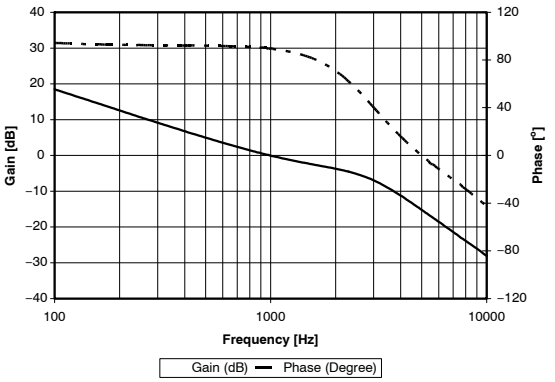

Figure 10. Closed Loop Gain and Phase of the LLC Power Stage for Nominal Output Current

As previously mentioned, the secondary RMS currents are quite high in this application. Parasitic layout resistances can thus affect the LLC stage efficiency. A PCB with 70 μm copper plating has been used for this demo board to minimize power losses related to the secondary side layout.

Resonant tank and transformer design:

An LLC transformer from Pulse engineering has been selected for this design. This transformer offers extra high leakage inductance thanks to a special bobbin arrangement (see demo board photo in Figure 63). The transformer leakage inductance is used as a resonant inductance. This solution eliminates the need for an additional resonant inductor, reducing the overall application cost. On the other hand, a transformer with high leakage inductance causes a stronger proximity effect in the windings, resulting in increased requirements for the winding construction. Another disadvantage of the leaky transformer is high stray flux that negatively impacts the radiated EMI emission. Significant eddy currents can be induced by stray flux in the surrounding metal parts. Therefore it is important to not place these parts too close to the transformer.

The transformer is designed in such a way that the LLC stage is operated in, or very close to, the series resonant frequency (f_s) for full load conditions and nominal bulk voltage. Efficiency is optimized for these operating conditions. The LLC stage operating frequency is increased up to 110 kHz to maintain output voltage regulation when the load diminishes. When the output load drops further down below 1.4 A, the maximum operating frequency clamp is reached and the application enters skip mode operation to reduce the LLC stage power losses. On the other

hand, when the bulk voltage drops, the secondary regulator decreases the LLC stage operating frequency down to 65 kHz to achieve the necessary gain for output voltage regulation.

First harmonic approximation (FHA, refer to References 7 or 11) is a common method for resonant converter analysis. In the actual application, the resonant tank is driven by a square wave voltage. However, FHA modeling does not use a square wave drive. Instead, an equivalent load resistance is used for FHA analysis to compensate for the difference (Equation 26):

$$R_{ac} = \frac{8}{\pi^2} \cdot \frac{V_{out}}{I_{out\_nom} \cdot \eta} = 0.51 \qquad \text{(eq. 26)}$$

Where:
R_{ac} – is the equivalent load resistance for the FHA model
η – is expected efficiency of the LLC stage (94.5%)

The FHA equivalent schematic of an LLC stage with external resonant inductor L_s and standard transformer with magnetizing inductance L_m and negligible leakage inductance can be seen in Figure 11.

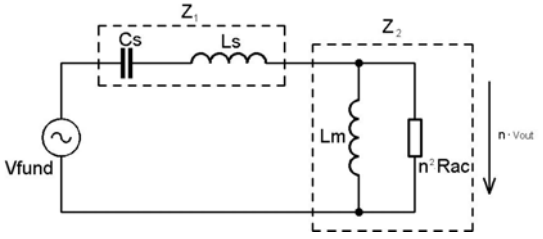

Figure 11. Equivalent Schematic for FHA Analysis

The LLC converter behaves like a frequency dependent divider i.e. the power stage gain can be modified by changing the operating frequency. The LLC stage gain needed for output voltage regulation under full load conditions and selected bulk voltage range (350 Vdc – 425 Vdc) can be calculated based on Equations 27 – 29.

$$G_{min} = \frac{2 \cdot \left(V_{out} + V_{f\_SR}\right)}{V_{bulk\_max}} = \frac{2 \cdot (12 + 0.2)}{425} = 0.057 \qquad \text{(eq. 27)}$$

$$G_{nom} = \frac{2 \cdot \left(V_{out} + V_{f\_SR}\right)}{V_{bulk\_nom}} = \frac{2 \cdot (12 + 0.2)}{395} = 0.0618 \qquad \text{(eq. 28)}$$

$$G_{max} = \frac{2 \cdot \left(V_{out} + V_{f\_SR}\right)}{V_{bulk\_min}} = \frac{2 \cdot (12 + 0.2)}{350} = 0.0697 \qquad \text{(eq. 29)}$$

Where:
V_{f_SR} – is the expected average drop of the SR rectifier including the secondary layout drop
V_{bulk_max} – is the maximum operating bulk voltage
V_{bulk_nom} – is the nominal operating bulk voltage
V_{bulk_min} – is the minimum operating bulk voltage

The resonant tank characteristic impedance (Equation 30) and quality factor (Equation 31) affect the operating frequency range requirement for output voltage regulation.

$$Z_0 = \sqrt{\frac{L_s}{C_s}} \qquad \text{(eq. 30)}$$

Where:
L_s – is the resonant inductor value
C_s – is the resonant capacitor value

$$Q = \frac{n^2 \cdot R_{ac}}{Z_0} \qquad \text{(eq. 31)}$$

The lower the resonant capacitor value, the higher the resonant inductance needs to be in order to assure nominal operating frequency. A higher resonant inductance value generally results in a more narrow operating frequency range throughout the line and load conditions. It is always beneficial to keep a narrow operating frequency range to optimize efficiency and EMI performance

Based on the above considerations, it is evident that the resonant tank with minimized resonant capacitance provides optimum performance. However, the resonant capacitor voltage can reach unacceptable levels if the resonant capacitance value is too low. It is beneficial to limit the resonant capacitor voltage excursion to a level that is below nominal bulk voltage level. There are three main reasons for this consideration:

1st the lower voltage ratings for the resonant capacitor
2nd less voltage stress for the PCB
3rd simple OCP circuitry can be implemented using clamping diodes (D6 and D9 options in demoboard PCB).

The nominal resonant capacitor RMS current can be approximated using Equation 32.

$$I_{Cs\_RMS\_nom} \approx I_{sec\_RMS\_nom} \cdot G_{nom} \approx \approx \frac{\pi}{2 \cdot \sqrt{2}} \cdot I_{out\_nom} \cdot G_{nom} \approx \approx \frac{\pi}{2 \cdot \sqrt{2}} \cdot 20 \cdot 0.062 \approx 1.38 \text{ A} \qquad \text{(eq. 32)}$$

Where:
$I_{out\_nom\_}$ – is the nominal output current

The above calculation does not include magnetizing current because it has only a minor impact. The resonant capacitor capacitance can now be calculated based on the selected capacitor peak voltage (Equation 33).

$$C_s = \frac{I_{Cs\_RMS\_nom} \cdot \sqrt{2}}{2 \cdot \pi \cdot f_{op\_nom} \cdot \left(V_{Cs\_peak\_nom} - \frac{V_{bulk\_nom}}{2}\right)} = \qquad \text{(eq. 33)}$$

$$= \frac{1.38 \cdot \sqrt{2}}{2 \cdot \pi \cdot 80 \cdot 10^3 \cdot \left(320 - \frac{395}{2}\right)} = 31.6 \text{ nF}$$

Where:
$V_{Cs\_peak\_nom}$ – is the resonant capacitor peak voltage under nominal load and bulk voltage conditions

Practically there are two possible choices for implementing the resonant capacitor:

a) one resonant capacitor of 33 nF
b) two resonant capacitors of 15 nF

Variant b) has been selected for this design i.e. two 15 nF capacitors (C_7 and C_{18} in Figure 6). The advantage of this solution is that the primary current divides equally between two capacitors and the bulk capacitor ripple current is reduced by 30%.

The resonant inductance value can be calculated from the selected nominal operating frequency using rearranged Thompson law (Equation 34). A nominal operating frequency of 80 kHz was selected for this application.

$$L_s = \frac{1}{C_s \cdot (2 \cdot \pi \cdot f_s)^2} = \quad \text{(eq. 34)}$$

$$= \frac{1}{30 \cdot 10^{-9} \cdot (2 \cdot \pi \cdot 80 \cdot 10^3)^2} = 131.9\ \mu H \approx 130\ \mu H$$

Where:
f_s – is the series resonant frequency ($f_s = f_{op\_nom}$ in our case)

The magnetizing inductance of the future transformer should be selected with respect to the LLC stage operating frequency range. The operating frequency range is reduced when a high magnetizing inductance value is used. On the other hand, the maximum gain of the LLC stage is reduced and the magnetizing current is not sufficient to overcharge the total bridge capacitance and maintain a ZVS condition when the magnetizing inductance value is too high. The maximum magnetizing inductance value that will still assure ZVS during no load conditions can be calculated based on the selected deadtime period, maximum operating frequency and total bridge capacitance (Equation 35). The bridge capacitance is composed of the primary MOSFETs output capacitances and the primary layout parasitic capacitance.

$$L_{m\_max} = \frac{DT}{8 \cdot f_{op\_max} \cdot C_{HB\_total}} = \quad \text{(eq. 35)}$$

$$= \frac{350 \cdot 10^{-9}}{8 \cdot 110 \cdot 10^3 \cdot 360 \cdot 10^{-12}} = 1.1\ mH$$

Where:
DT –is the selected deadtime period (350 ns for this design)
F_{op_max} –is the maximum operating frequency
C_{HB_total} –is the total bridge parasitic capacitance (2 * C_{oss} + C_{layout})

The primary RMS current increases if too low of magnetizing inductance value is used. Increased RMS current results in higher losses generated in the transformer and primary MOSFETs. The magnetizing to resonant inductance ratio of $k = L_m / L_s = 5.5$ has been chosen for this design as a compromise between losses generation and LLC stage operating frequency range. Magnetizing inductance can be calculated using Equation 36.

$$L_m = k \cdot L_s = 5.5 \cdot 130 \cdot 10^{-6} = 715\ \mu H \quad \text{(eq. 36)}$$

Where:
k – is the ratio between magnetizing and resonant inductance

All of the above calculations have been performed with the expectation that the application will operate at the series resonant frequency for nominal load (20 A) and bulk voltage (395 Vdc). The nominal gain of an LLC converter, that features external resonant inductance L_s, a transformer with negligible leakage inductance ($L_{lk} \rightarrow 0$), and primary inductance $L_{primary} = L_m$, is equal to the inverse of the transformer turns ratio when operated at series resonant frequency (Equation 37).

$$G_{nom} = \frac{1}{n_{discrete}} = \sqrt{\frac{L_{secondary}}{L_{primary}}} = \frac{2 \cdot (V_{out} + V_f)}{V_{bulk\_nom}} = \quad \text{(eq. 37)}$$

$$= \frac{2 \cdot (12 + 0.2)}{395} = 0.0618$$

Where:
$L_{primary}$ – is the primary inductance measured with secondary winding opened
$L_{secondary}$ – is the secondary inductance measured with primary winding opened
$n_{discrete}$ – is the transformer turns ratio for the LLC design with external resonant coil

Required secondary inductance can then be calculated using Equation 38.

$$L_{secondary} = L_{primary} \cdot G_{nom}^{\ 2} = 715 \cdot 10^{-6} \cdot 0.0618^{\ 2} = \quad \text{(eq. 38)}$$

$$= 2.73\ \mu H$$

A simulation model can be built to verify the full load gain characteristic of the proposed LLC design with external resonant inductor (Figure 12). A transformer with high coupling coefficient is expected => coupling → 1.

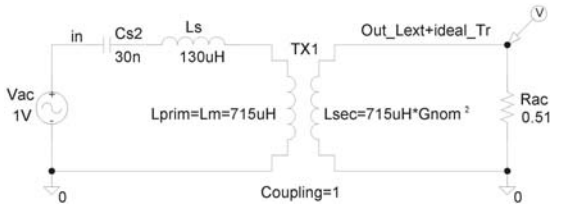

Figure 12. Simulation Model for the LLC Stage with External Resonant Inductance

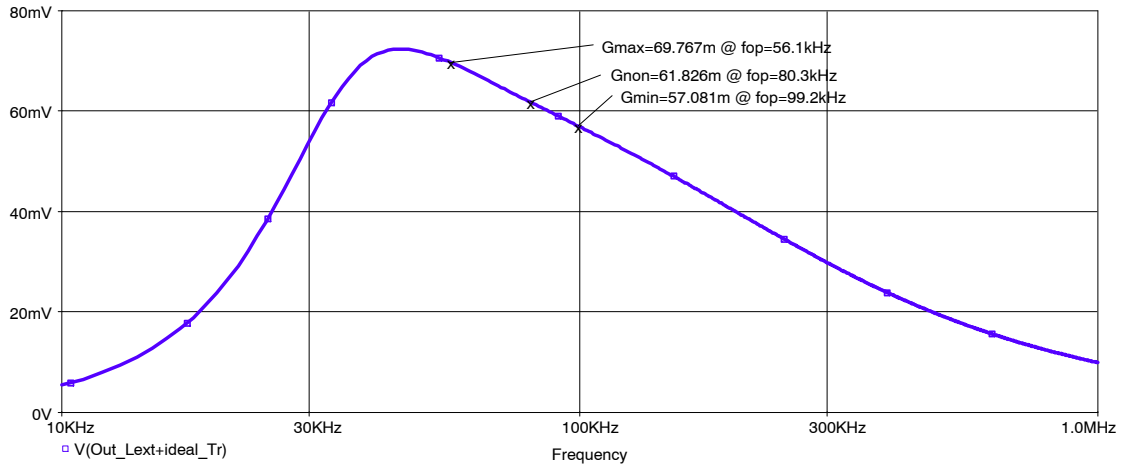

Figure 13. Simulated Gain Characteristic for the LLC Stage Design with External Resonant Inductance, Full Load Conditions

The simulated full load gain characteristic in Figure 13 shows that the proposed design will work in series resonant frequency for full load and nominal bulk voltage conditions.

The difference between the LLC design with external resonant inductance and the design that uses a transformer with high leakage inductance can be determined with simulations. The integrated resonant tank gain differs from the inversed transformer turns ratio when operated in series resonant frequency. This phenomenon is related to the fact that the leakage inductance is physically not located in series with the primary winding like in the external resonant coil solution. The gain of the LLC design with integrated resonant tank, that uses transformer with primary inductance $L_{primay} = L_m$, leakage inductance $L_{lk\_primary} = L_s$ and secondary to primary turns ratio n_{disc}, is thus higher than the inversed turns ratio for the discrete solution when operated at series resonant frequency (Equation 39).

$$G_{nom\_integrated} > \frac{1}{n_{discrete}} \quad \text{(eq. 39)}$$

Figure 14 shows the simulated gain characteristics comparison for both solutions.

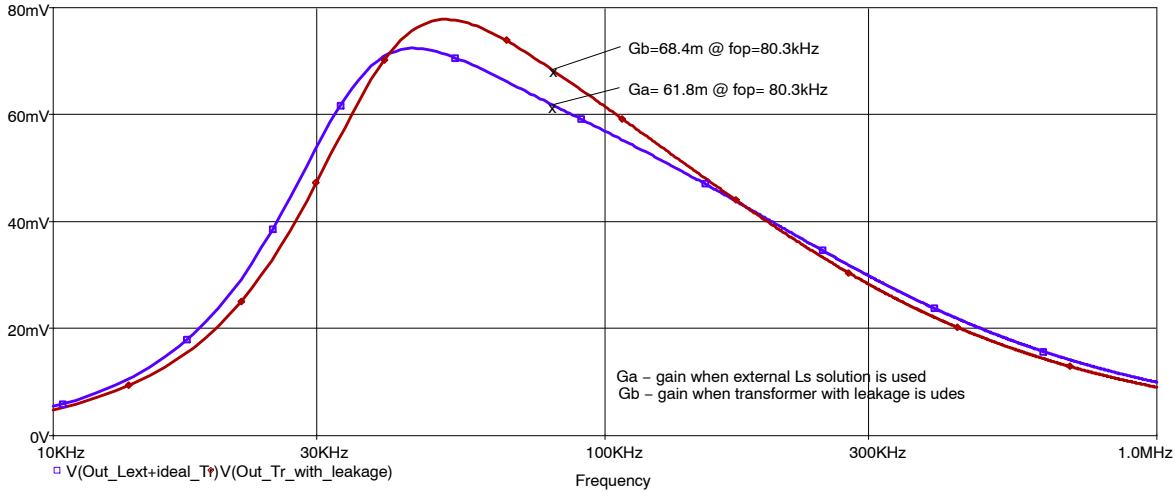

Figure 14. Simulated Gain Characteristics – Comparison Between Resonant Tanks with External Resonant Inductance and with Leakage Resonant Inductance. Both Designs Feature the Same Secondary to Primary Transformer Ratio $n_{discrete}$.

The primary to secondary turns ratio has to be increased by coupling coefficient to assure the same nominal gains at series resonant frequency for both LLC resonant tank solutions. The new turns ratio of the design with integrated leakage inductance is defined by Equation 40.

$$n_{integrated} = \frac{n_{discrete}}{\sqrt{1 - \frac{L_s}{L_m}}} = \frac{16.18}{\sqrt{1 - \frac{130}{715}}} = 17.88 \quad \text{(eq. 40)}$$

Where:
$L_s = L_{lk\_primary}$ – is the primary inductance measured with secondary winding shorted
$L_m = L_{primary}$ – is the primary inductance measured with secondary winding opened

A SPICE model of the modified integrated resonant tank can be seen in Figure 15.

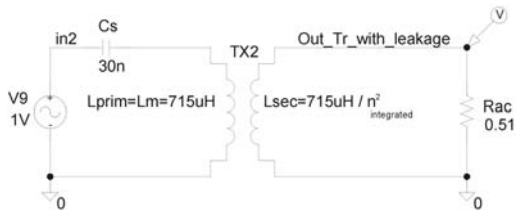

Figure 15. Simulation Model of the LLC Stage with Integrated Resonant Tank and Modified Turns Ratio $n_{integrated}$

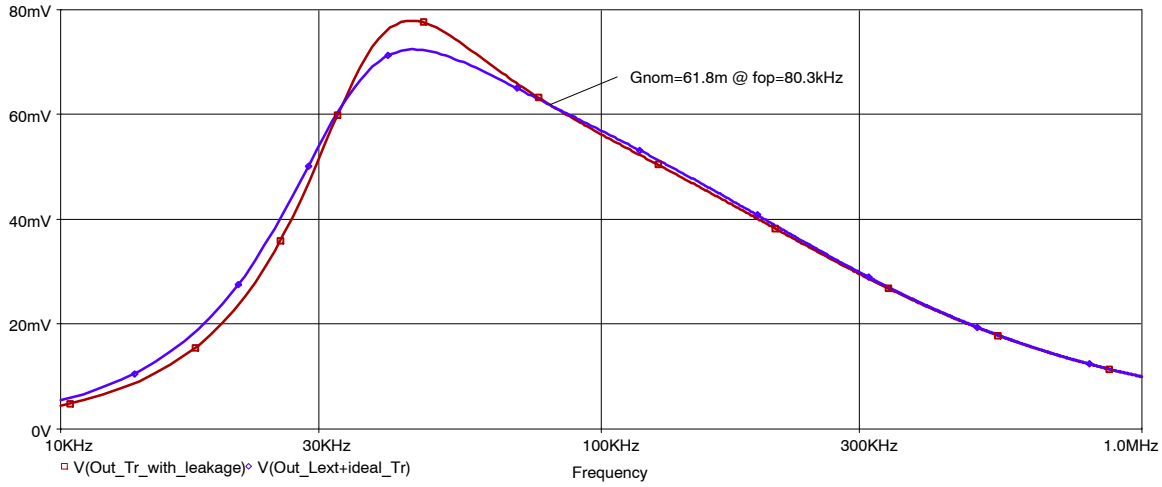

Figure 16. Simulated Characteristics – Comparison Between Resonant Tanks with External Resonant Inductance and with Leakage Resonant Inductance and Modified Turns Ratio.

Simulation results from Figure 16 show that the nominal gains for both solutions are the same when the operating frequency is equal to the resonant frequency. The modified integrated resonant tank solution also provides higher gain below series resonant frequency. This is beneficial as the operating frequency range will be reduced compared to the LLC design with external resonant coil.

The calculated resonant tank components are as follows:
Resonant capacitor: C_s = 2 x 15 nF
Transformer with divided bobbin:
$L_{primary}$ = 715 μH
$L_{secondary} = L_{primary}/n_{integrated}^2$ = 2.23 μH
$L_{lk\_primary}$ = 130 μH when secondary winding is shorted

The transient simulation results for the proposed LLC resonant tank design are shown in Figure 17. Bulk voltage of 395 Vdc and output load of 20 A have been applied during this simulation. The results show that the output voltage is regulated to the target level i.e. 12 Vdc when the application works at a frequency of 80.3 kHz, which meets the target resonant frequency (80 kHz).

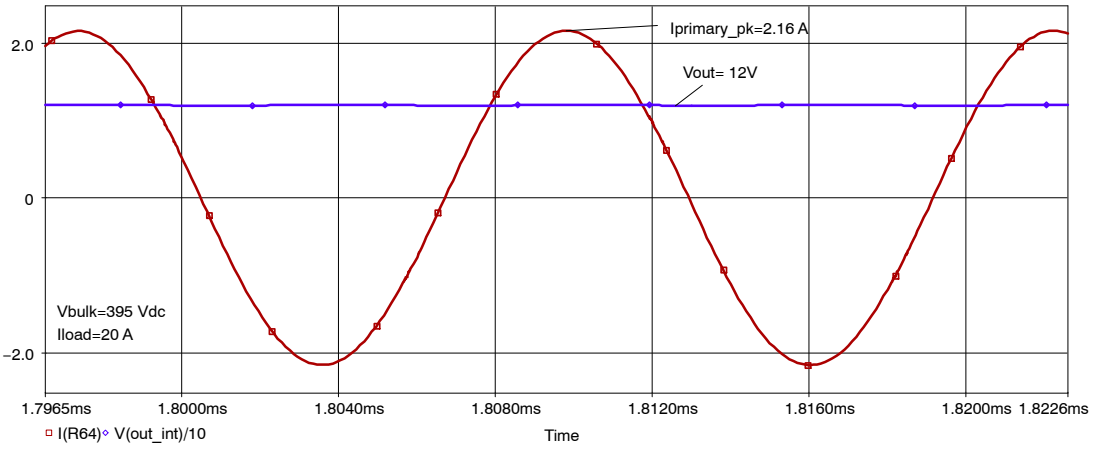

Figure 17. Transient Simulation for Proposed Resonant Tank Design

The number of primary turns needs to be calculated with respect to the transformer flux density excursion. Maximum flux density will be reached for the minimum operating frequency and maximum bulk voltage (Equation 41).

$$N_p = \frac{V_{bulk-max}}{8 \cdot \Delta B_{max} \cdot f_{SWmin} \cdot A_e} = \\ = \frac{420}{8 \cdot 0.125 \cdot 67 \cdot 10^3 \cdot 167 \cdot 10^{-6}} \approx 38 \text{ turns} \quad \text{(eq. 41)}$$

Where:
B_{max} – is the selected peak flux density
F_{sw_min} – is the minimum operating frequency clamp
A_e – is the effective area of the ferrite core center leg cross section

A ferrite core with air gap on the center leg has to be used to allow for primary inductance adjustment. The air gap stores most of the magnetizing energy related to the primary winding. Thus it is beneficial to place the air gap below the primary winding to minimize additional stray flux and reduce the proximity effect.

The air gap position within the bobbin affects primary and secondary inductance values. Generally, the inductance of an inductor with gapped ferrite core is lower when the gap is located below the coil winding rather than outside of the winding. The difference between both cases is due to the magnetic flux bulging out from the gap and coil. When the air gap is not located under the coil winding there will be higher stray flux – refer to Figure 18.

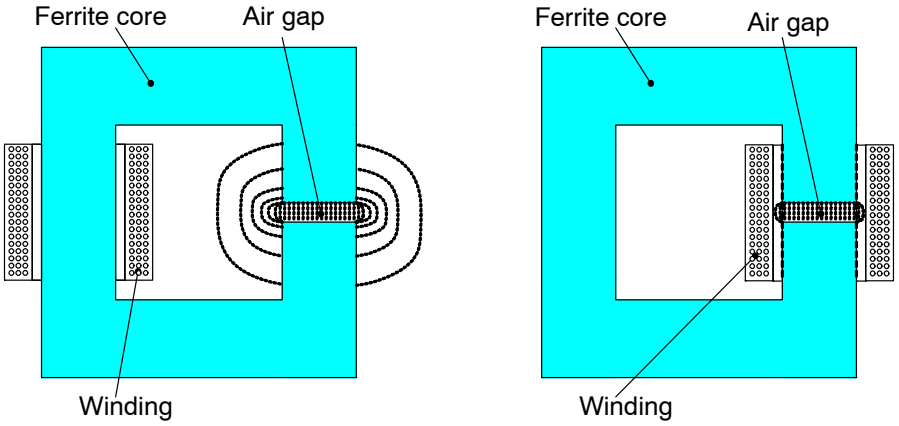

Figure 18. Inductor Inductance and Stray Flux Dependency on the Air Gap Position

A similar situation occurs in the transformer with divided bobbin and air gap located below the primary winding – Figure 19.

There is only one ferrite core but it does not feature the same magnetic conductivity (permanence) for the primary and secondary windings! This is because the air gap is shielded by the primary winding only. The magnetic conductivity of the primary winding $\Lambda_{primary}$ is thus lower than the magnetic conductivity for the secondary winding $\Lambda_{secondary}$ (Equations 42 – 44).

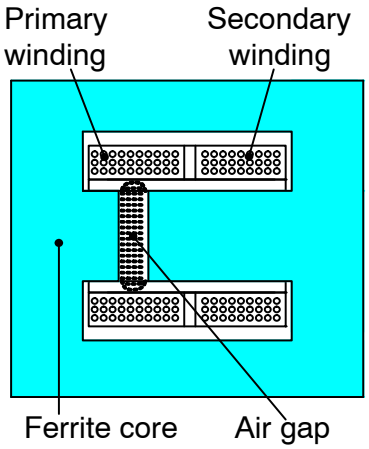

Figure 19. Transformer with Divided Bobbin and Air Gap Below Primary Winding

$$\Lambda_{primary} = \frac{L_{primary}}{N_p{}^2} \quad \text{(eq. 42)}$$

$$\Lambda_{secondary} = \frac{L_{secondary}}{N_s{}^2} \quad \text{(eq. 43)}$$

$$\Lambda_{primary} < \Lambda_{secondary} \quad \text{(eq. 44)}$$

Due to this core non−homogeneity, the physical turns ratio (N) is not equal to the electrical turns (n) ratio that is given by the primary and secondary inductances (Equation 45).

$$\frac{N_p}{N_s} \neq \sqrt{\frac{L_{primary}}{L_{secondary}}} \quad \text{(eq. 45)}$$

Where:
N_p – is the primary winding turns number
N_s – is the secondary winding turns number

The number of the secondary winding turns can be calculated based on the magnetic conductivity for the secondary winding and the required secondary inductance (Equation 46).

$$N_s = \sqrt{\frac{L_{secondary}}{A_{L\_secondary}}} \quad \text{(eq. 46)}$$

The air gap position also affects the total transformer leakage inductance, which needs to be adjusted to the required value.

The primary and secondary magnetic conductivities calculation and the total transformer stray flux calculation are not a simple task for a transformer with divided bobbin. Finite Element numerical Methods (FEM) with a precisely prepared model need to be used. Often the “cut−and−try” method is used during the transformer prototype design.

Finally, the secondary winding composed from two turns (N_s = 2) of copper strip has been used in this LLC transformer design to reach the required secondary inductance.

The auxiliary winding is used to power the SMPS primary controllers during normal and no load operating conditions. The auxiliary voltage of 18 V needs to be used for nominal operating conditions to assure a sufficient V_{CC} level when the board is not loaded. The coupling coefficient between auxiliary and secondary windings has to be as high as possible to assure proper auxiliary voltage regulation. Thus it is beneficial to locate the auxiliary winding directly above the secondary windings. The safety requirements then push for triple insulated wire. The required number of turns for the auxiliary winding can be calculated using Equation 47.

$$N_{aux} = \frac{V_{aux} + V_{f\_daux}}{V_{out} + V_{f\_SR}} \cdot N_s = \frac{18 + 0.7}{12 + 0.2} \cdot 2 = 3 \text{ turns} \quad \text{(eq. 47)}$$

Where:
V_{aux} – is the target auxiliary voltage
V_{f_daux} – is the forward voltage drop of the diode used in the auxiliary V_{CC} path
V_{f_SR} – is the forward voltage drop of the SR system including layout dropouts

The primary winding RMS current can be calculated using Equation 48.

$$I_{primary\_RMS\_nom} = \sqrt{\frac{1}{8} \cdot \left(I_{out\_nom}{}^2 \cdot \pi^2 \cdot G_{nom}{}^2 + \frac{V_{bulk\_nom}{}^2}{24 \cdot L_m{}^2 \cdot f_{op\_nom}{}^2} \right)} = \quad \text{(eq. 48)}$$

$$= \sqrt{\frac{1}{8} \cdot \left(20^2 \cdot \pi^2 \cdot 0.0618^2 + \frac{395^2}{24 \cdot \left(715 \cdot 10^{-6}\right)^2 \cdot \left(80 \cdot 10^3\right)^2} \right)} = 1.46 \text{ A}$$

The secondary winding RMS current for operation in resonant frequency and full load conditions is the same as the secondary rectifier current (Equation 49).

$$I_{sec\_RMS} = I_{out\_nom} \cdot \frac{\pi}{4} = 20 \cdot \frac{\pi}{4} = 15.7 \text{ A} \quad \text{(eq. 49)}$$

The LLC transformer skin effect needs to be considered during windings design for the nominal operating frequency. The skin depth for copper wire can be calculated based on Equation 50.

$$\delta = \frac{65}{\sqrt{f_{op\_nom}}} = \frac{65}{\sqrt{80 \cdot 10^3}} = 0.23 \text{ mm} \quad \text{(eq. 50)}$$

The maximum winding wire diameter that will be effectively used by the AC current is then two times higher than the calculated skin depth i.e. $\phi = 0.46$ mm. It makes no sense to use wires with higher diameter in primary or secondary windings because current cannot penetrate deeper into the conductor than to the calculated skin depth.

As aforementioned, the proximity effect caused by the primary and secondary windings positioning is another limitation in transformers with divided bobbin construction. The winding turns located closer to the opposite winding on the bobbin are affected by the field of other turns from the winding and have the strongest proximity effect. Proximity effect analysis is out of scope of this application note – one can refer to Reference 12 for more information on this subject.

After considering the skin effect and proximity effect it is evident that the best solution to winding construction is to use litz wire composed of several insulated conductors with diameter smaller than 0.46 mm. The secondary winding conducts a high RMS current compared to the primary, so it is beneficial to use copper strip lines instead of multiple litz wires. The primary winding has been implemented with litz wire 22xØ0.16. The secondary windings are composed of copper strip lines 8 mm wide and 0.2 mm thick. The auxiliary winding is composed of three turns of triple insulated wire with a diameter of Ø = 0.25 mm. This winding is located directly above the secondary windings to assure good coupling as mentioned above.

Some manufacturers specify the leakage inductance under the condition of all secondary windings shorted. This approach cannot be applied for a center tapped secondary side design because only one winding from the pair contributes resonance each switching period half cycle. Figure 20 with Table 2 shows how to measure the leakage inductances of a transformer with center tapped secondary side.

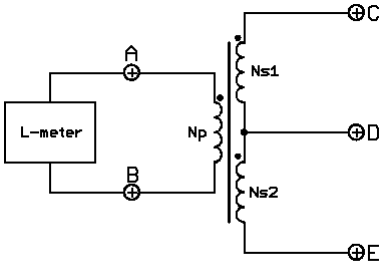

Figure 20. Transformer Primary Leakage Inductance Measurements

Table 2. WINDINGS CONFIGURATIONS DURING MEASUREMENTS OF LEAKAGE INDUCTANCE

Parameter	Measured Between Pins	Secondary Pins Configuration
$L_{lk(p-s1)}$	A–B	C–D short D–E open
$L_{lk(p-s2)}$	A–B	C–D open D–E short
$L_{lk(total)}$	A–B	C–D short D–E short
$L_{primary}$	A–B	C–D open D–E open

It is necessary to assure good matching between $L_{lk(p-s1)}$ and $L_{lk(p-s2)}$ leakage inductances otherwise the series resonant frequency would differ in each switching half cycle. As a result, the secondary current through each secondary branch would differ. The secondary current difference would increase losses and temperature in one of the secondary branches.

Figure 21 shows the simulated results for a case where the secondary currents leakage inductances imbalance is 5%.

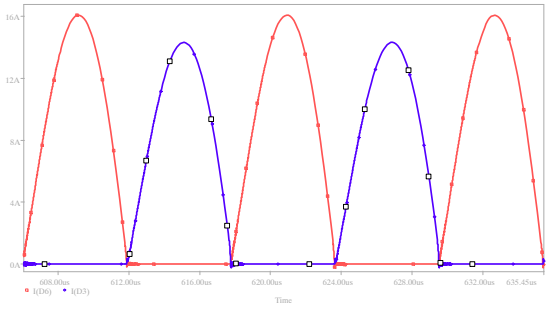

Figure 21. Simulated Secondary Currents for Application with Primary Leakage Inductances Imbalance of 5%

Other possible sources of imbalance in the LLC power stage are the secondary layout parasitic inductances. The transformer turns ratio between primary and secondary is quite high for a 12 V output application. When reflected to the resonant tank circuitry, the secondary parasitic inductances are multiplied by the transformer turns ratio squared. This means that even very small secondary layout parasitic inductance asymmetry (like 50 nH) causes a big difference in resonant frequencies for each switching half period. The secondary layout thus needs to be as symmetrical as possible to achieve balanced LLC stage operation.

The final transformer specification is summarized in below figures and tables.

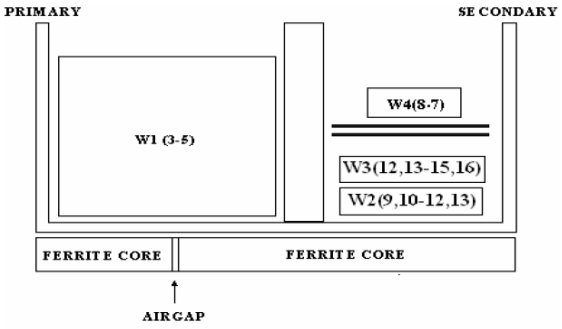

Figure 22. The Transformer Windings Arrangement Within the Bobbin

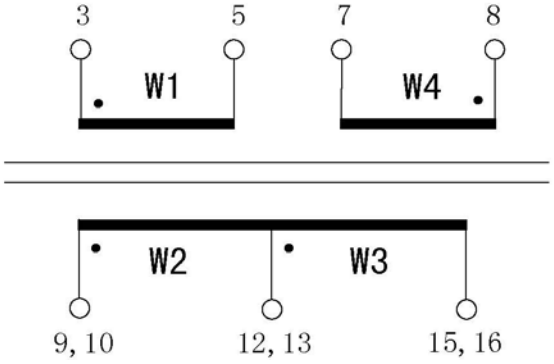

Figure 23. Transformer Windings Pinout

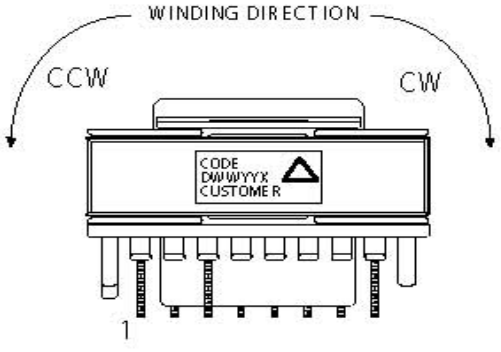

Figure 24. Transformer Winding Directions

Table 3. TRANSFORMER PRIMARY INDUCTANCE SPECIFICATION

Primary Inductance			L_p (μH)	Tolerance	R (mΩ)	Tolerance
Between Pins	3	5	715	±10%	101	±15%

Table 4. TRANSFORMER LEAKAGE INDUCTANCES SPECIFICATION

Primary Inductance			L_{LK} (μH)	Tolerance	Shorted Pins
Between Pins	3	5	130.5	±7%	9–10–12–13
Between Pins	3	5	131.8		12–13–15–16
Between Pins	3	5	126.8		9–10–12–13–15–16

Table 5. TRANSFORMER WINDINGS SPECIFICATION

Winding #	Pin #		Turns and Gauge		Layers (Turns)	Winding Method	Insulation Tape	
	Start	Finish	Turns	Wire Gauge			Turns	Thickness Width
W1	3	5	38	UEW+NY LIT Z 0.16∅x22# Grade 2 (NEMA MW80C/IEC 317−21) Thermal Class 155°C	5 (9 + 9 + 9 + 9 + 2)	CW Closed		
W2	9, 10	12, 13	2	Cu Foil W = 8 mm T = 0.2 mm	2	CCW	2	2 mils 9 mm
W3	12, 13	15, 16	2	Cu Foil W = 8 mm T = 0.2 mm				
W4	8	7	3	TIW 0.25∅ Thermal Class B	1	CW Closed		

PCB Design

The PCB layout of the LLC stage primary side is not very critical because switching of the main MOSFETs happens only under ZVS conditions and the influence of the PCB parasitic inductances on the operating frequency is negligible. The LLC stage secondary side layout is very critical especially in applications with low output voltages.

It is recommended that both paths from the secondary windings to the filtering capacitor bank should be made with the same length. A difference in parasitic inductance between paths results in a different resonant frequency for each half of the switching period. As the secondary RMS current is high, the parasitic resistance of the secondary layout should be minimized. This SMPS is designed on a two layer PCB with 70 μm copper plating.

Results

Please follow the steps detailed in the test procedure for the NCP4303 demo/evaluation board if testing the demoboard performance. Below measurements are shown for further information on how this design operates in practice.

Thanks

I would like to thank the below companies for providing the samples used in this demoboard.

Epcos – http://www.epcos.com
Koshin – http://www.koshin.com.hk
Pulse – http://www.pulseeng.com
Wurth – http://www.we−online.com
Coilcraft – http://www.coilcraft.com

Conclusion

This demoboard shows only one of many possible implementations of the NCP4303A/B synchronous rectification controller and is not intended as a final design for end customers. The main goal of this document is to introduce a typical application and illustrate how the various features help to decrease total cost and increase SMPS efficiency. Optional features are included in the PCB layout, thus it is easy to update the application according to specific requests.

References:

1. NCP4303 data sheet
2. NCP1605 data sheet
3. NCP1397 data sheet
4. Application note AND8257/D
5. Application note AND8327/D
6. Application note AND8281/D
7. Bo Yang – Topology Investigation for Front−End DC−DC Power Conversion for Distributed Power System
8. M. B. Borage, S. R. Tiwari and S. Kotaiah – Design Optimization for an LCL – Type Series Resonant Converter
9. Dr. Ray Ridley – http://www.ridleyengineering.com/snubber.htm
10. ON Semiconductor documentation TND399/D – 216 W All in One SMPS Reference Design
11. M. Jovanovic, “Principle of Resonant Power Conversion”, in−house seminar, Toulouse 2004.
12. Xi Nan, C. R. Sullivan – An Improved Calculation of Proximity−Effect Loss in High−Frequency Windings of Round Conductor

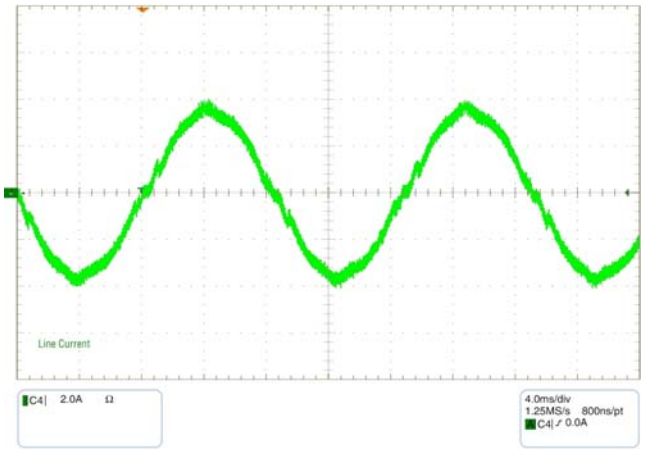

Figure 25. Application Input Current Measured for 110 V_{AC} / 60 Hz Input and Full Load Conditions

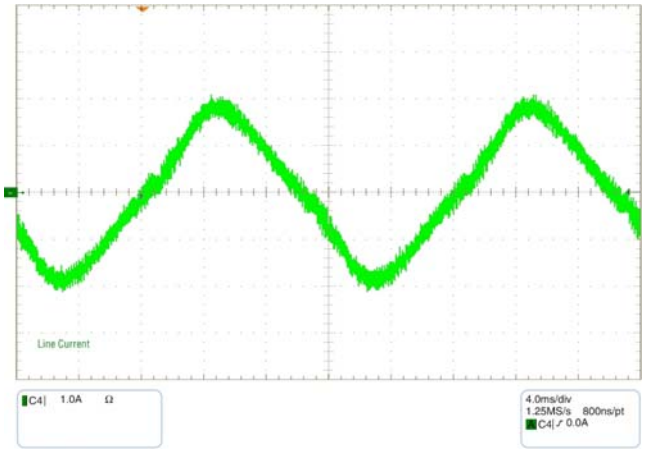

Figure 26. Application Input Current Measured for 230 V_{AC} /50 Hz Input and Full Load Conditions

Figure 27. LLC Primary Current and Bridge Voltage for I_{load} = 20 A

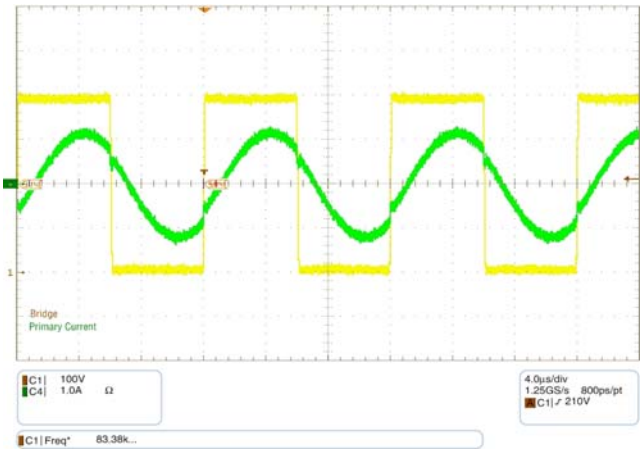

Figure 28. LLC Primary Current and Bridge Voltage for I_{load} = 10 A

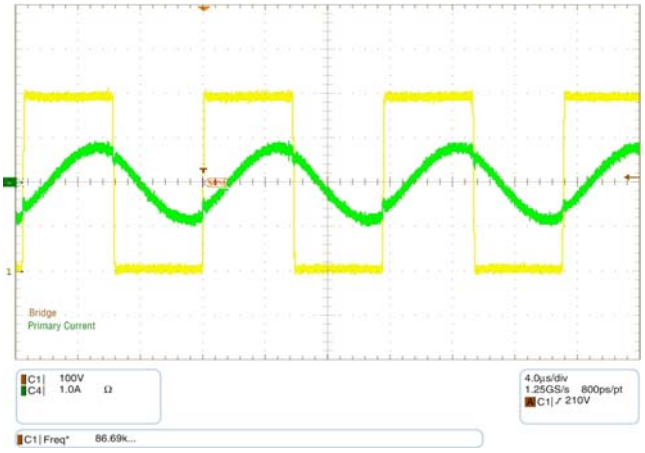

Figure 29. LLC Primary Current and Bridge Voltage for I_{load} = 5 A

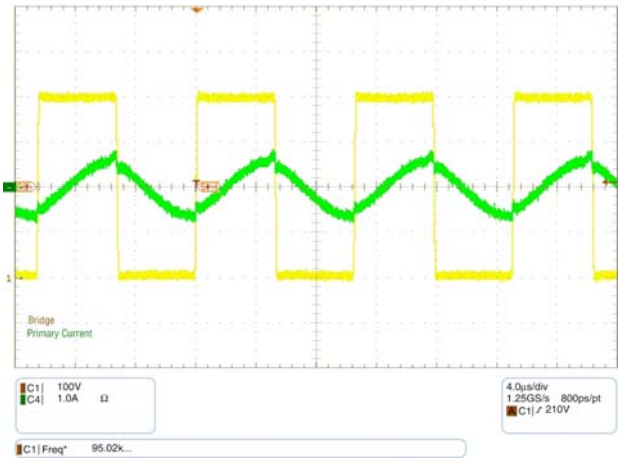

Figure 30. LLC Primary Current and Bridge Voltage for I_{load} = 2.5 A

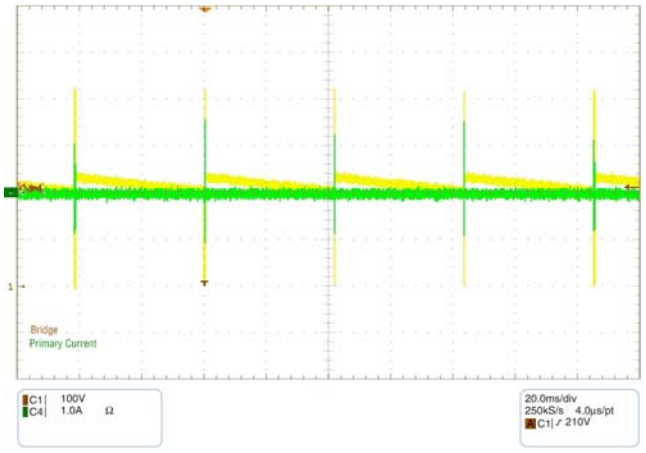

Figure 31. LLC Primary Current and Bridge Voltage for I_{load} = 0 A, SR is Operating

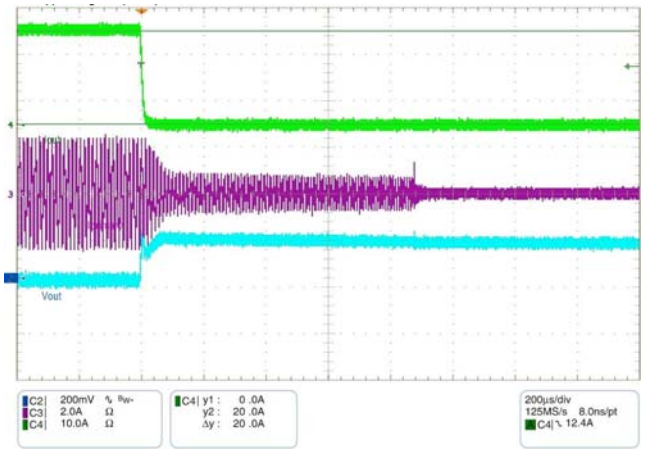

Figure 34. SMPS Response to Transient Loading 20 A to 0 A, 1.6 A/µs

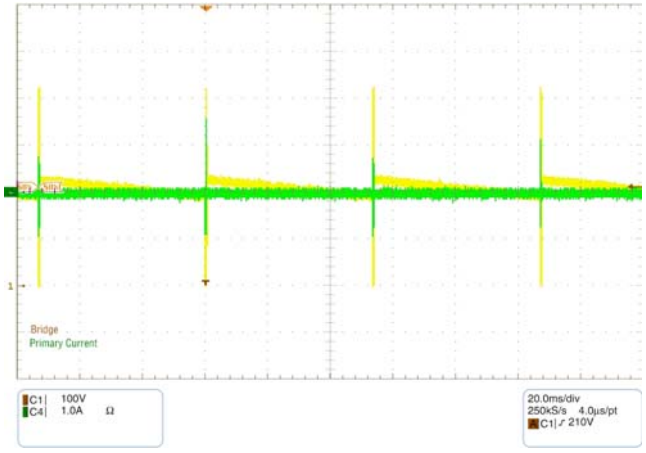

Figure 32. LLC Primary Current and Bridge Voltage for I_{load} = 0 A, SR is Not Operating

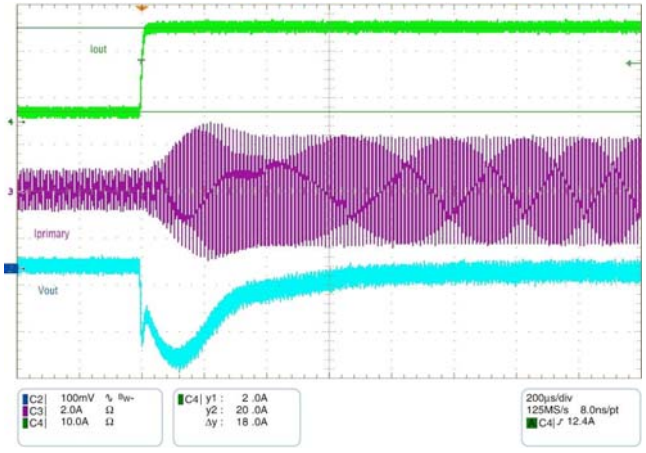

Figure 35. SMPS response to Transient Loading 2 A to 20 A, 1.6 A/µs

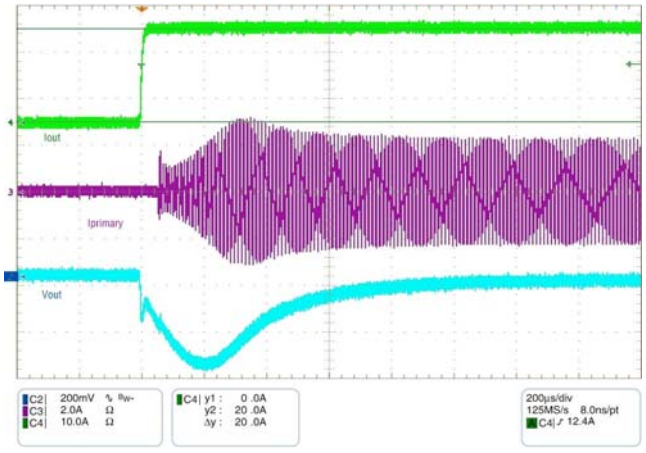

Figure 33. SMPS Response to Transient Loading 0 A to 20 A, 1.6 A/µs

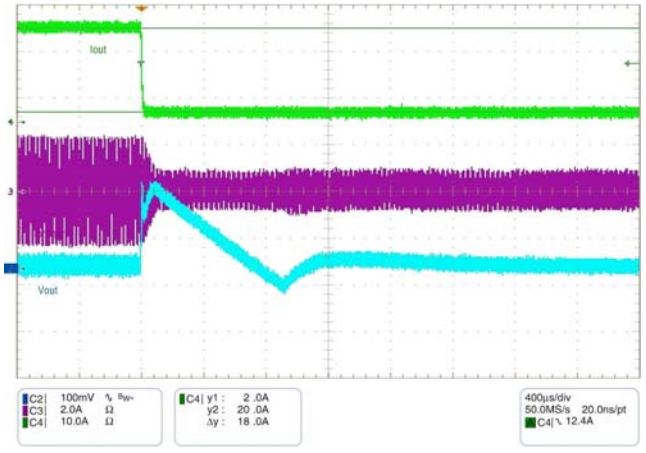

Figure 36. SMPS Response to Transient Loading 20 A to 2 A, 1.6 A/µs

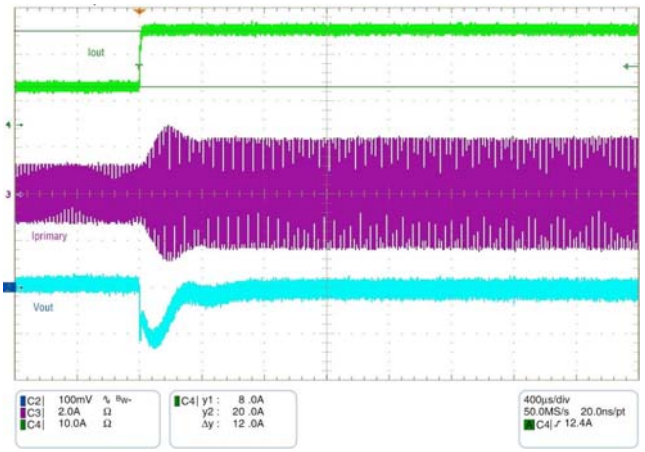

Figure 37. SMPS Response to Transient Loading 8 A to 20 A, 1.6 A/μs

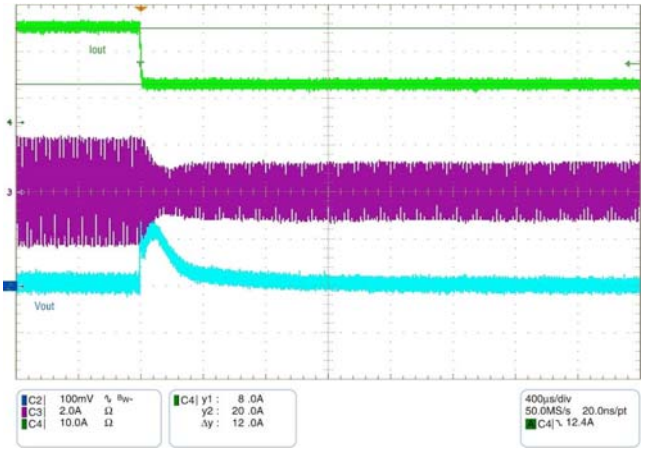

Figure 38. SMPS Response to Transient Loading 20 A to 8 A, 1.6 A/μs

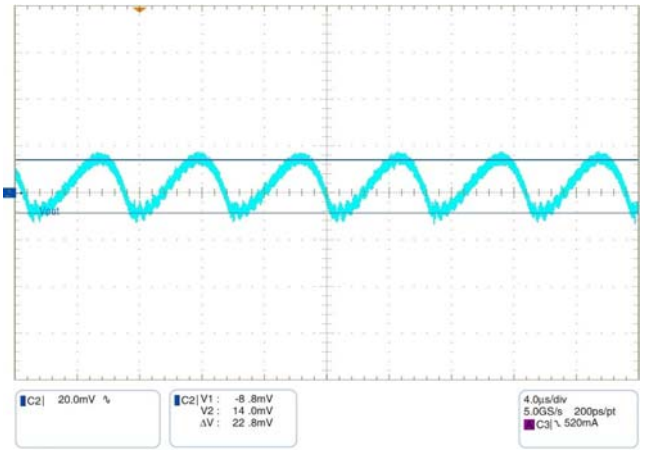

Figure 39. Output Voltage Ripple Under Full Load Conditions

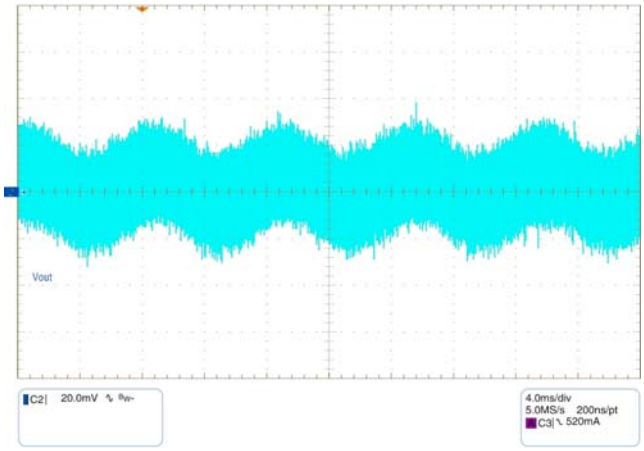

Figure 40. Bulk Voltage Ripple Image in the Output Voltage Under Full Load Conditions, 110 Vac/60 Hz

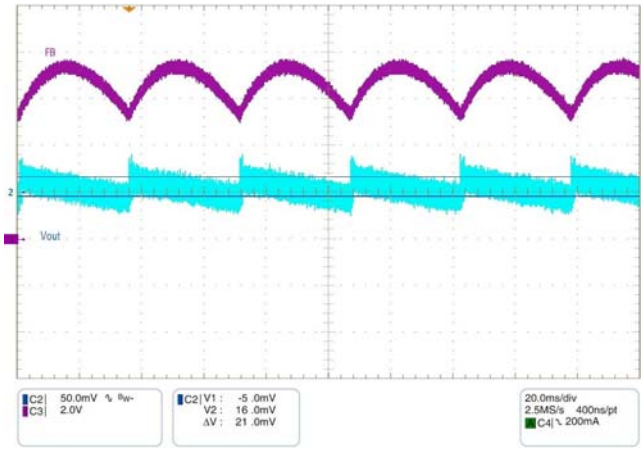

Figure 41. Output Voltage Ripple During No Load Conditions – SR is Turned Off

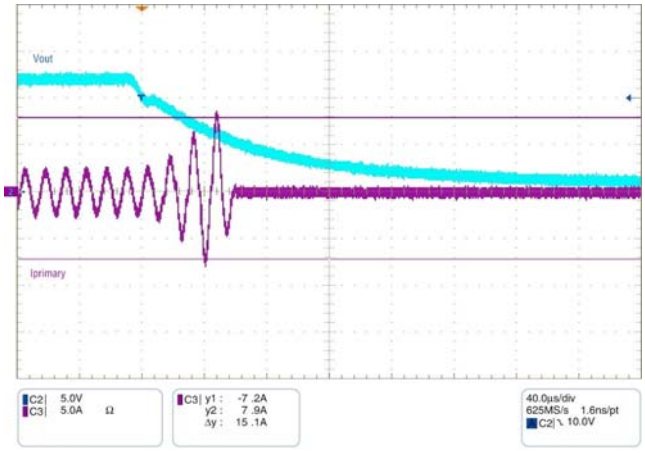

Figure 42. Transition From Full Load to Output Short−Circuit

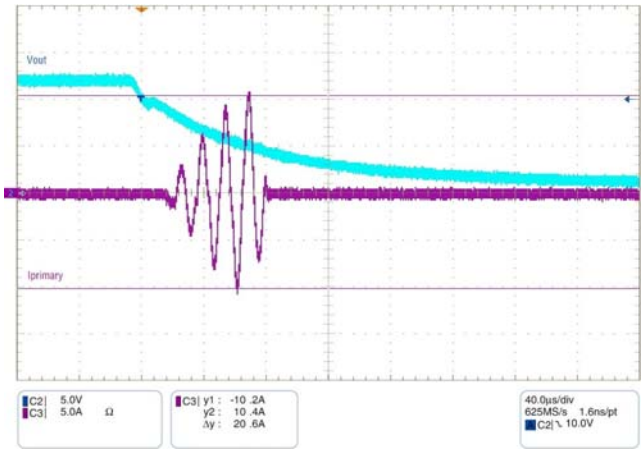

Figure 43. Transition From No Load Operation to Output Short−Circuit

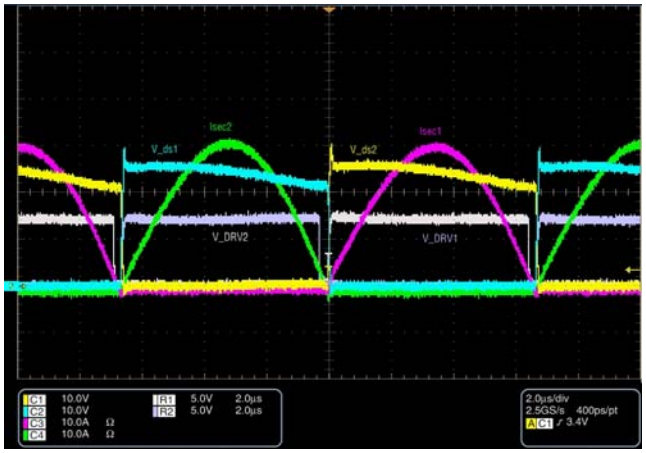

Figure 46. Secondary Side Currents, SR Gate and V_{ds} signals for I_{out} = 20 A, IRFB3206

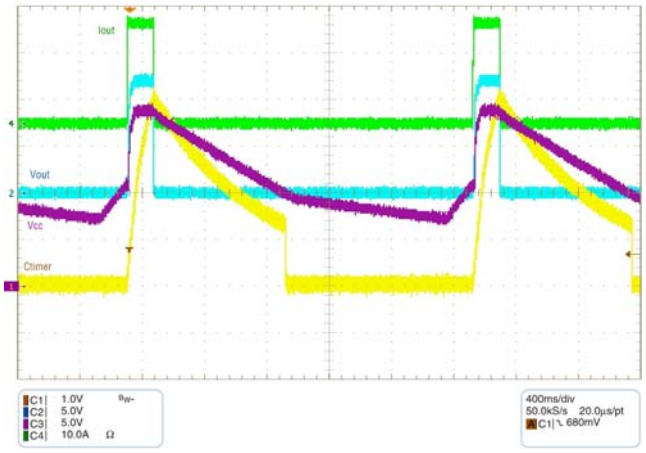

Figure 44. SMPS Operation Under Overload Conditions, Restart Time Given by V_{CC} Restart

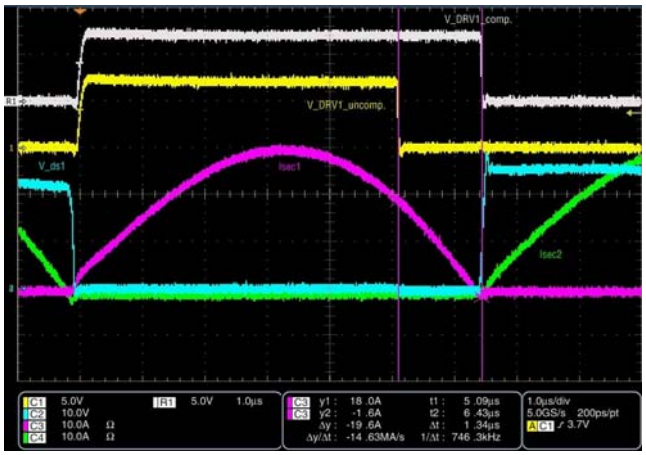

Figure 47. Secondary SR Gate Signals Comparison for Compensated and Uncompensated SR System I_{out} = 20 A, IRFB3206

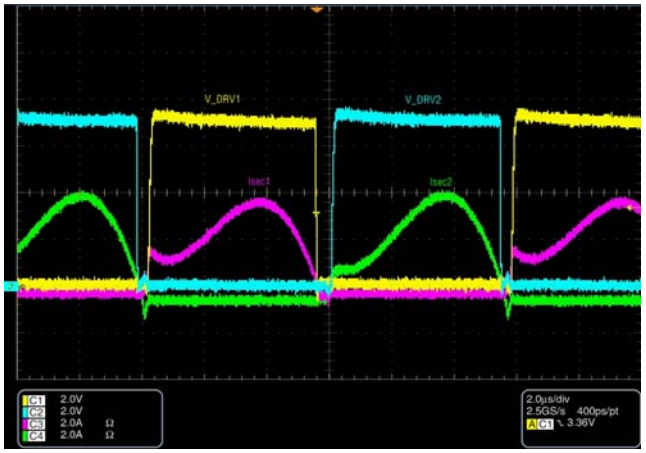

Figure 45. Secondary Side Currents and SR Gate Drive Signals for I_{out} = 2.5 A, IRFB3206

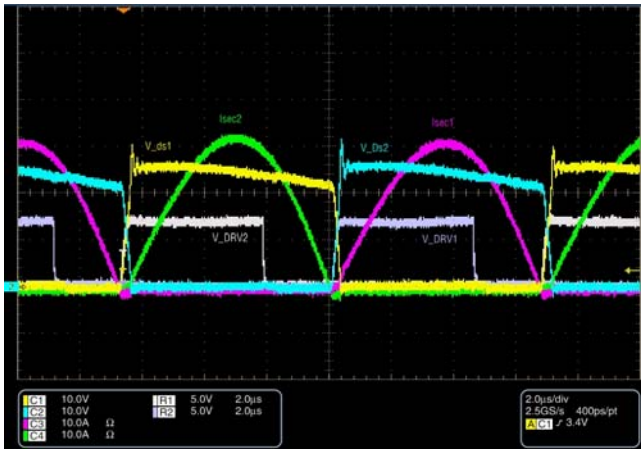

Figure 48. Secondary Side Currents, SR Gate and V_{ds} Signals for I_{out} = 20 A, IPP015N04N – Uncompensated

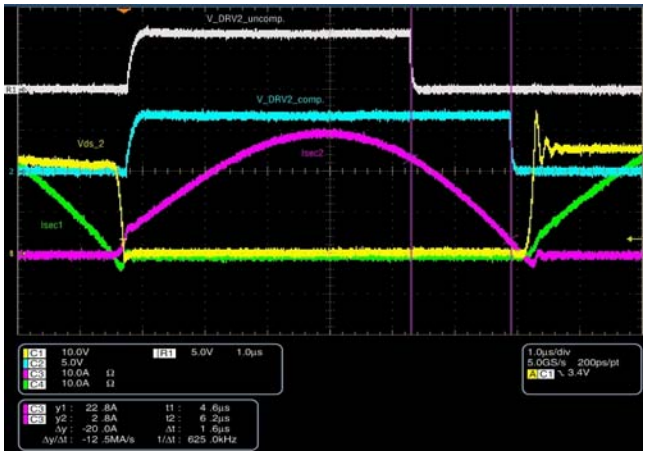

Figure 49. Secondary Side Currents, SR Gate and V_{ds} Signals for I_{out} = 20 A, IPP015N04N – Compensated

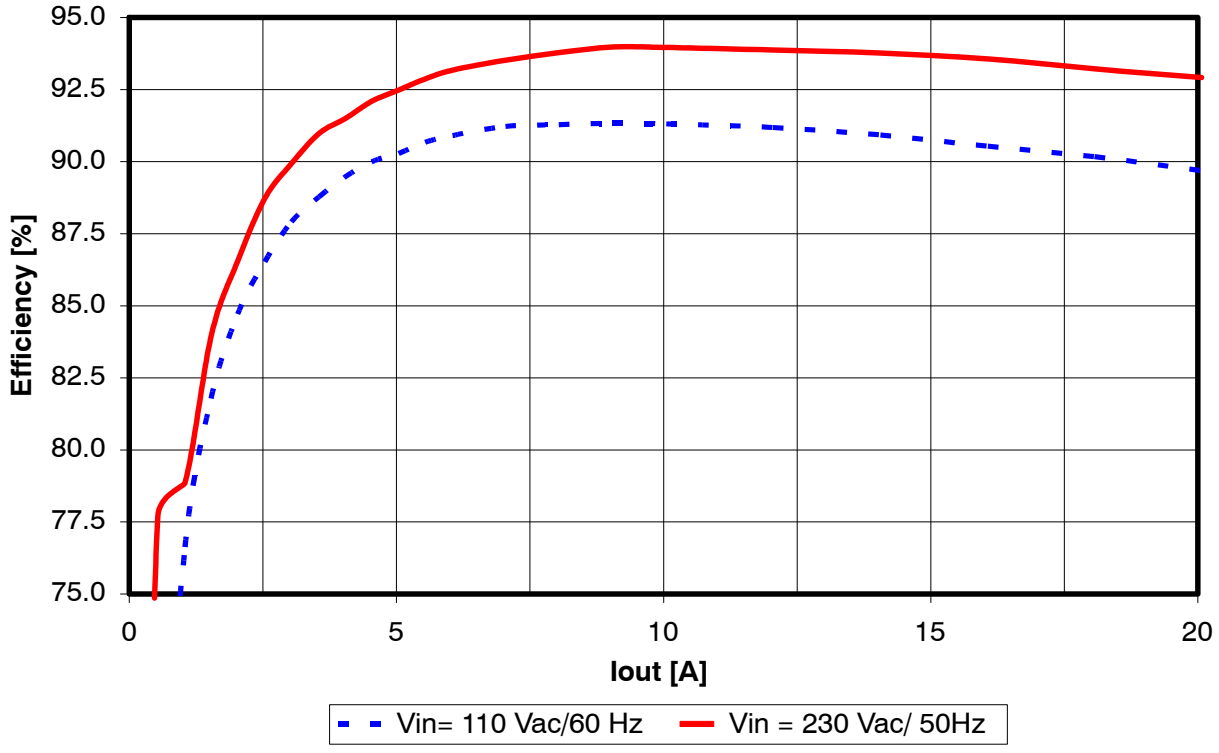

Figure 50. Demoboard Efficiency versus Output Current for Compensated SR System and IRFB3206 SR MOSFETs

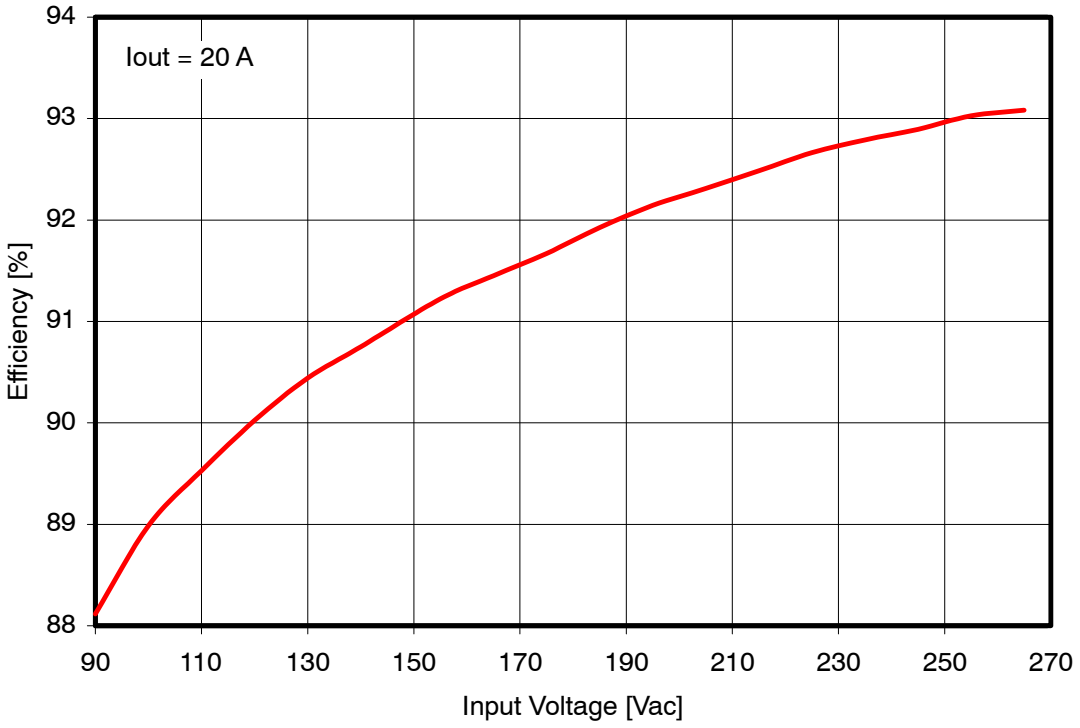

Figure 51. Demoboard Full Load Efficiency versus Input Voltage for Compensated SR System and IRFB3206 SR MOSFETs

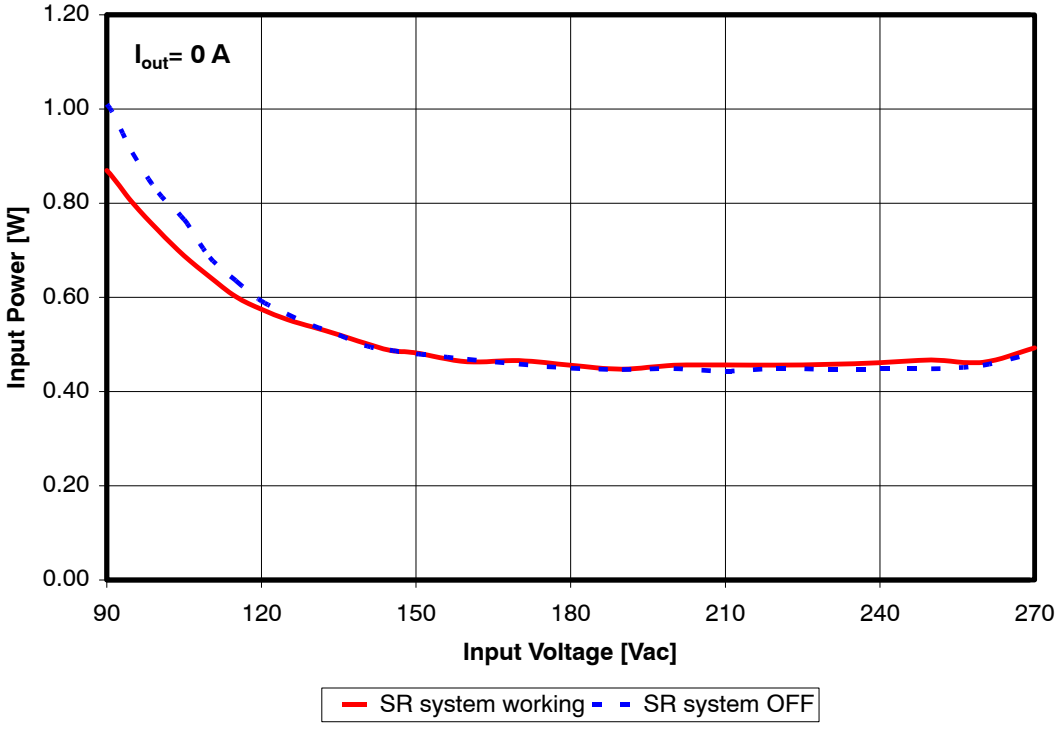

Figure 52. Demoboard No Load Consumption for SR System Working and Turned Off

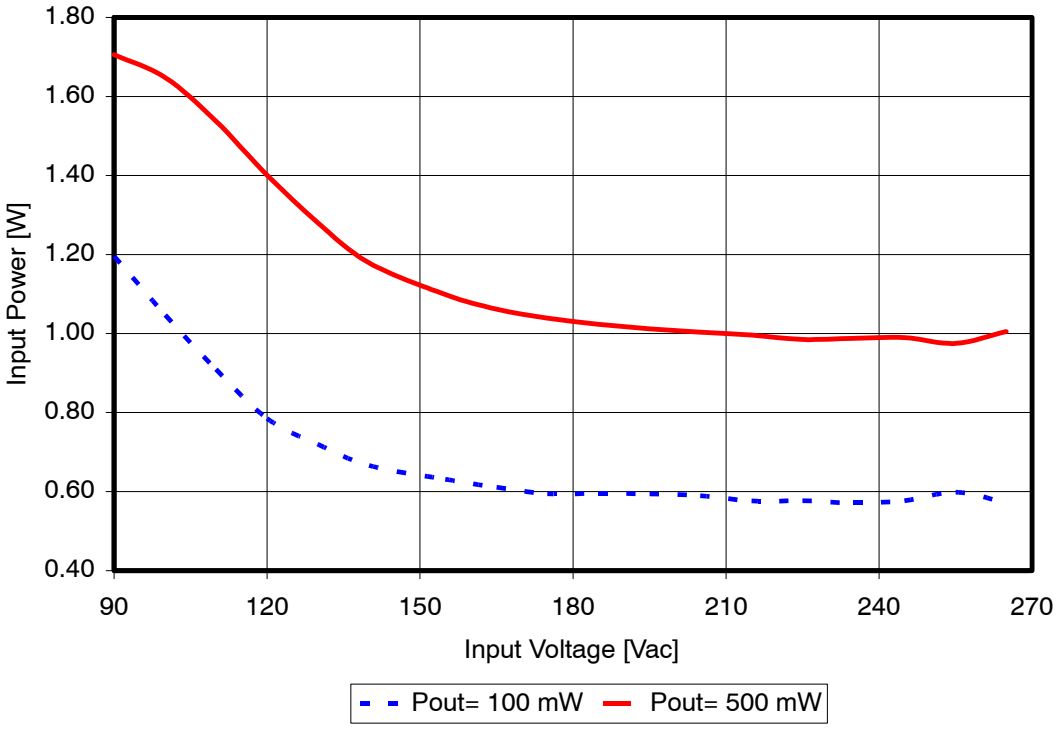

Figure 53. Demoboard Consumption for 100 mW and 500 mW Loads (SR System Working)

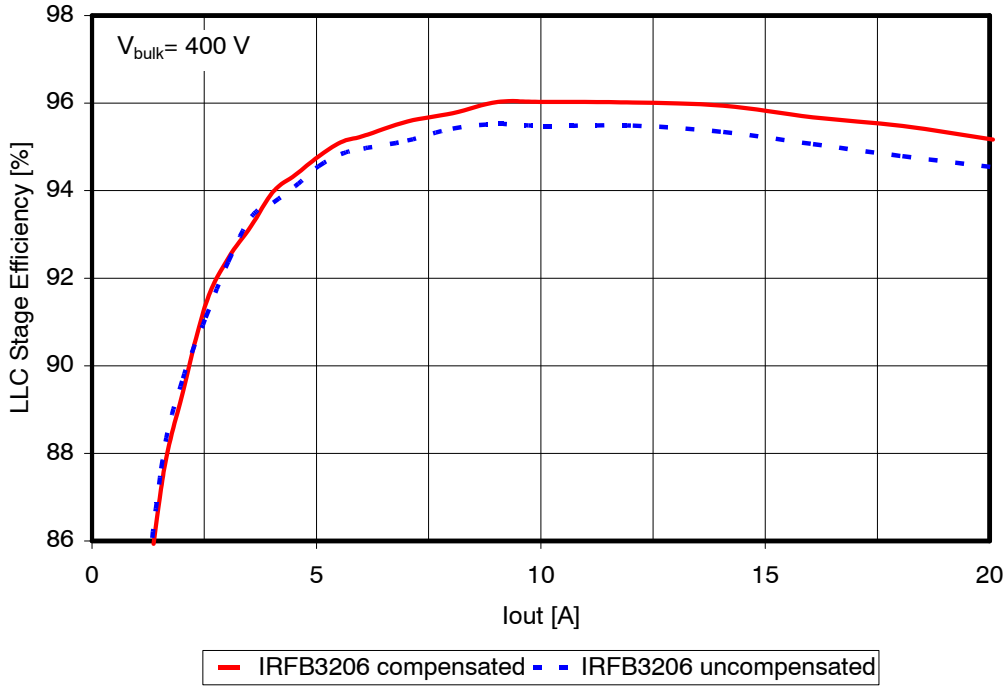

Figure 54. LLC Stage Efficiency versus Output Current for Compensated and Uncompensated SR Systems Featuring IRFB3206 MOSFETs and Nominal Bulk Voltage of 400 Vdc

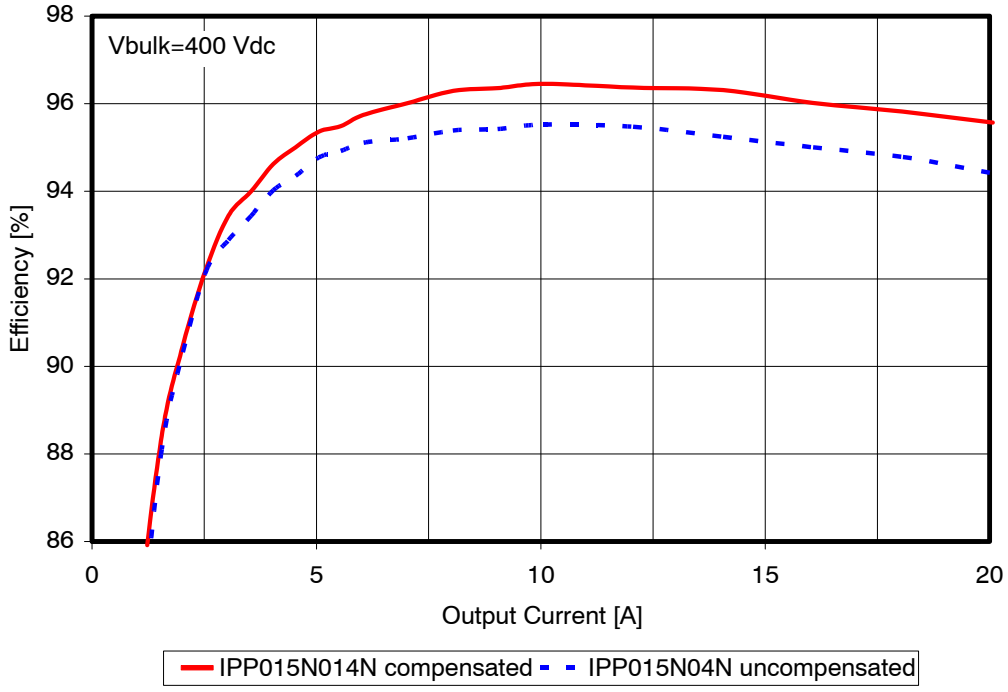

Figure 55. LLC Stage Efficiency versus Output Current for Compensated and Uncompensated SR Systems Featuring IPP015N04N MOSFETs and Nominal Bulk Voltage of 400 Vdc

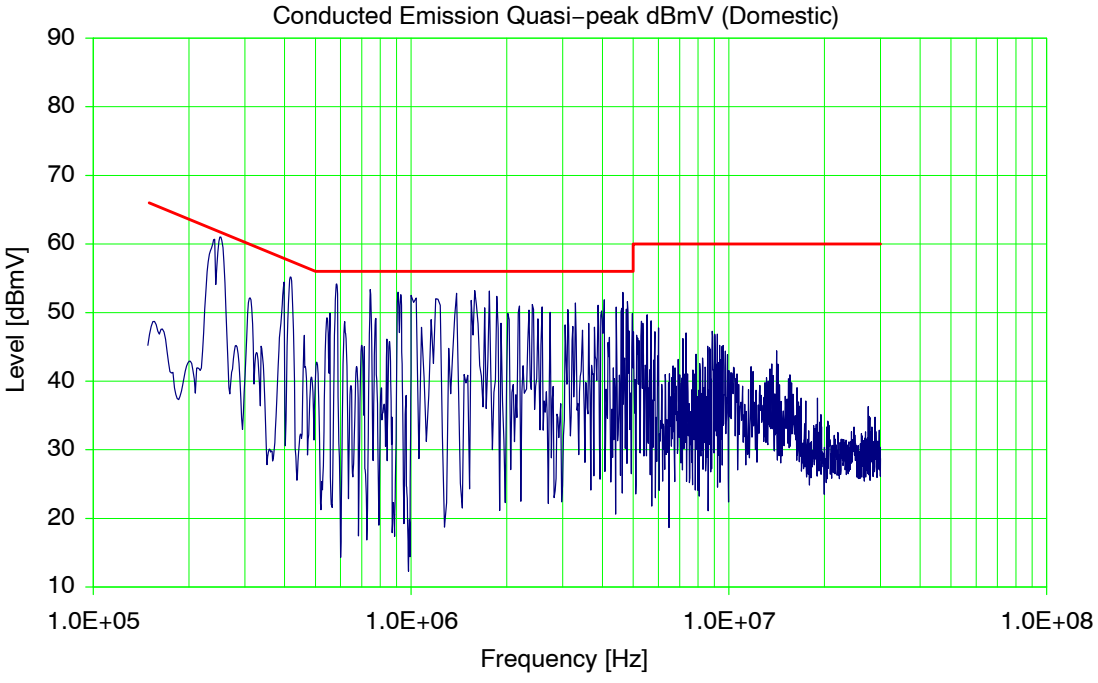

Figure 56. Conducted EMI Signature of the Board at Full Load and 110 V_{AC} Input

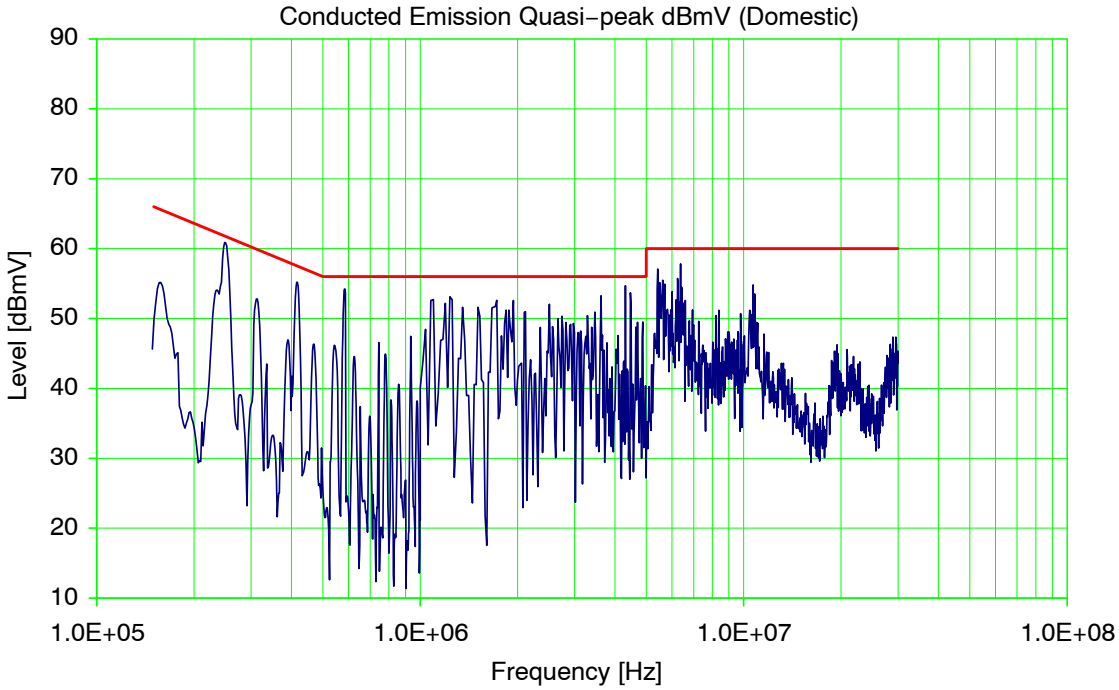

Figure 57. Conducted EMI Signature of the Board at Full Load and 230 V_{AC} Input

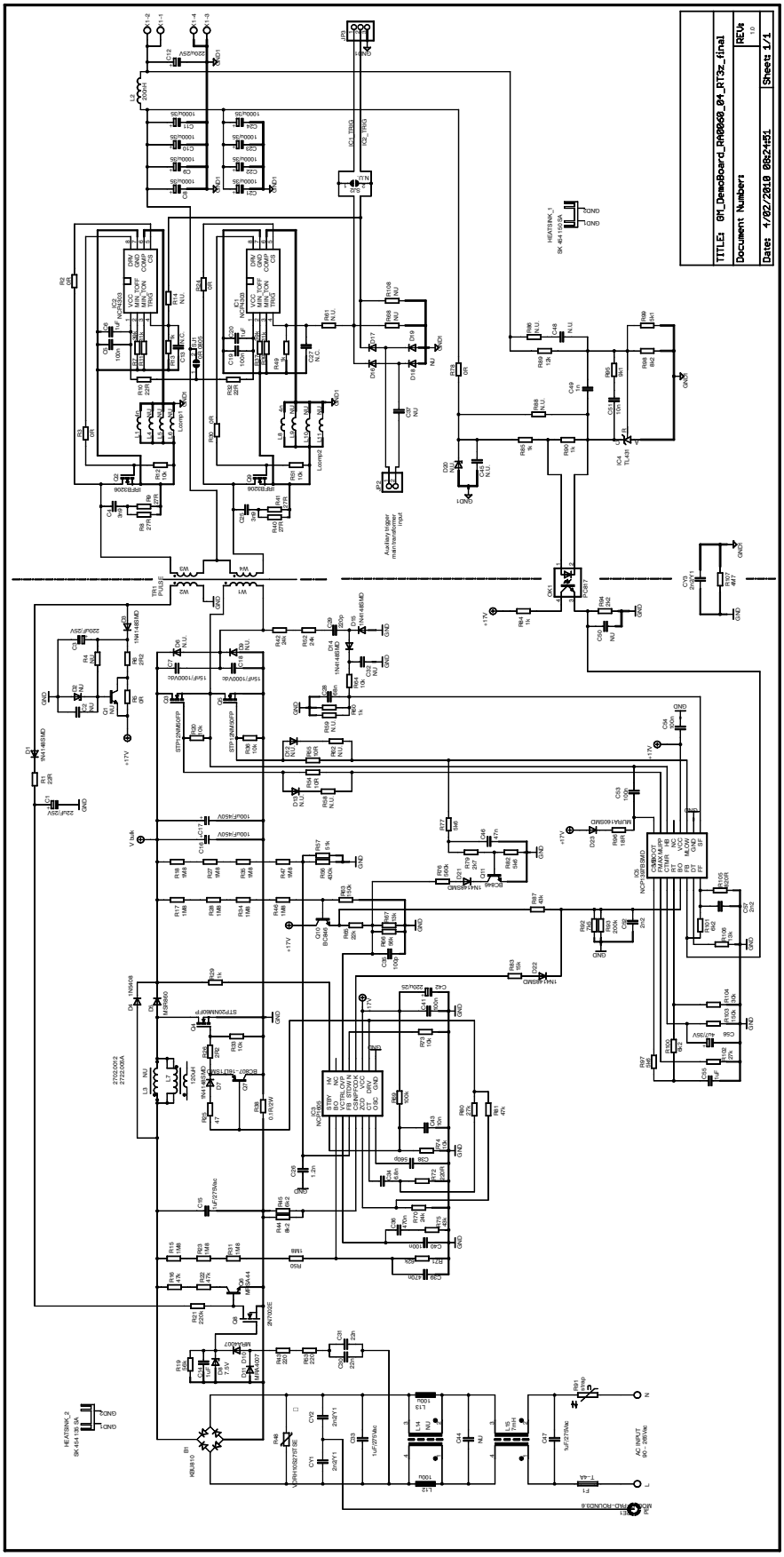

Figure 58. Demoboard Schematic Including PCB Options

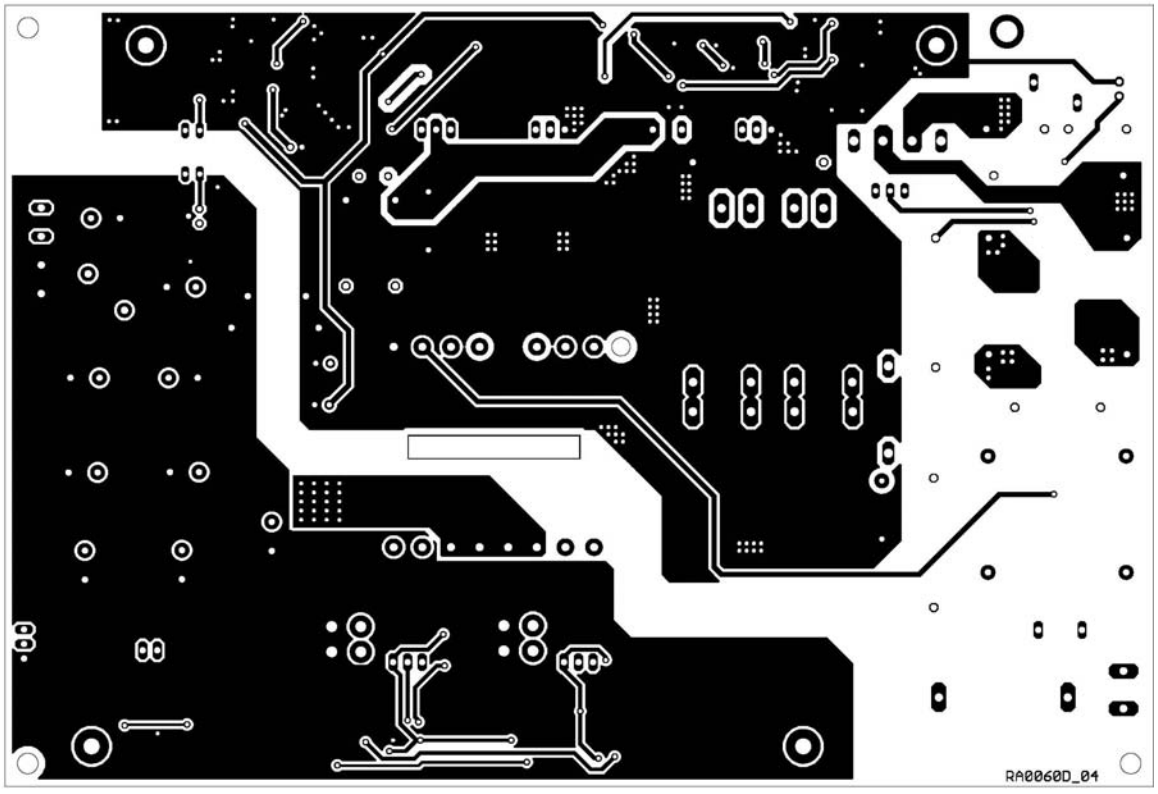

Figure 59. Top Side of the PCB

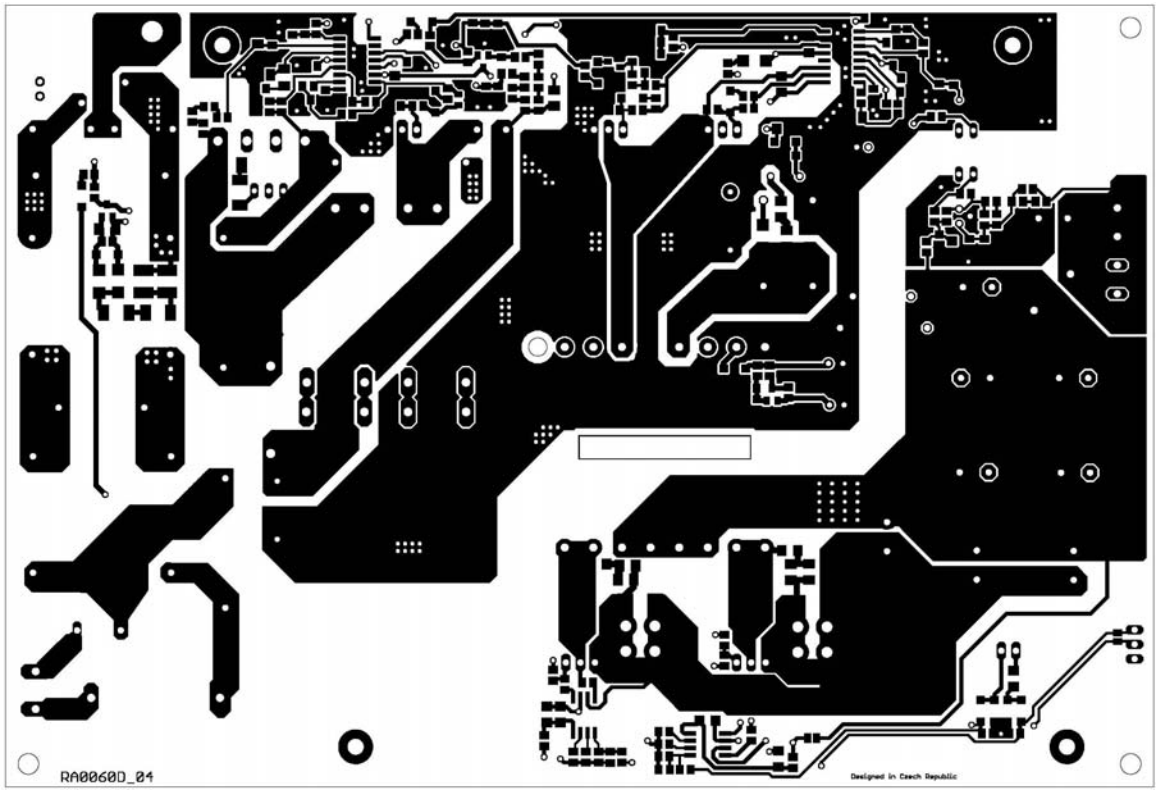

Figure 60. Bottom Side of the PCB

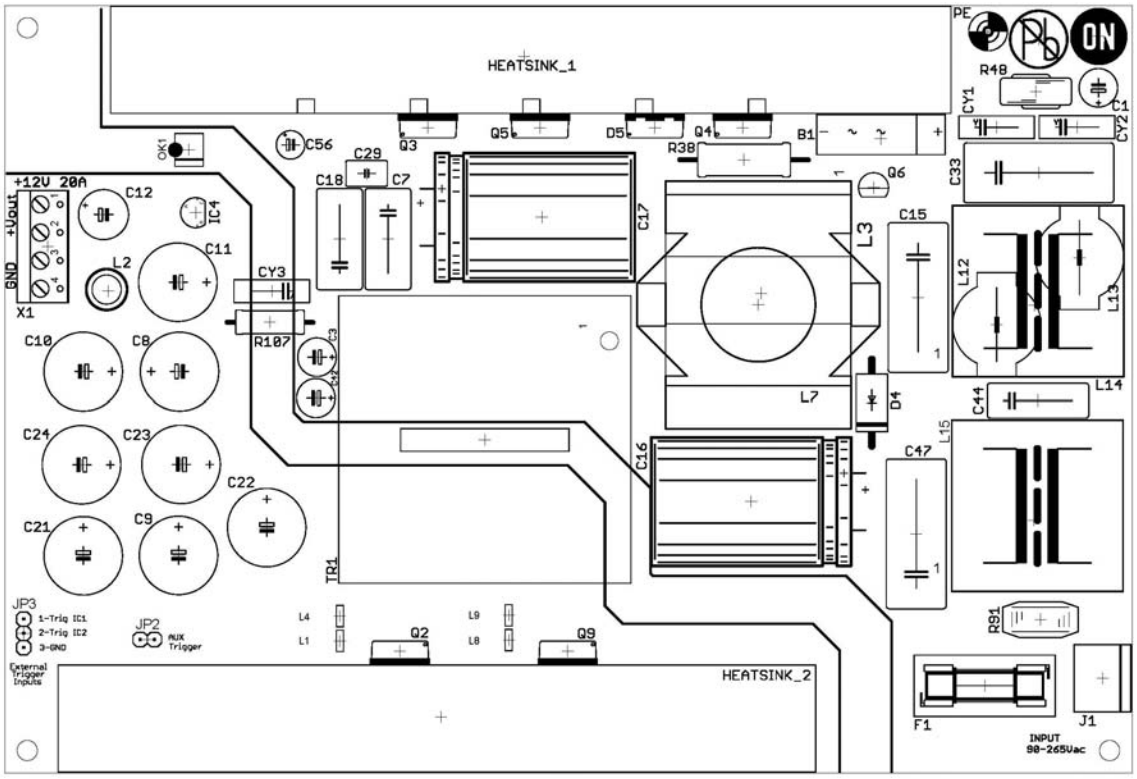

Figure 61. Top Labels

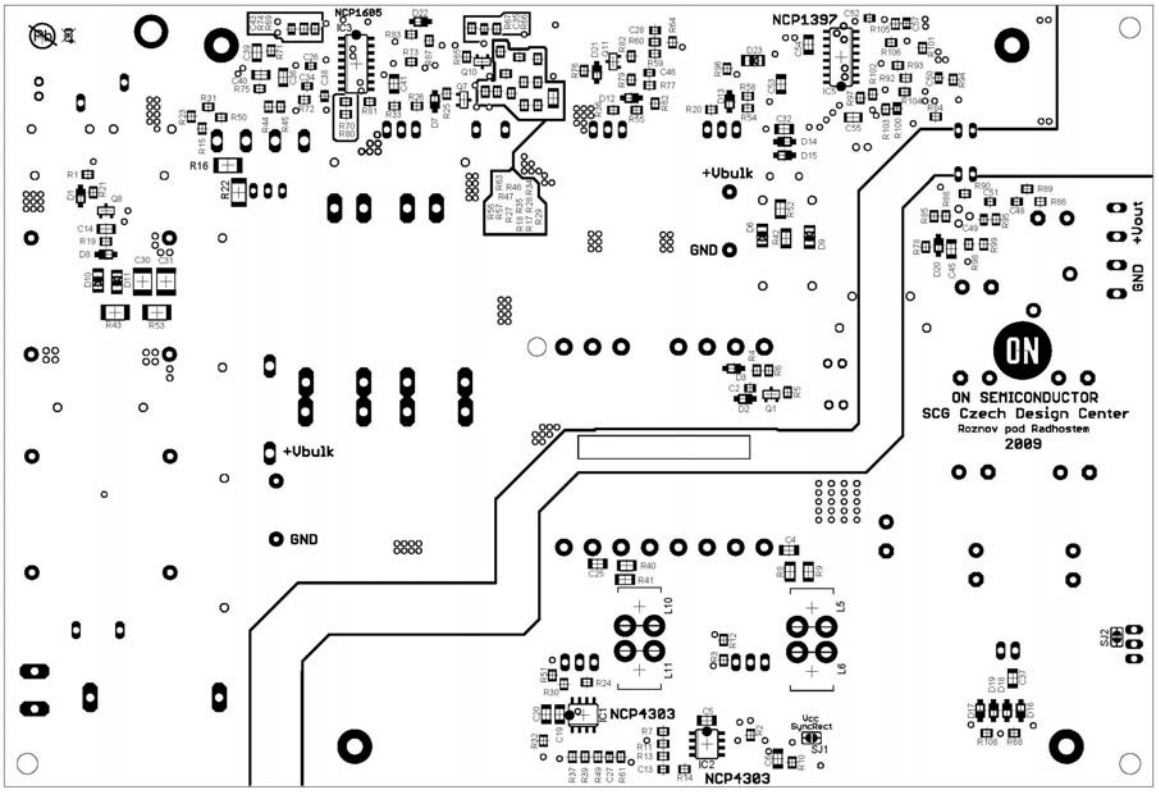

Figure 62. Bottom Labels

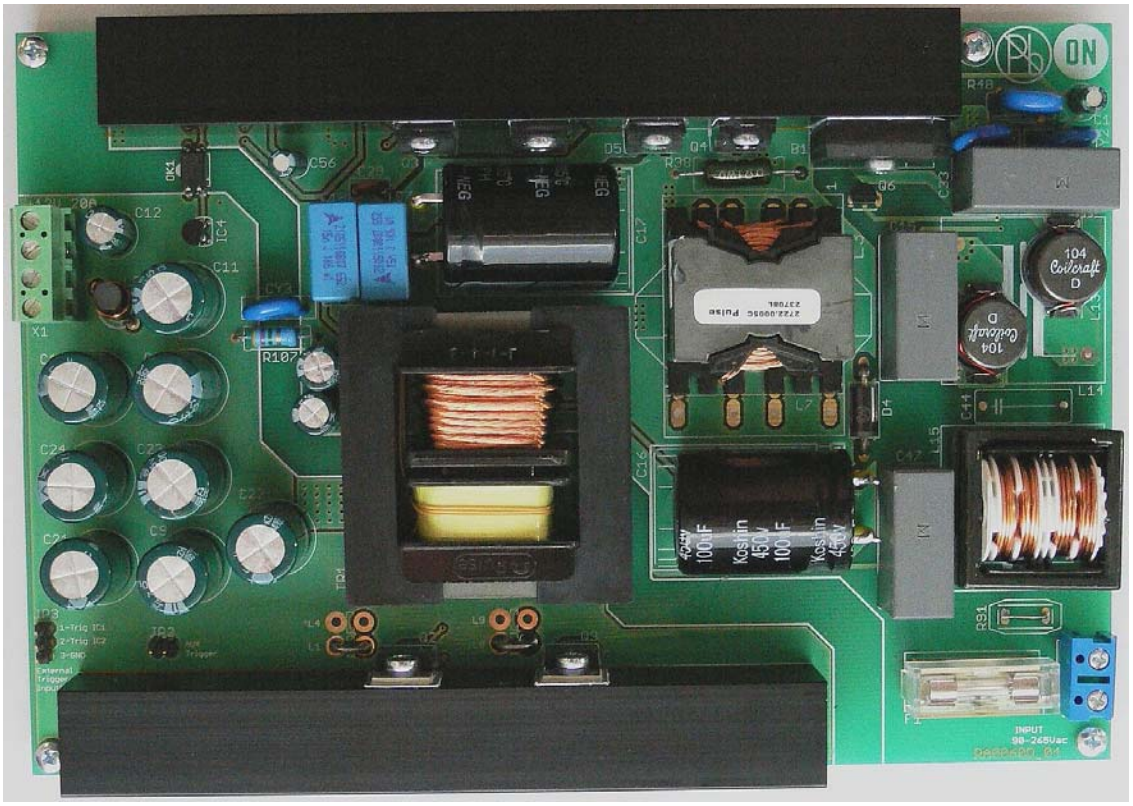

Figure 63. Demoboard Photo – Top Side

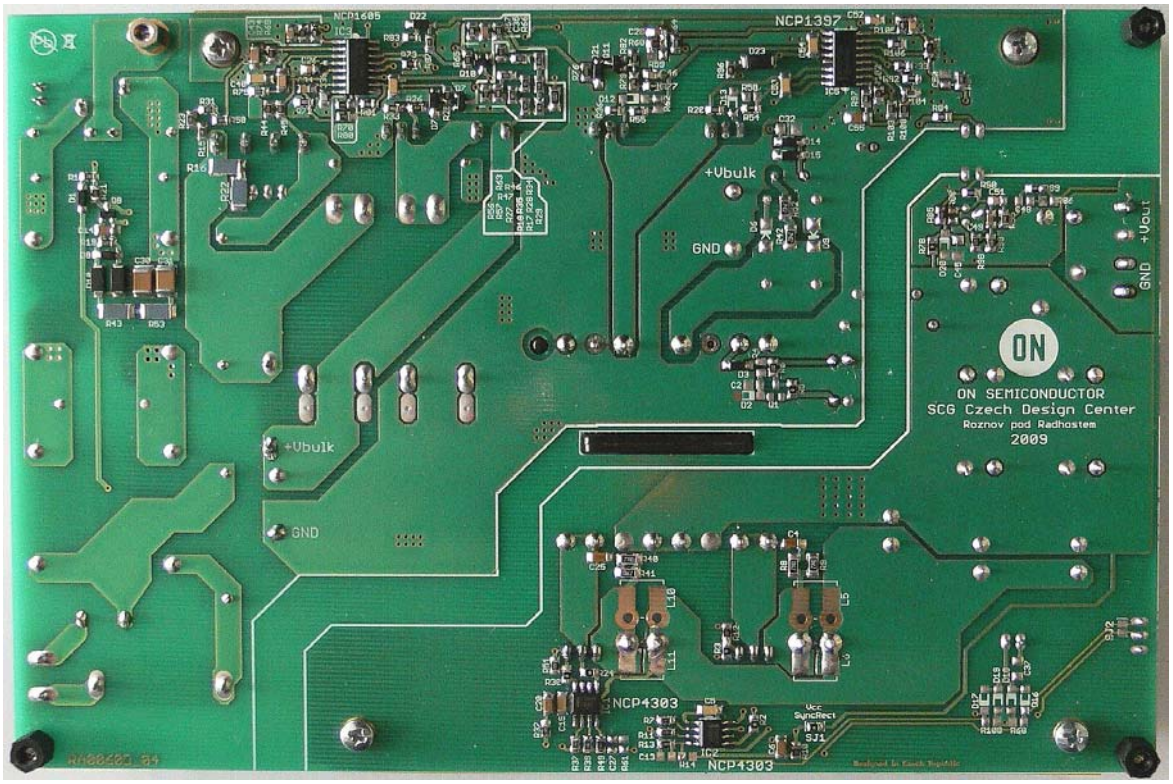

Figure 64. Demoboard Photo – Bottom Side

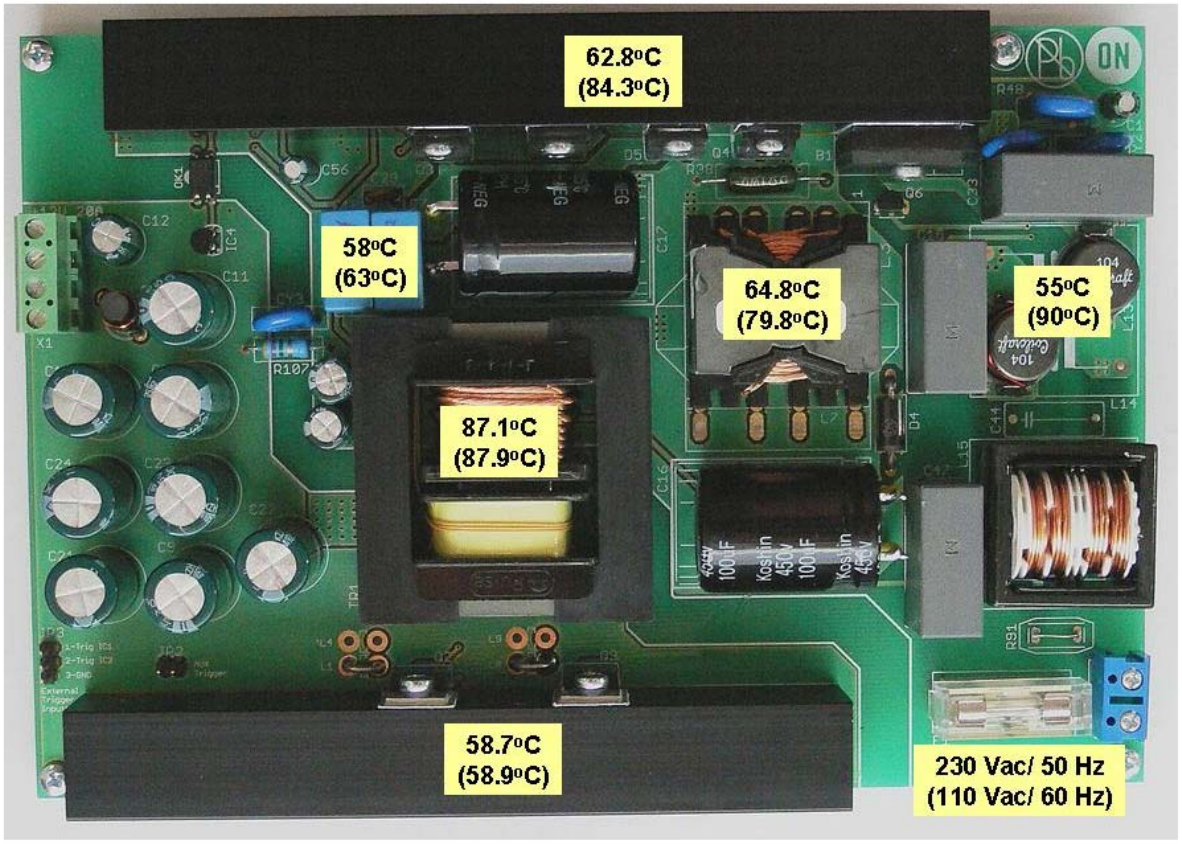

Figure 65. Demoboard Photo, Top Side with Measured Temperatures on the Full Loaded Board

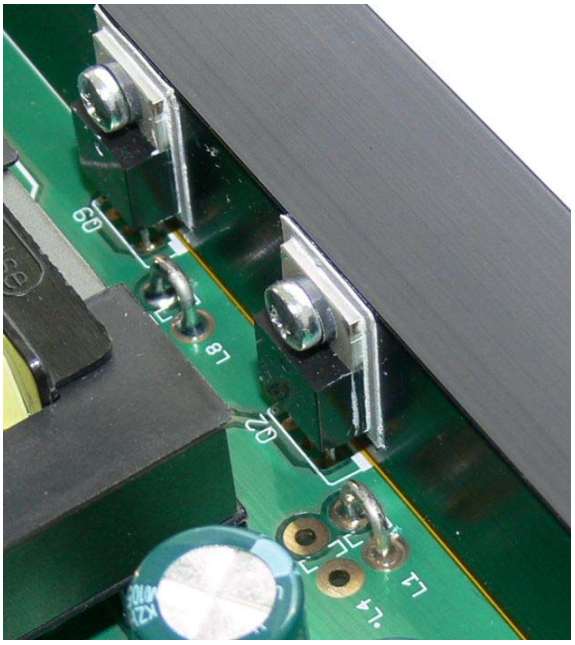

Figure 66. Detail Photo of the SR Compensation Inductances

Table 6. BILL OF MATERIALS FOR THE NCP4303 DEMO BOARD

Designator	Qty	Description	Value	Toler-ance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Pb−Free
B1	1	Bridge Rectifier	KBU8M	–	KBU8M	Fairchild	KBU8M	Yes	Yes
C1	1	Electrolytic Capacitor	22 mF / 25 V	20%	Through Hole	Koshin	KZH−025V220MC110	Yes	Yes
C3, C12, C42	3	Electrolytic capacitor	220 mF / 25 V	20%	Through Hole	Koshin	KZH−025V221MF115	Yes	Yes
C2, C13, C27	3	MKP Capacitor	NU	–	805	–	–	Yes	Yes
C6, C14, C20, C55	4	Ceramic Capacitor	1 mF	10%	1206	Kemet	C1206F105K5RACTU	Yes	Yes
C15, C33, C47	3	MKP Capacitor	1.0 μF / 275 Vac	20%	Through Hole	Epcos	B32923C3105M	Yes	Yes
C16, C17	1	Electrolytic Bulk Capacitor	100 μF / 450 V	20%	Through Hole	Koshin	KPH−450V100UF	Yes	Yes
C50	1	Ceramic Capacitor	NU	–	805	–	–	Yes	Yes
C26	1	Ceramic Capacitor	1.2 nF	10%	805	Kemet	C0805C124K1RACTU	Yes	Yes
C38	1	Ceramic Capacitor	560 pF	10%	805	Kemet	C0805C561K5RACTU	Yes	Yes
C28	1	Ceramic Capacitor	68 nF	10%	805	Kemet	C0805C683K5RACTU	Yes	Yes
C29	1	Ceramic Capacitor	220 pF	10%	Through Hole	Kemet	C0805C221K5RACTU	Yes	Yes
C30, C31	2	Ceramic Capacitor	22 nF / 1 kV	10%	1812	Kemet	C1812C223KDRACTU	Yes	Yes
C32, C37	2	Ceramic Capacitor	NU	–	1206	–	–	Yes	Yes
C34	1	Ceramic Capacitor	6.8 nF	10%	805	Kemet	C0805C682K5RACTU	Yes	Yes
C35	1	Ceramic Capacitor	100 pF	10%	805	Kemet	C0805C101K5GACTU	Yes	Yes
C36, C39	2	Ceramic Capacitor	470 nF	10%	1206	Kemet	C1206C474K5RACTU	Yes	Yes
C4, C25	2	Ceramic Capacitor	3.9 nF	10%	1206	Kemet	C1206C392K5RACTU	Yes	Yes
C5, C19,C40, C41, C53, C54	6	Ceramic Capacitor	100 nF	10%	1206	Kemet	C1206C104K5RACTU	Yes	Yes
C43, C51	2	Ceramic Capacitor	10 nF	10%	805	Kemet	C0805C103K5RACTU	Yes	Yes
C44	1	Capacitor	NU	–	Through Hole	–	–	Yes	Yes
C45	1	Ceramic Capacitor	NU	–	1206	–	–	Yes	Yes
C46	1	Ceramic Capacitor	47 nF	10%	805	Kemet	C0805C473K5RACTU	Yes	Yes
C48	1	Ceramic Capacitor	NU	–	805	–	–	Yes	Yes
C49	1	Ceramic Capacitor	1 nF	10%	805	Kemet	C0805C102K5RACTU	Yes	Yes
C52, C57	2	Ceramic Capacitor	2.2 nF	10%	805	Kemet	C0805C222K5RACTU	Yes	Yes
C56	1	Electrolytic Capacitor	4.7 mF / 50 V	20%	Through Hole	Koshin	KLH−050V4R7MC110	Yes	Yes
C7, C18	2	Metal Film Capacitor	15 nF / 1600 V	5%	Through Hole	Epcos	B32652A1153J	No	Yes
C8, C9, C10, C11, C21, C22, C23, C24	8	Electrolytic Capacitor	1000 mF / 35 V	20%	Through Hole	Koshin	KZH−035V102MH250	Yes	Yes
CY1, CY2, CY3	3	Ceramic Capacitor	2.2 nF / Y1/X1	20%	Through Hole	Murata	DE1E3KX222MA5B	Yes	Yes
D1, D3, D7, D14, D15, D21, D22, D23, R6	9	Switching Diode	MMSD4148	–	SOD−123	ON Semiconductor	MMSD4148T3G	No	Yes
D10, D11	2	Surface Mount Ultrafast Power Rectifier	MURA160	–	SMA	ON Semiconductor	MURA160T3G	No	Yes
D12, D13	2	Diode	NU	–	SOD−123	–	–	Yes	Yes
D16, D17, D18, D19	4	Diode	NU	–	SOD−123	–	–	Yes	Yes
D2	1	Diode	NU	–	SOD−123	–	–	Yes	Yes
D20	1	Diode	NU	–	SOD−123	–	–	Yes	Yes
D4	1	Standard Recovery Rectifier	1N5408	–	Axial Lead	ON Semiconductor	1N5408RLG	No	Yes
D5	1	Soft Recovery Rectifier	MSRF860	–	TO220 (2 LEAD)	ON Semiconductor	MSRF860G	No	Yes
D6, D9	2	Diode	NU	–	SMA	–	–	Yes	Yes

Table 6. BILL OF MATERIALS FOR THE NCP4303 DEMO BOARD

Designator	Qty	Description	Value	Toler-ance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Pb−Free
D8	1	Zener Diode	7.5 V	5%	SOD−123	ON Semiconductor	MMSZ7V5T1G	No	Yes
HEATSINK_1	1	Heat Sink	SK 454 150 SA	−	SK 454 150 SA	Fischer Elektronik	SK 454 150 SA	Yes	Yes
HEATSINK_2	1	Heat Sink	SK 454 135 SA	−	SK 454 135 SA	Fischer Elektronik	SK 454 135 SA	Yes	Yes
IC1, IC2	2	Secondary Side Synchronous Rectifier	NCP4303B	−	SOIC−8	ON Semiconductor	NCP4303BDR2G	No	Yes
IC3	1	Power Factor Controller	NCP1605	−	SOIC−16	ON Semiconductor	NCP1605ADR2G	No	Yes
IC4	1	Programmable Precision Reference	TL431	0.4%	TO−92	ON Semiconductor	TL431BCLPG	No	Yes
IC5	1	Resonant Mode Controller	NCP1397B	−	SOIC−16	ON Semiconductor	NCP1397BDR2G	No	Yes
J1	1	Input Terminal Block	Pitch 7.5 mm	−	CTB0110/2	Camden El.	CTB0110/2	Yes	Yes
JP2	1	Jumper 1x2	−	−	2 x 2.54 mm	Various	−	Yes	Yes
JP3	1	Jumper 1x3	−	−	3 x 2.54 mm	Various	−	Yes	Yes
L1, L8	2	Inductor − Wire Strap	−	−	Wire Strap	−	−	Yes	Yes
L12, L13	2	Inductor	100 μH	20%	DO5040H	Coilcraft	DO5040H−104MLB	Yes	Yes
L14	1	Inductor	NU	−	−	−	−	Yes	Yes
L15	1	EMI filter	7 mH	15%	TLBI	Pulse	6001.0069	Yes	Yes
L2	1	Inductor	200 nH	20%	L−US20A	Bohemia Electric	TC−05001510−00	Yes	Yes
L3	1	Inductor	NU	−	−	−	−	Yes	Yes
L4, L5, L6, L9, L10, L11	6	Inductor	NU	−	−	−	−	Yes	Yes
L7	1	Inductor	120 μH	10%	2722.0005C	Pulse	2722.0005C	Yes	Yes
OK1	1	Opto Coupler	HCPL−817	−	DIP−4	Avago Technologies	HCPL−817−000E	Yes	Yes
Q1	1	General Purpose Transistor	NU	−	SOT−123	−		Yes	Yes
Q10, Q11	2	General Purpose Transistor NPN	BC846	−	SOT−123	ON Semiconductor	BC846ALT1G	No	Yes
Q2, Q9	2	MOSFET transistor	IRFB3206	−	TO−220	International Rectifier	IRFB3206GPBF	Yes	Yes
Q3, Q5	2	MOSFET transistor	STP12NM50FP	−	TO−220	ST Microelectronics	STP12NM50FP	Yes	Yes
Q4	1	MOSFET transistor	STP20NM60FP	−	TO−220	ST Microelectronics	STP20NM60FP	Yes	Yes
Q6	1	High Voltage Transistor NPN	MPSA44	−	TO−92	ON Semiconductor	MPSA44RL1G	No	Yes
Q7	1	PNP General Purpose Transistor	BC807−16L	−	SOT−22	ON Semiconductor	BC807−16LT1G	No	Yes
Q8	1	Small Signal MOSFET N−Channel	2N7002E	−	SOT−23	ON Semiconductor	2N7002ET1G	No	Yes
R1, R10, R32	3	Resistor SMD	22 R	1%	805	Rohm Semiconductor	MCR10EZPF22R0	Yes	Yes
R100, R101	2	Resistor SMD	6.2 k	1%	805	Rohm Semiconductor	MCR10EZHF6201	Yes	Yes
R104	1	Resistor SMD	30 k	1%	805	Rohm Semiconductor	MCR10EZHF3002	Yes	Yes
R105	1	Resistor SMD	820 R	1%	805	Rohm Semiconductor	MCR10EZPF8200	Yes	Yes
R107	1	Resistor trough hole, high voltage	4.7 M	5%	414	Vishay	VR37000004704JA100	Yes	Yes
R11, R39	2	Resistor SMD	11 k	1%	805	Rohm Semiconductor	MCR10EZPF1102	Yes	Yes
R12, R20, R33, R36, R51, R64, R73, R74	8	Resistor SMD	10 k	1%	805	Rohm Semiconductor	MCR10EZPF1002	Yes	Yes
R13, R49, R60, R84, R85, R90	6	Resistor SMD	1 k	1%	805	Rohm Semiconductor	MCR10EZPF1001	Yes	Yes
R14, R58, R59, R61, R62, R86, R88	7	Resistor SMD	NU	−	805	−	−	Yes	Yes

Table 6. BILL OF MATERIALS FOR THE NCP4303 DEMO BOARD

Designator	Qty	Description	Value	Toler-ance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Pb−Free
R15, R17, R18, R23, R27, R28, R31, R34, R35, R46, R47, R50	12	Resistor SMD	1.8 M	1%	805	Rohm Semiconductor	MCR10EZHF1804	Yes	Yes
R16, R22	2	Resistor SMD	47 k	5%	2010	Vishay	CRCW201047K0JNEF	Yes	Yes
R19, R66	2	Resistor SMD	56 k	1%	805	Rohm Semiconductor	MCR10EZHF5602	Yes	Yes
R2, R3, R24, R30, R78	5	Resistor SMD	0 R	–	805	Rohm Semiconductor	MCR10EZPJ000	Yes	Yes
R21	1	Resistor SMD	220 k	1%	805	Rohm Semiconductor	MCR10EZPF2203	Yes	Yes
R25	1	Resistor SMD	47 R	1%	805	Rohm Semiconductor	MCR10EZPF47R0	Yes	Yes
R29	1	Resistor SMD	1 k	1%	1206	Rohm Semiconductor	MCR18EZPF1001	Yes	Yes
R38	1	Resistor Through Hole	0.1 R / 3 W	1%	Axial Lead	Vishay	PAC300001007FAC000	Yes	Yes
R4, R68, R108	3	Resistor SMD	NU	–	805	–	–	Yes	Yes
R42, R52	2	Resistor SMD	24 k	1%	1206	Rohm Semiconductor	MCR18EZPF2402	Yes	Yes
R43, R53	2	Resistor SMD	220 R	5%	2010	Vishay	CRCW2010220RJNEF	Yes	Yes
R44, R98	2	Resistor SMD	8.2 k	1%	805	Rohm Semiconductor	MCR10EZHF8201	Yes	Yes
R45	1	Resistor SMD	6.2 k	1%	805	Rohm Semiconductor	MCR10EZHF6201	Yes	Yes
R48	1	Varistor	S10K275	–	Disc – 10 mm	Epcos	B72210S0271K101	Yes	Yes
R54, R55	2	Resistor SMD	10 R	1%	805	Rohm Semiconductor	MCR10EZPF10R0	Yes	Yes
R56	1	Resistor SMD	430 k	1%	805	Rohm Semiconductor	MCR10EZPF4303	Yes	Yes
R57	1	Resistor SMD	51 k	1%	805	Rohm Semiconductor	MCR10EZHF5102	Yes	Yes
R5, R26	2	Resistor SMD	2.2 R	1%	805	Rohm Semiconductor	MCR10EZHJ2R2	Yes	Yes
R63, R103	2	Resistor SMD	150 k	1%	805	Rohm Semiconductor	MCR10EZPF1503	Yes	Yes
R65	1	Resistor SMD	22 k	1%	805	Rohm Semiconductor	MCR10EZHF2202	Yes	Yes
R67, R106	2	Resistor SMD	13 k	1%	805	Rohm Semiconductor	MCR10EZHF1302	Yes	Yes
R69	1	Resistor SMD	100k	1%	805	Rohm Semiconductor	MCR10EZPF1003	Yes	Yes
R7, R37	2	Resistor SMD	39 k	1%	805	Rohm Semiconductor	MCR10EZHF3902	Yes	Yes
R70	1	Resistor SMD	24 k	1%	805	Rohm Semiconductor	MCR10EZHF2402	Yes	Yes
R71	1	Resistor SMD	62 k	1%	805	Rohm Semiconductor	MCR10EZHF6202	Yes	Yes
R72	1	Resistor SMD	220 R	1%	805	Rohm Semiconductor	MCR10EZPJ221	Yes	Yes
R75, R87	2	Resistor SMD	43 k	1%	805	Rohm Semiconductor	MCR10EZHF4302	Yes	Yes
R76	1	Resistor SMD	560 k	1%	805	Rohm Semiconductor	MCR10EZPF5603	Yes	Yes
R77, R82, R97	3	Resistor SMD	5.6 k	1%	805	Rohm Semiconductor	MCR10EZHF5601	Yes	Yes
R79	1	Resistor SMD	2.7 k	1%	805	Rohm Semiconductor	MCR10EZHF2701	Yes	Yes
R8, R9, R40, R41	4	Resistor SMD	27 R	1%	1206	Rohm Semiconductor	MCR18EZPF27R0	Yes	Yes
R80, R102	2	Resistor SMD	27 k	1%	805	Rohm Semiconductor	MCR10EZHF2702	Yes	Yes
R81	1	Resistor SMD	47 k	1%	805	Rohm Semiconductor	MCR10EZHF4702	Yes	Yes
R83	1	Resistor SMD	15 k	1%	805	Rohm Semiconductor	MCR10EZHF1502	Yes	Yes
R89	1	Resistor SMD	12 k	1%	805	Rohm Semiconductor	MCR10EZHF1202	Yes	Yes
R91	1	NTC Thermistor	B57235S509M	20%	Disc – Radial	Epcos	B57235S509M	Yes	Yes
R92	1	Resistor SMD	7.5 k	1%	805	Rohm Semiconductor	MCR10EZHF2701	Yes	Yes
R93	1	Resistor SMD	200 k	1%	805	Rohm Semiconductor	MCR10EZPF2003	Yes	Yes
R94	1	Resistor SMD	2.2 k	1%	805	Rohm Semiconductor	MCR10EZHF2201	Yes	Yes
R95	1	Resistor SMD	9.1 k	1%	805	Rohm Semiconductor	MCR10EZHF9101	Yes	Yes
R96	1	Resistor SMD	18 R	1%	805	Rohm Semiconductor	MCR10EZPF18R0	Yes	Yes
R99	1	Resistor SMD	5.1 k	1%	805	Rohm Semiconductor	MCR10EZHF5101	Yes	Yes

Table 6. BILL OF MATERIALS FOR THE NCP4303 DEMO BOARD

Designator	Qty	Description	Value	Toler-ance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Pb−Free
SJ1	1	SMD Jumper	0 R	5%	805	Rohm Semiconductor	MCR10EZPJ000	Yes	Yes
SJ2	1	SMD Jumper	NU	–	–	–	–	Yes	Yes
TR1	1	Transformer	–	–	–	Pulse	See AN for spec	Yes	Yes
X1	2	Output Terminal Block	Pitch 5 mm	–	20.700M/2	IMO	20.700M/2	Yes	Yes
F1 – Cover	1	Cover, PCB Fuse Holder	–	–	–	Multicomp	MCHTC−150M	Yes	Yes
F1 – Fuse	1	Fuse, Medium Delay	4 A	–	–	Bussmann	TDC 210−4A	Yes	Yes
F1 – Holder	1	Fuse Holder	–	–	SH22.5A	Multicomp	MCHTC−15M	Yes	Yes

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