ON Semiconductor

Is Now

To learn more about onsemi™, please visit our website at
www.onsemi.com

AND8149/D

Understanding and Using the NCV1124 VR Sensor Interface

ON Semiconductor®

http://onsemi.com

APPLICATION NOTE

The NCV1124 offers a dual−channel low component count interface solution for ground referenced variable reluctance sensors. The product is easy to use when the basic circuit operation is understood and when certain application guidelines are followed. This note, along with the NCV1124 data sheet (NCV1124/D) will provide the user with the information necessary for successful application.

Circuit Basics

Each channel of the NCV1124 has independent input bias and clamp circuitry, and independent comparators with Hysteresis voltage generators. Both channels share a common reference generator for normal and diagnostic modes. A block diagram detailing one channel is shown in Figure 1 along with some of the external application components. We'll explore the circuit using one channel and, where convenient, use a subscripted "x" to indicate either channel.

The voltage developed by the VR sensor is applied through resistor R1 to the IN1 pin. When the VR sensor produces no voltage (V_{RS} = 0) the IN1 pin is biased to the voltage developed by I1 x (R1 + R_{RS}). When the diagnostic pin is at GND (normal mode) the IN1 voltage is compared by COMP1 to the voltage at the IN_{ADJ} pin developed by I2 x R_{ADJ} plus or minus V_{HYS}. When the diagnostic pin is at V_{CC} (diagnostic mode) the IN1 voltage is compared to the voltage developed by (I2 + I3) x R_{ADJ} plus V_{HYS}.

From the comparator's viewpoint, these voltages are respectively V_P and V_N, as shown by the labels in the block diagram at the comparator's inputs, P and N. When $V_N > V_P$, the comparator output will be low, transistor N1 will be off and OUT1 will be $\approx V_{CC}$. When $V_N < V_P$, the comparator output will be high, transistor N1 will be on and OUT1 will be $\approx$GND.

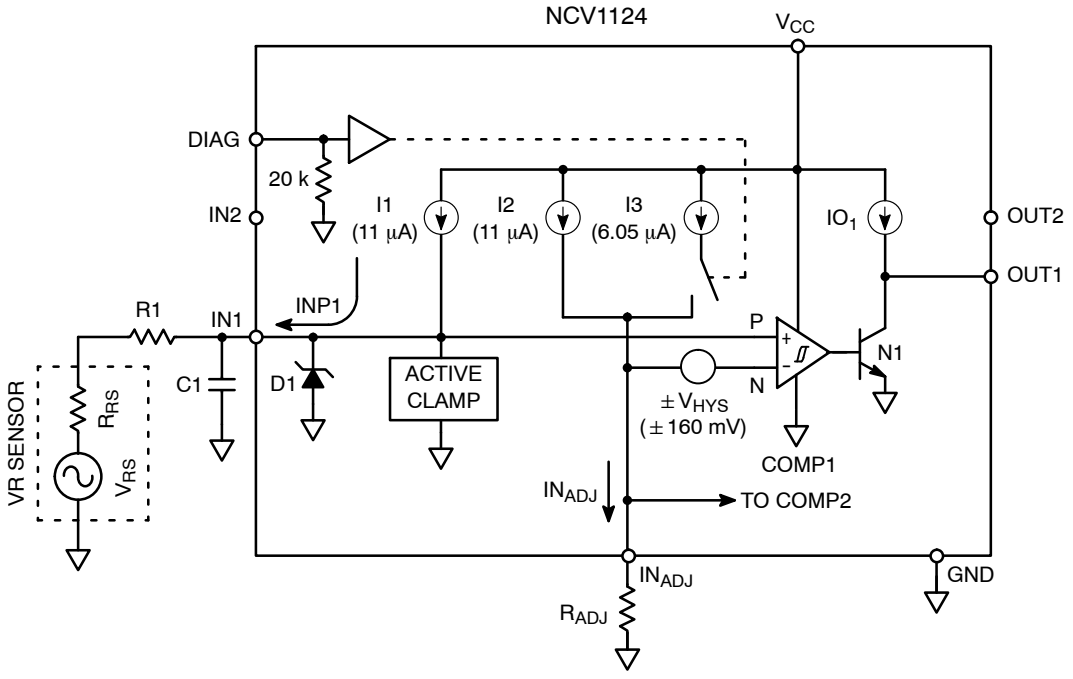

Figure 1. NCV1124 Block Diagram

The polarity of V_{HYS} is controlled by the input states of COMP1. When $V_{IN1} < V_{INADJ}$, V_{HYS} has the polarity shown in Figure 2A. When $V_{IN1} > V_{INADJ}$, V_{HYS} has the polarity shown in Figure 2B.

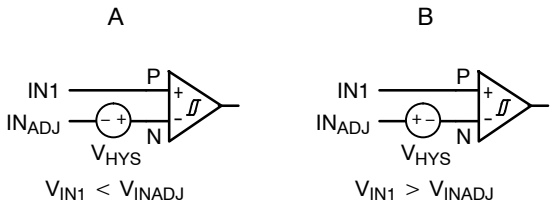

Figure 2. Hysteresis Voltage States

In the normal mode, V_{HYS} is alternately added to and subtracted from the bias voltage developed by I2 x R_{ADJ}. In the diagnostic mode, V_{HYS} is added to the bias voltage developed by (I2 + I3) x R_{ADJ}. The resultant voltages are described in the data sheet variously as $\pm V_{HYS}$ or as the trip point ($\pm$TRP) thresholds, nominally specified as $\pm$160 mV *around* the bias voltage developed by IN_{ADJ} and R_{ADJ}. Figure 3 shows the threshold and bias voltage relationships between V_{INADJ} and V_{HYS} for normal and diagnostic modes, and the bias voltage for V_{INX} (V_{IN1}).

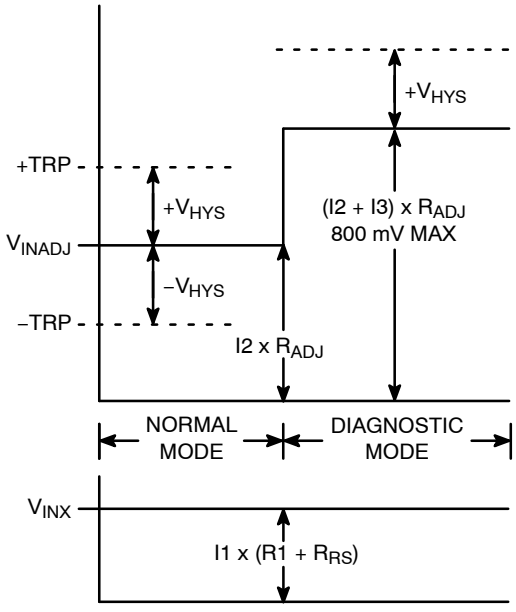

Figure 3. Comparator Bias Points and Thresholds

The resistance of R1 + R_{RS} should be substantially equal to R_{ADJ} as prescribed by the data sheet. In the normal mode $INP_X = IN_{ADJ}$ and equal resistances at the IN_X and IN_{ADJ} pins will establish equal voltage bias points. The voltage produced by the VR sensor alternates around the V_{INX} bias voltage. The $V_{INX} \pm V_{RS}$ voltage (V_P) is compared to the $\pm$TRP voltage (V_N) produced by the alternating polarity of V_{HYS} around the V_{INADJ} bias voltage. The NCV1124's normal mode input vs. output responses are shown in Figure 4. For clarity, the VR sensor voltage is shown as a triangular wave.

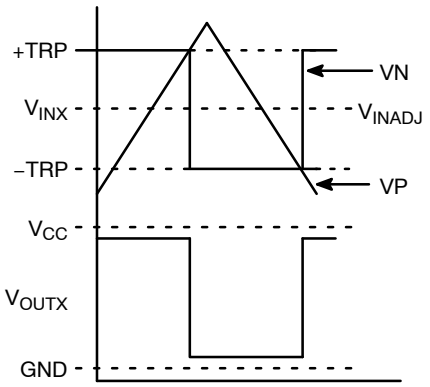

Figure 4. Input vs. Threshold and Output Responses (Normal Mode)

Let's review the circuit basics, using Figure 1. We'll use the component values of R_{RS} = 1.0 kΩ, R1 = 22 kΩ and R_{ADJ} = 24 kΩ, and we'll use the typical data sheet values: $\pm V_{HYS} = \pm 160$ mV, INP1 = 11 μA, and $IN_{ADJ} = K_I$ x INP1, where K_I = 1.00 in the normal mode and K_I = 1.55 in the diagnostic mode. We'll ignore C1 for the moment.

Assume that R_{ADJ} is zero, that DIAG = GND (normal mode), and that we've connected a voltage source (V_{RS}) to IN1. Assume also that R1 and R_{RS} are zero. OUT1 will then go low when V_{RS} is increased to slightly greater than +160 mV above GND, and then go high when V_{RS} is decreased to slightly less than –160 mV below GND. With the IN_{ADJ} pin connected to GND (R_{ADJ} = 0), $\pm$TRP = $\pm V_{HYS}$ and the trip points are $\pm V_{HYS}$ around GND. The lowest IN_X signal we can detect is $\pm V_{HYS}$.

Next we'll set R_{ADJ} = 24 kΩ, set R_{RS} = 1.0 kΩ and R1 = 22 kΩ. Using the equivalent R_{RS} + R1 resistance of 23 kΩ (R_{EQ}) and the 11 μA INP1 (I1) current, V_{IN1} (with V_{RS} = 0) will be 253 mV (11 μA x 23 kΩ). Since in the normal mode K_I = 1.00, the IN_{ADJ} current is 11 μA (I2) and V_{INADJ} is now 264 mV (11 μA x 24 kΩ). With IN_{ADJ} biased to V_{INADJ}, $\pm$TRP = $V_{INADJ} \pm V_{HYS}$ and the trip points are $\pm V_{HYS}$ around V_{INADJ}. OUT1 will change states when V_{IN1} is slightly greater than +424 mV and when V_{IN1} is slightly less than +104 mV (264 mV $\pm$ 160 mV) *above* GND.

With R_{EQ} nearly the same as R_{ADJ} and since 253 mV < 264 mV ($V_{IN1} < V_{INADJ}$), V_{HYS} will be +160 mV (Figure 2) and OUT1 will be in a high state since 253 mV < 424 mV ($V_{IN1} < V_{INADJ} + V_{HYS}$ or $V_P < V_N$). With V_{IN1} = 253 mV, OUT1 will go low when V_{RS} is slightly greater than 171 mV above V_{INADJ}, and V_{HYS} will change polarity to –160 mV. When V_{RS} is slightly less than 149 mV below V_{INADJ}, OUT1 will go high and V_{HYS} will change back to +160 mV. In the normal mode, IN_{ADJ} = INP1 and with $R_{EQ} \approx R_{ADJ}$, the lowest IN_X signal we can detect is ($V_{INADJ} - V_{INX}$) $\pm V_{HYS}$.

Now we'll set the V_{RS} voltage to zero volts. When V_{IN1} is compared to V_{INADJ} + V_{HYS} (the 424 mV trip point), OUT1 will be in a high state since 253 mV < 424 mV (V_P < V_N). If we increase R_{EQ} to slightly above 38.545 kΩ (424 mV/11 μA) OUT1 will go to a low state (V_P > V_N).

Now we'll set DIAG = V_{CC}. Since in the diagnostic mode K_I = 1.55, the current at the IN_{ADJ} pin will increase by 55% to 17.05 μA (I2 + I3) so that the IN_{ADJ} bias voltage is now 409.2 mV (17.05 μA x 24 kΩ) and the trip point is now 569.2 mV (V_{INADJ} + V_{HYS}). With V_{IN1} at 424 mV (38.545 kΩ x 11 μA) OUT1 will be in a high state since 424 mV < 569.2 mV (V_P < V_N). If we further increase R_{EQ} to slightly above 51.745 kΩ (569.2 mV/11 μA) OUT1 will go to a low state (V_P > V_N).

These results show that we can expect to diagnose minimum (R_{DMIN}) and maximum (R_{DMAX}) resistances respectively at 38.545 kΩ, equivalent to [(1.00 x R_{ADJ}) + (V_{HYS}/INP_X)] and at 51.745 kΩ, equivalent to [(1.55 x R_{ADJ}) + (V_{HYS}/INP_X)] and a resistance *change* of 51.745 kΩ – 38.545 kΩ =13.2 kΩ, equivalent to 0.55 x R_{ADJ}.

Input Clamps

There are two clamp points associated with the inputs IN1 and IN2. Figure 5 shows the simplified clamp circuitry. The data sheet specifies these points as positive (7.0 V typical) and negative (–0.30 V typical.) Since VR sensors can easily produce voltages in excess of 120 V peak, the 7.0 V clamp prevents damage to the NCV1124 by keeping these voltages below the breakdown voltage of the manufacturing process for the product. Since the substrate of an integrated circuit must always be at the lowest voltage potential, the –0.30 V clamp prevents turn–on of parasitic elements within the IC.

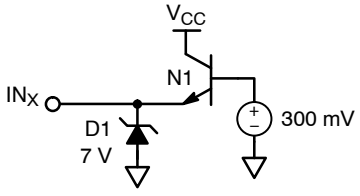

Figure 5. Simplified Input Clamp Circuit

Circuit Dynamics

Getting predictable behavior from the NCV1124 requires correct power–up and pre–conditioning of the comparators' inputs. Since there is no internal power–up control circuitry, this must be managed in the application via the components at the V_{CC} pin and the IN_X and IN_{ADJ} pins. Assuming that diagnostics are done at power–up, and since V_{INADJ} + V_{HYS} is the reference to which V_{INX} is compared, we need to establish V_{INADJ} *before* V_{INX} to guarantee predictable behavior. The RC delays imposed by pre–conditioning also need to be considered in order to obtain correct diagnostic results. The following sections will show the circuit behavior with and without the presence of a VR sensor and with several circuit modifications. The sensor used with the test circuits is a 680 mH 1.0 kΩ automotive–type sensing unit. In all cases the DIAG input is held low. Be sure to note the voltage and time scales in the graphs presented.

Powering Up

The slew rate of the V_{CC} power supply must be slow enough to allow the internal bias currents and voltages to be correctly established. Using the test circuit in Figure 6 we can observe the power–up behavior when a step is applied to the V_{CC} pin.

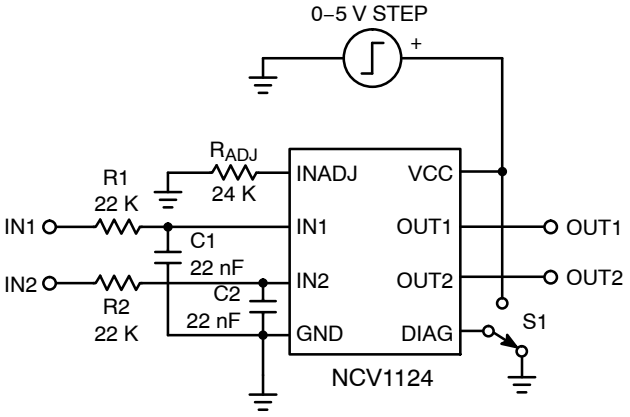

Figure 6. Test Circuit 1

The graphs of Figures 7 and 8 show the results when a 5.0 V V_{CC} step is applied to Test Circuit 1, with and without a VR sensor. In Figure 7 the V_{IN1} quickly reaches the 1.6 V clamp point despite the 22 nF capacitor at the IN1 pin. Because of the quick rise time of the V_{CC} step, the INP1 current is not yet well controlled (>>11 μA.) Figure 8 shows that when a VR sensor is present, V_{IN1} still quickly approaches the 1.6 V clamp, then decays to the level defined by INP1 x (R1 + R_{RS}). The decay rate (τ_{IN1}) is established by C1 x (R1 + R_{RS}). Note that in both graphs V_{IN1} is established *before* V_{INADJ} (our reference node) and OUT1 remains low.

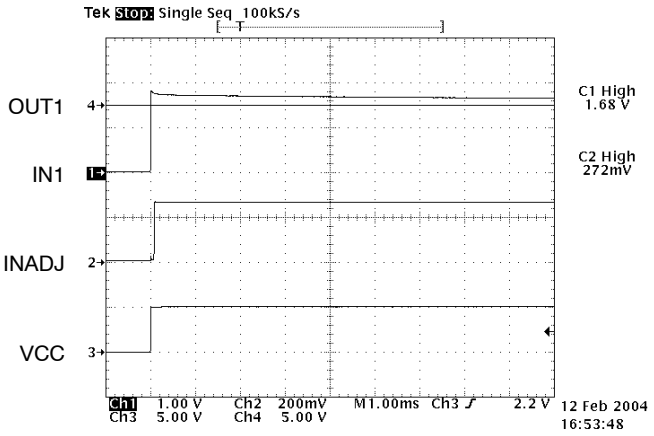

Figure 7. Sensor Absent

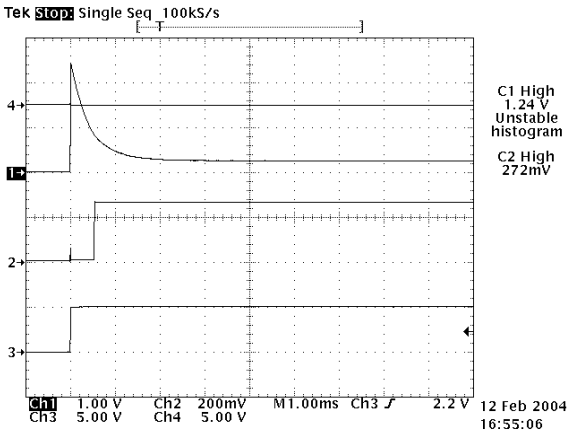

Figure 8. Sensor Present

Experiment has shown that proper operation results with a V_{CC} slew rate of about 1.0 V/μs, so limiting the slew rate to 0.5 V/μs adds sufficient margin. If the bulk filter capacitance in the application's 5.0 V regulator circuit isn't large enough to keep the slew rate to ≤ 0.5 V/μs, a simple RC network added to the V_{CC} pin can do the trick. A V_{CC} bypass capacitor is recommended in any event. Figure 9 shows the R_{SLEW}−C_{SLEW} arrangement.

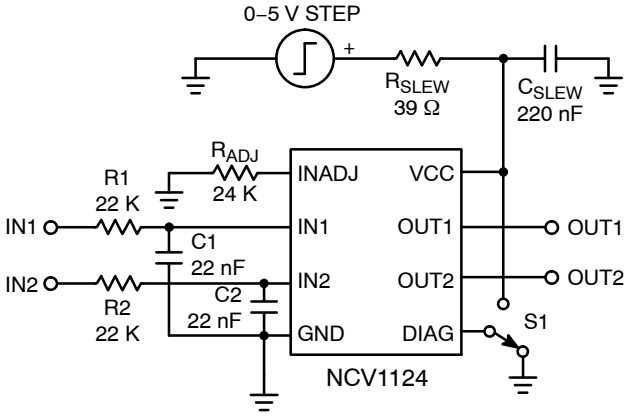

Figure 9. Test Circuit 2

The NCV1124 data sheet specifies 5.0 mA maximum operating current, so choosing R_{SLEW} = 39 Ω would produce about a 200 mV drop at the V_{CC} pin. Recalling that an exponential response is linear over the range of t = 0 to t = 0.6τ, set t/τ = 0.6 and solve for V_t: V_t = [5.0 V−0.2 V] x [1−$e^{-0.6}$] = 2.16 V. Given the 0.5 V/μs requirement, the time needed to reach 2.16 V is: 2.16 V/(0.5 V/μs) = 4.32 μs. Since this time represents t/τ = 0.6, we solve that τ = t/0.6: 4.32 μs/0.6 = 7.2 μs. Lastly we find C_{SLEW} = τ/R_{SLEW} = 185 nF and choose the next highest standard value, 220 nF.

Note that the choice for R_{SLEW} only accounted for the voltage drop produced during power−up and did not consider additional dynamic currents during output switching or activation of the negative IN_X clamps, each of which will produce additional drops (ripple voltages) at the V_{CC} pin. R_{SLEW} can be decreased and C_{SLEW} increased to reduce ripple voltages.

Figure 10 shows that our V_{CC} slew rate is now 0.425 V/μs when a 5.0 V step is applied to Test Circuit 2 (and also reveals the intrinsic start−up delay of the NCV1124's internal circuitry, ≈130 μs for the sample tested.)

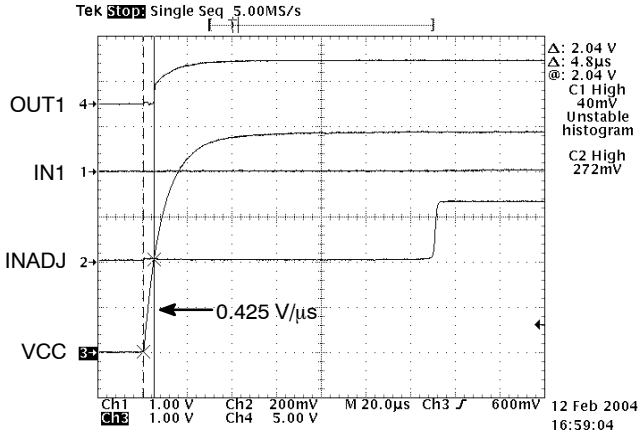

Figure 10. V_{CC} Slew ≤ 0.5 V/μs

Figures 11 and 12 show the results when a 5.0 V V_{CC} step is applied to Test Circuit 2. Figure 11 shows that the V_{IN1} ramps linearly to the 1.6 V clamp point in about 3.0 ms due to C1 and the now correctly established INP1 current. Since V_{INADJ} is already established as V_{IN1} ramps up, OUT1 initially goes high and then low when V_{IN1} crosses the +TRP threshold. Figure 12 shows that when a VR sensor is present, the V_{IN1} rises exponentially to the level defined by INP1 x (R1 + R_{RS}). Again, the rise rate (τ_{IN1}) is established by C1 x (R1 + R_{RS}). In both cases V_{IN1} has the expected response when the correctly established INP1 current step is applied to a capacitor (sensor absent) or an RC combination.

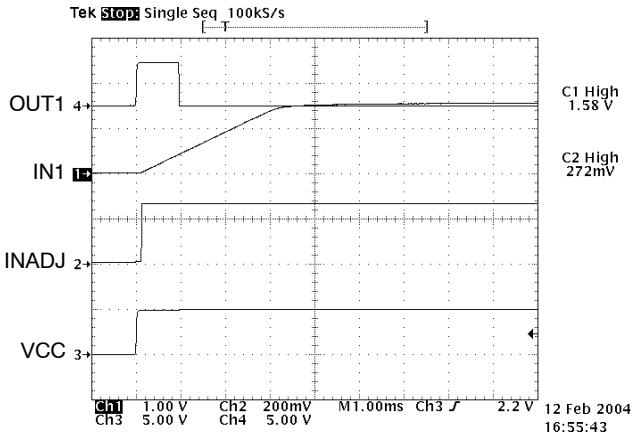

Figure 11. Sensor Absent

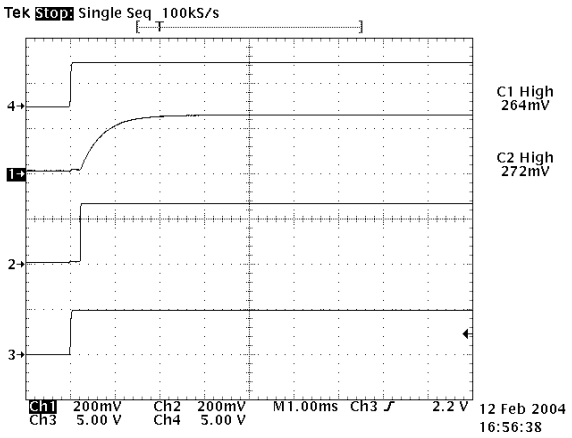

Figure 12. Sensor Present

Pre−Conditioning

As described in the data sheet, R1 and C1 provide a low pass filter and, when power−up is properly managed, also serve to pre−condition the comparator to the correct state by delaying the IN1 signal. We could also force V_{INADJ} to be quickly established regardless of the external components at the IN_X inputs. Adding a capacitor (C3 in Figure 13) between the power supply and IN_{ADJ} pin does the job for both channels. With (R1 + R_{RS}) $\approx$ R_{ADJ}, choosing C3 = C1 gives nearly equal τ_{INX} and τ_{INADJ} time constants and settling times under nominal circuit conditions.

The benefit of C3 comes with both a risk and a penalty. Power supply noise could be coupled through C3 to IN_{ADJ} and thereby risk modulation of the comparators' trip points. The risk could be reduced by using separate a "clean" supply or by using a voltage reference $\geq$ 1.6 V (the clamp voltage.) Of course, we'd have to be certain that these alternate voltages are established before the NCV1124's V_{CC} voltage. The penalty is the delay that results from the R_{ADJ} x C_3 time constant, τ_{INADJ}. We need to wait several time constants at power−up and when changing from the normal mode to the diagnostic mode before sampling OUT_X.

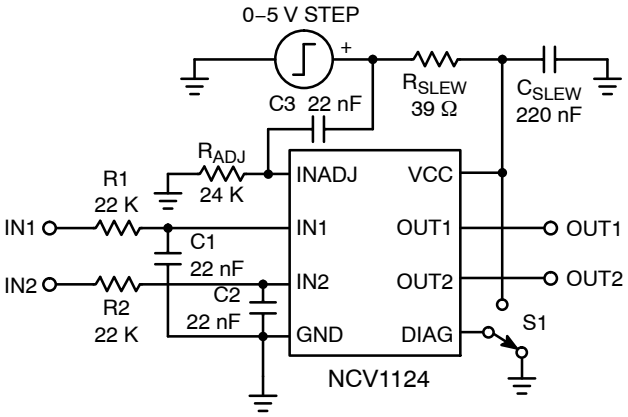

Figure 13. Test Circuit 3

Figures 14 and 15 show the results when a 5.0 V V_{CC} step is applied to Test Circuit 3. Both figures show the effect of C3 on V_{INADJ}. Since C3 initially appears as a short−circuit, V_{INADJ} is quickly brought to the power supply voltage, then decays to the bias point defined by IN_{ADJ} x R_{ADJ}. The decay rate (τ_{INADJ}) is established R_{ADJ} x C3. Again, in both cases V_{IN1} has the expected responses.

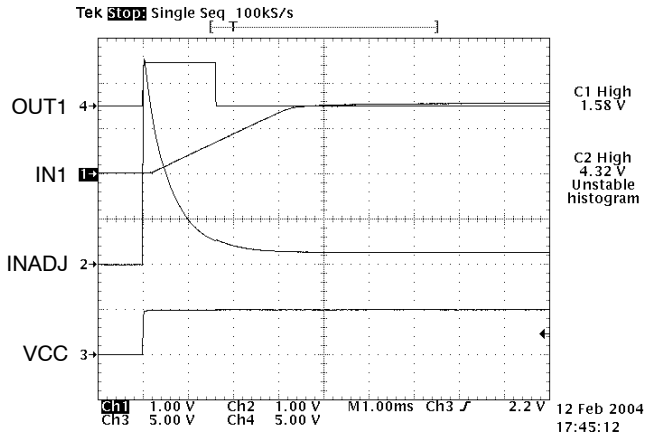

Figure 14. Sensor Absent

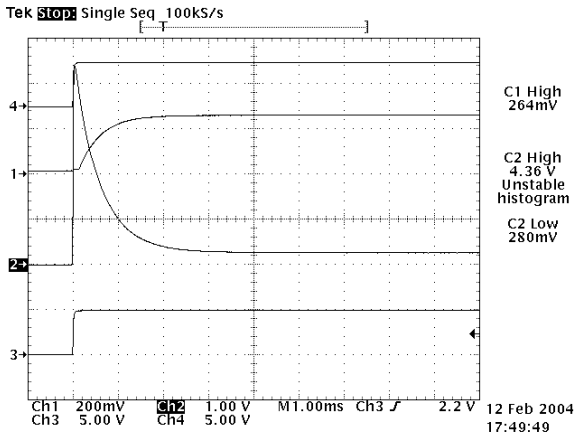

Figure 15. Sensor Present

Diagnostic Operation

Now that we've examined the circuit basics and the power−up and pre−conditioning requirements, we can examine how to interpret the NCV1124's outputs at power−up and when changing modes. We can also see the impact of the component choices and how the resulting delays (τ_{INX} and τ_{INADJ}) imposed affect diagnostics.

Each input circuit consists of a VR sensor, series resistor, and filter capacitor. While equation 13 in the data sheet shows how to determine the quality of the VR sensor resistance R_{RS}, the quality of the entire input circuit can be assessed by including the series resistor with R_{RS}: $R_{RS} + R_X = [(INP_X \times K_I \times R_{ADJ}) + V_{HYS}]/INP_X$.

A shorted sensor or shorted filter capacitor can be diagnosed if no change in the output occurs during normal operation (DIAG = GND) when it is expected that the VR sensor should produce an output voltage greater than $(V_{INADJ} - V_{INX}) \pm V_{HYS}$.

An open sensor or series resistor (Figures 11 and 14) can be diagnosed at power−up (DIAG = GND) *after* the delay that results from τ_{INADJ} and, since CV/I = t, *after* the delay (t_{INX}) that results from C_X, V_{CLAMPX}, and INP_X. V_{IN1} eventually reaches the 1.6 V clamp voltage and V_{INADJ} will eventually settle to $R_{ADJ} \times I_{NADJ}$. While Figures 12 and 15 show that OUT1 does not change state after both V_{IN1} and V_{INADJ} have settled, it is necessary to wait until after the delays before changing the state of the DIAG input to guarantee valid results. Setting DIAG = V_{CC} then will *not* change the output state since $V_{INX} >> (V_{INADJ} + V_{HYS})$ *before* changing the state of the diagnostic input.

A normal input circuit (Figures 12 and 15) can be diagnosed at power−up (DIAG = GND) *after* the τ_{INX} delay and *after* the τ_{INADJ} delay. Figures 12 and 15 also show that OUT1 does not change state after both V_{IN1} and V_{INADJ} have settled, it is again necessary to wait before changing the state of the DIAG input. Setting DIAG = V_{CC} then will *not* change the output state since V_{IN1} is already below V_{INADJ} *before* changing the state of the diagnostic input.

So how does setting DIAG = V_{CC} give us any additional information? When the input circuit resistances change enough to cause V_{INX} to be greater than $V_{INADJ} + V_{HYS}$, OUT_X will go low. When DIAG = GND, this will occur when $(R_X + R_{RS})$ is just slightly greater than $R_{DMIN} = [(1.00 \times R_{ADJ}) + (V_{HYS}/INP_X)]$. When DIAG = V_{CC}, this will occur when $(R_X + R_{RS})$ is just slightly greater than $R_{DMAX} = [(1.55 \times R_{ADJ}) + (V_{HYS}/INP_X)]$.

We've seen, after correct power up and pre−conditioning, that OUT_X will go high and remain high if the input circuit is good and that OUT_X will go low and remain low if the input circuit is bad. If OUT_X is low after power−up, then DIAG is switched to V_{CC}, OUT_X will go high if $R_{DMIN} = (R1 + R_{RS}) \leq R_{DMAX}$. So two samples of OUT_X are needed to know the quality of the input circuit: one after power−up and one after changing DIAG from low to high. Table 1 summarizes diagnostic behavior.

Table 1. Diagnostic Behavior

OUT_X After Power−Up	DIAG	OUT_X After DIAG	Circuit Quality
H	L → H	H	GOOD
L	L → H	L → H	$R_{DMIN} \leq (R1 + R_{RS}) \leq R_{DMAX}$
L	L → H	L	BAD

The worst−case delays for sampling OUT_X occur where R1 + R_{RS} is just at R_{DMIN} when $V_{IN} = V_{INADJ} + V_{HYS}$. For the Test Circuit 2 case in Figure 9, we need to wait several R_{DMIN} x C1 time constants after power−up for V_{INX} to settle before sampling OUT_X. If we wait the typical 5τ, V_{INX} will be near 99.4% of $V_{INADJ} + V_{HYS}$. We now only need to wait for the mode change delay time specified in the data sheet (20 μs max.) after changing DIAG from low to high before again sampling OUT_X.

For the Test Circuit 3 case in Figure 13, we need to wait the *longer* of several R_{DMIN} x C1 or τ_{INADJ} time constants after power−up for V_{INX} or V_{INADJ} to settle before sampling OUT_X. If we wait the typical 5τ, V_{INX} will be near 99.4% of $V_{INADJ} + V_{HYS}$ (or vice−versa.) Since the I_{NADJ} current will have a step change of 55% typical when changing from normal mode to diagnostic mode, we need to wait an additional $5\tau_{INADJ}$ after changing DIAG from low to high before again sampling OUT_X.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative