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Tips and Tricks to Build Efficient Circuits with NCP1200

Prepared by: Christophe Basso
ON Semiconductor
14, rue Paul Mesplé – BP1112 – 31035 TOULOUSE Cedex 1, France
33 (0)5 34 61 11 54
e–mail: christophe.basso@onsemi.com

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APPLICATION NOTE

Introduction

The NCP1200 easily lends itself to designing Switch–Mode Power Supplies (SMPS) in a snap–shot and its success speaks for itself. However, customers applications (and problems) are unique and often necessitate the addition of specific component arrangements around the IC. As usual, solving one particular design constraint brings another one with it, perhaps puzzling the designer even more. This application note answers typical questions that a designer can raise when starting his own system analysis, but also tries to answer some problems common to Switch–Mode Power Supply applications.

The following topics are covered in this document:

- Adding an External Latching Circuit for Over Voltage Protection or Over Temperature Shutdown
- Driving Big Gate–charge MOSFET
- Reducing the Standby Power with an Auxiliary Winding that Disables the DSS Operation
- Using Auxiliary Winding Without Affecting the OCP Trip Point, but Disabling the DSS
- Using Auxiliary Winding Without Affecting the OCP Trip Point and Keeping the DSS Working
- Inserting a Resistor with Pin 8 to Avoid Over–dissipation of the Package
- ’When I Insert a Resistor in the Gate of My MOSFET, the Supply Becomes Instable”
- “What MOSFET Size can I Drive in Half–wave Configuration?”
- “I Have Routed my 1200 with a Large Copper Area Around the Package. What Power can I Dissipate?”
- “What Power Level can I Expect from the NCP1200?”
- A Low–cost Open Loop Offline Converter
- Brown–out Protection
- Reducing the Burst in Overload Mode
- A Primary Regulated Converter for TV Sets
- Improving Short–circuit Protection with an Auxiliary Winding

Adding an External Latching Circuit for Over Voltage Protection or Over Temperature Shutdown

When pulling NCP1200’s feedback pin below the skip cycle level (pin1 voltage), output oscillations cease. If this action is accomplished through a thyristor, permanent latch–off occurs until the user cycles the V_{CC} down and up again by unplugging the power supply. By firing the thyristor via a zener diode connected to an auxiliary winding, an efficient Over Voltage Protection (OVP) circuit can be implemented. Figure 1 depicts the solution.

At rest, when the SMPS is properly working, Q1 and Q2 are transparent to the operations because the 10 kΩ resistors block them. As soon as the auxiliary winding level exceeds the zener voltage and fires Q2, the whole SCR turns on and via the 1N4148, pulls FB low. As a result, it immediately stops the 1200 driving pulses: the SMPS shuts off. However, the Dynamic Self–Supply (DSS) being still alive (V_{CC} ramps up and down between 10–12 V), the 47 kΩ resistor keeps the SCR latched despite the disappearance of the default. Once the user cycles V_{CC} down and up again (e.g. by unplugging the power supply from the mains outlet), the SCR de–biases and allows the 1200 to restart. Q1/Q2 could be ON Semiconductor dual combo bipolar MMBT3946DW. If for transformer noise reasons Vpin1 is much lower than its default value (1.4 V), a BAT54 must be wired in place of the 1N4148 to ensure that FB passes well below Vpin1: $Q2\_Vce_{sat} + V_f < Vpin1$. Increasing the value of the 47 k will change the total latch–off behavior into auto–recovery mode, as the default over current protection does.

A temperature shutdown can be realized on top of the above SCR by adding a PNP, as portrayed by Figure 2. The Negative Temperature Coefficient sensor (NTC) is selected to pull the PNP’s base toward ground at the wanted shutdown level. To obtain slightly more dynamic on the base level, a simple diode is inserted in series with the emitter. A more economic solution involves a single thermistor, also shown on the same picture.

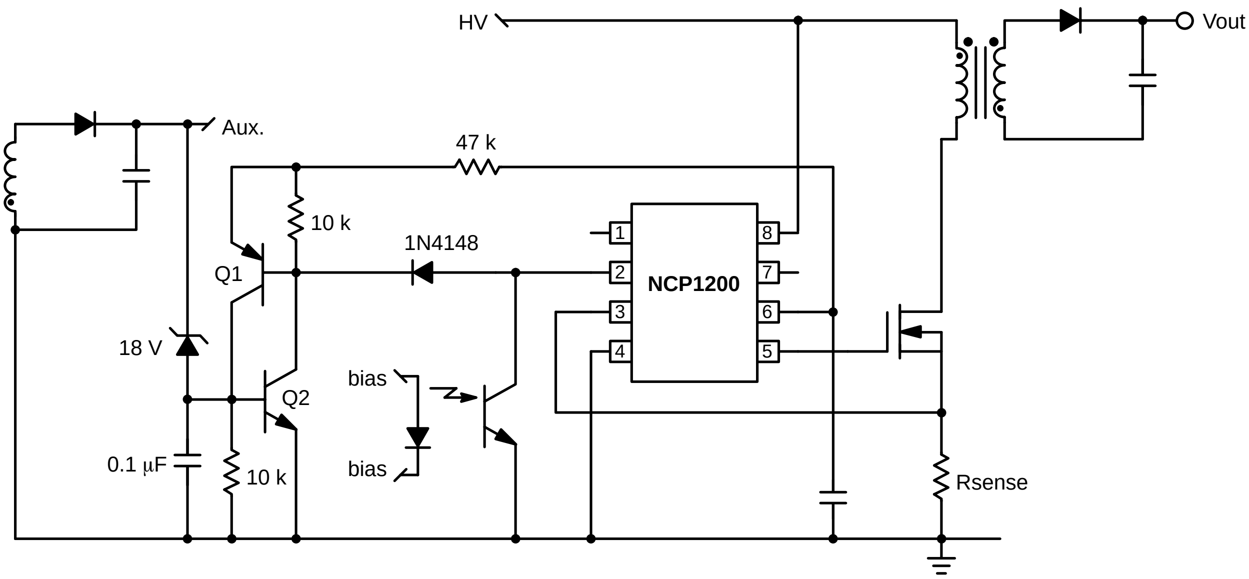

Figure 1. A Dual–Transistor Arrangement Latches–Off the NCP1200 in Case of an OVP Event

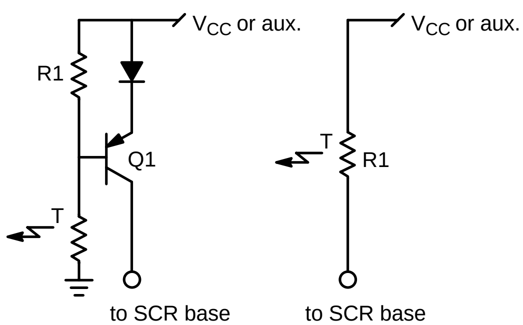

Figure 2. A NTC and a Simple PNP Make an Easy–to–Build Thermal Sensor Which Fires the SCR

Driving Big Gate–Charge MOSFETs

What actually limits the NCP1200 drive capability is the DSS and not its driver stage. The driver output connects a 40 Ω resistor between V_{CC} and gate (see 1200 data sheet) during the ON state whereas a 12 Ω is connected in the discharge path (OFF time). If the MOSFET exhibits a large total gate charge Qg, turn–on and turn–off times will be longer but it will properly work, probably generating high switching losses. Problems usually arise because those big MOSFETs heavily load the DSS and it is important to assess the total current consumption in worse conditions. This total consumption can be evaluated through the following formula: $I_{total} = I_{CC1} + Fswitching_{max} \times Qg_{max}$. Suppose that we use a 3 A MOSFET affected by a 25 nC Qg, then the total average current that the DSS must deliver is: 750 μA + 72 k x 25 n = 2.5 mA, if you would select a P60 version. The DSS current is 4 mA @ $T_j = 25°C$. However, when supplied by the high–voltage rail, the junction temperature will quickly rise, lowering the DSS capability to its minimum value stated in the data–sheet. This value being 2.8 mA @ $T_j = 125°C$, care must be taken that T_j stays lower than this number to ensure adequate safety margin.

Needless to say that the DIP8 option offering much better thermal specs compared to SO–8, it will be preferred in high Qg applications. A good news is that the internal NCP1200 consumption significantly reduces with temperature (see characterization curves in the data sheet) and consequently eases the DSS.

Now suppose that you would like to drive big MOSFETs, featuring large Qg e.g. 60 nC or even 100 nC. It becomes impossible to use the DSS. Should you try, you would observe a V_{CC} that immediately collapses below 10 V after turn–on: all the current the DSS delivers is eaten by the MOSFET driving. Even if this poor situation would work, you would not be able to sense a short–circuit anymore because the function is activated only if the V_{CC} goes up and down, e.g. between V_{CCOFF} and V_{CCON}. As a result, using an auxiliary winding becomes the only solution. However, we will see below that the aux. winding can degrade the Over Current Protection (OCP) trip point. Figure 3 offers an interesting intermediate solution where the aux. winding plays an important role but does not bother the DSS operation, keeping the precise OCP trip point intact.

In this example, Q1 buffers the drive output and the energy necessary to drive the big MOSFET is derived from the auxiliary winding. At power–on, the DSS charges both capacitors, Caux and CV_{CC} which are isolated by D1 as soon as the auxiliary voltage has built up above the NCP1200 V_{CCON} level. The drive current passes through Q1 and the 1200 delivers a small current to bias its base. At the opposite, D3 routes the gate current inside the 1200 as usual. A resistance can be inserted between the emitter and the gate to slow–down the turn–on transition. The no–load standby performance is better than without auxiliary winding because the only current seen by the DSS is roughly I_{CC1} which is low. Figure 3 clearly allows the NCP1200 to build SMPS of any output power levels, Flyback or Forward.

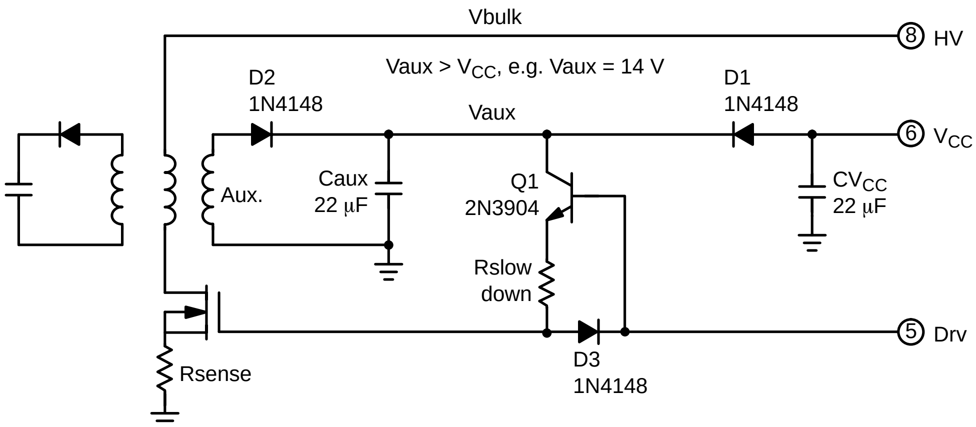

Figure 3. By Taking the Energy from the Auxiliary Winding Only at Turn–On, DSS Operation Is Not Bothered and IC Consumption Is Kept Within Safe Limits

Reducing the Standby Power with an Auxiliary Winding that Disables the DSS Operation

In certain applications, a low standby power is mandatory. This option clearly prevents from using the DSS because the 1200 supply would be the most consuming portion of the SMPS in no–load conditions. To stop the DSS, an external voltage must force the 1200 V_{CC} to be permanently above V_{CCON} or 11 V as given in the data sheet. Failure to reach that level would imply a DSS re–activation with all the losses in standby. Wiring the auxiliary winding with skip–cycle components can be a little tricky, especially if you target an extremely low standby power. Why? Because in standby, the pulses are not a continuous flow but a short burst whose recurrence can be as low as several tens of milli–seconds (skip cycle technique). Provided your auxiliary circuit exhibits some losses, you will not be able to maintain a self–supply above 11 V, re–activating the DSS again. Another problem takes place: the primary to secondary leakage inductance. This inductance generates a spike detected by the auxiliary diode which artificially raises the auxiliary voltage (Figure 4 with arbitrary levels). This effect can accidentally destroy the 1200 but also deteriorate the OCP detection point.

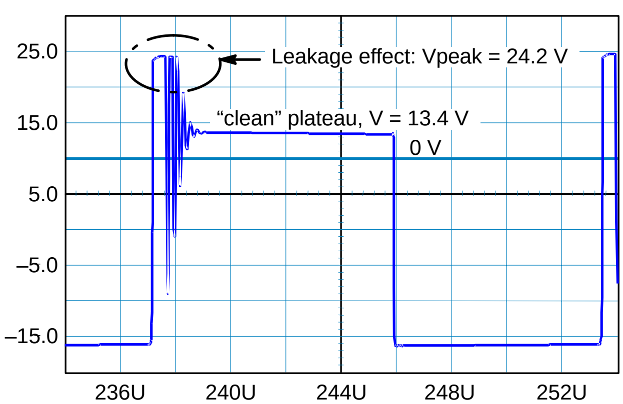

Figure 4. The Leakage Effect Seen on the Auxiliary Side Pulls–Up the Final Level Peak–Rectified by the Diode

As the NCP1200 V_{CC} cannot exceed 16 V, care must be taken at the design stage to limit the voltage excursion while running nominal load. A good solution would be to first integrate the leakage spike and then rectify the wave with a diode as Figure 5 suggests. Unfortunately, in standby, the auxiliary level would collapse because the burst energy is so low that the 22 Ω would dramatically limit the 22 µF re–fuelling current. We will exploit this feature in a later application.

The solution consists in splitting the rectifying section in two blocks, the second one clamping V_{CC} below 16 V. This solution is depicted by Figure 6. The BAT54 is only here to avoid hampering the startup time by charging two capacitors together. If this is not a problem, you can simply omit it. The zener voltage can be lowered but the maximum V_{CCOFF} (12.5 V) must be reached otherwise the 1200 won’t startup.

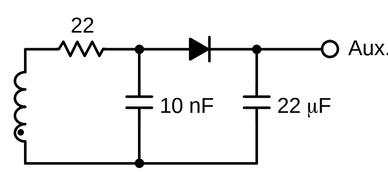

Figure 5. A Resistor and a Capacitor Can Integrate the Perfidious Leakage Inductance

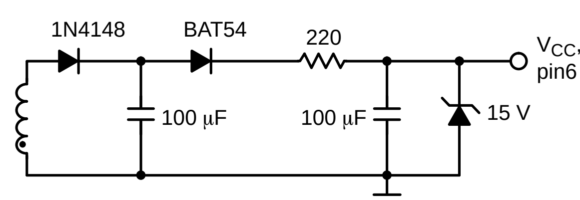

Figure 6. This Configuration Ensures Self–Supply in Standby and Prevents V_{CC} from Exceeding the 16 V Maximum Rating

Using an auxiliary winding as wired according to Figure 6 offers true short–circuit protection but the precise over load mode detection brought by the DSS is lost. This is imputed to the primary leakage inductance, which in some cases is so energetic, that a short on the secondary power winding cannot drop the auxiliary winding, preventing short–circuit detection. Reducing the primary clamp level (via the RCD network) represents a good solution, but to the detriment of the efficiency. If this is a problem in your application, below are other solutions keeping all the 1200 goodies with an auxiliary winding.

A 70 W demo board was built using an auxiliary supply and revealed less than 100 mW standby power at 350 VDC input level.

Using Auxiliary Winding Without Affecting the OCP Trip Point, but Disabling the DSS

One great aspect of the DSS, is the fact that the OCP circuitry is activated whatever the auxiliary voltage is, because it does not use any! In low standby power applications, you will need to wire an auxiliary winding to permanently disconnect the DSS. Unfortunately, the 1200 internal OCP circuitry activates when V_{CC} crosses V_{CCON} ($\approx$ 10 V) while going down. This action naturally takes place with the DSS, but if you wire an auxiliary winding, it just disappears because you managed to keep Vaux above 10 V to invalidate the DSS. As a result, if you overload the output, NCP1200 will activate its burst only when the auxiliary V_{CC} collapses below 10 V. And what happens if you have a poor coupling between the windings and a large primary leakage inductance (see Figure 4)? You never detect the OCP.

We have seen that the leakage inductance generates an energetic spike that couples to the auxiliary winding. Why not sampling the auxiliary voltage on the plateau, a short time further to the leakage appearance? This is exactly what Figure 7 circuit does for you.

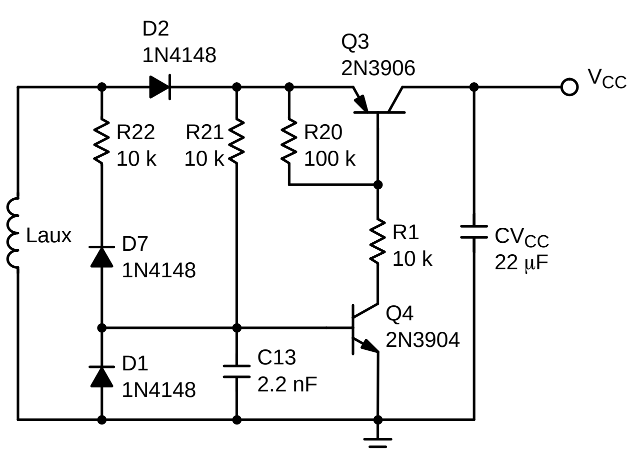

Figure 7. The Delay Introduced by Q4 Samples Right After the Leakage and You Obtain a Nice DC Voltage

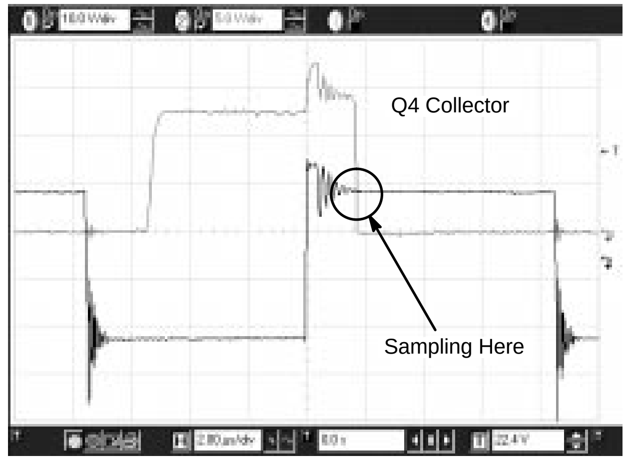

Figure 8. By Delaying the Sampling Time,You Obtain a Clean Auxiliary Level Without Any Leakage Effect

When the main power switch is ON, capacitor C13 is discharged through R22 and D7 whereas D1 avoids a deep reverse bias of Q4 base–emitter junction. When the main switch opens, the secondary voltage sharply rises and node 1 becomes positive. However, C13 being discharged, Q3 stays open and V_{CC} does not grow up. After a short period of time (adjustable through R21 or C13), Q4 closes and brings Q3's base closer to ground. V_{CC} now goes up and catches up node 2 level, minus Q3's V_{ce} sat. If the time delay is correctly selected, V_{CC} is absolutely clean from any voltage spike because you have sampled the plateau.

Figure 8 details the scope shot obtained using this circuit. As you can see, the sampling time occurs right after the leakage and the auxiliary level extracted from this plateau is clean. This solution can also be very useful in application where precise primary regulation is needed.

With this solution, the off–time is truncated to avoid the leakage effect. In standby, when skip cycle takes over, this off–time is considerably reduced and our delay circuit loses quite a bit of precious energy: the auxiliary winding collapses and cannot self–supply anymore the 1200. To combine the advantages of a clean self–supply (remember, to get a precise overcurrent trip point or a good primary regulation level if any) together with excellent standby power performance, Figure 9 offers an interesting solution. The schematic becomes more complicated but has been tested fine.

Q1 and Q2 perform their duty as described above but when voltage is present over C2, Q3 is biased and keeps D8's anode low enough to block it. When the supply enters standby, C2's level goes low and unleashes Q3 which can now let the current flow through D8, keeping 1200 self–supplied in standby. As soon as the load comes back, Q3 closes again and C2 recovers its role.

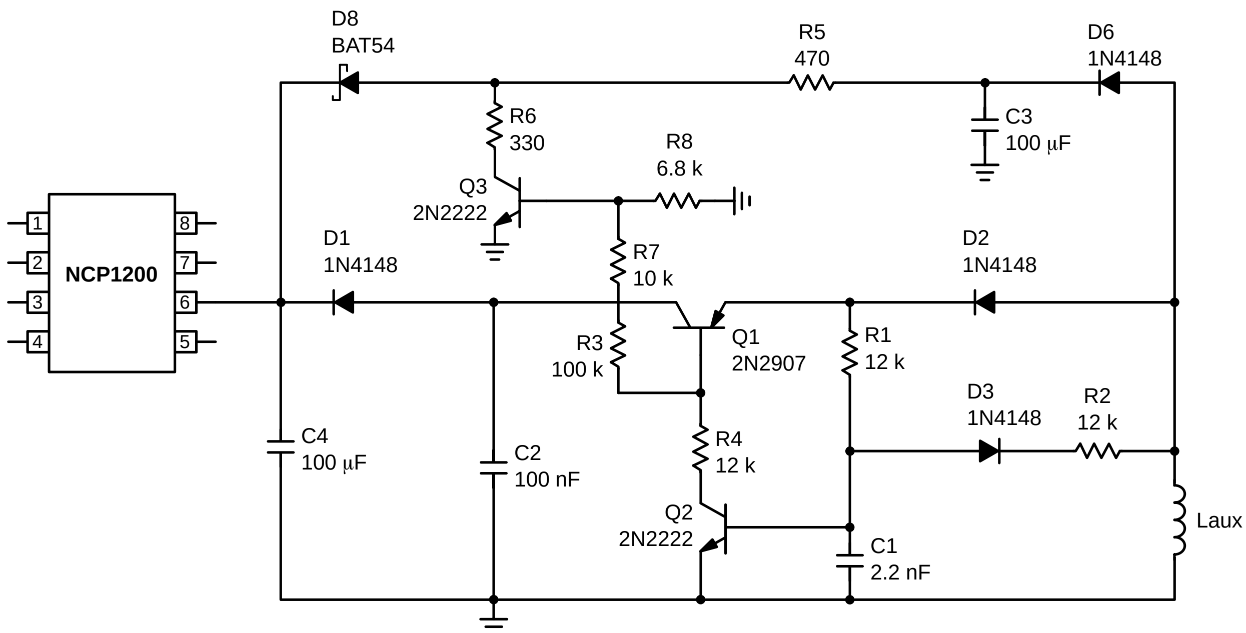

Figure 9. A Shunt Prevents the Auxiliary Level to Supply the 1200 in Normal Operation But Becomes Active in Standby

Using Auxiliary Winding Without Affecting the OCP Trip Point and Keeping the DSS Working

The DSS offers a very interesting feature which is the ability to implement true overload detection. Standard UC384X–based systems are usually built with an auxiliary winding but because of the poor cross–regulation between the windings, it is almost impossible to implement a precise over load protection. However, these systems can usually cope with short–circuit constraints because the auxiliary winding finally collapses when V_{out} equals zero. (See Figure 4 to see who is guilty.) As such, the DSS is a very desirable choice when true over load protection is required by the customer. Unfortunately, in no–load conditions, the DSS being connected to the high–voltage rail, you directly measure this power consumption on the input, despite the low current consumption of the 1200. In some very stringent standby power requirements, you simply cannot accept these losses. Figure 10 presents a solution built on top of that presented in Figure 3.

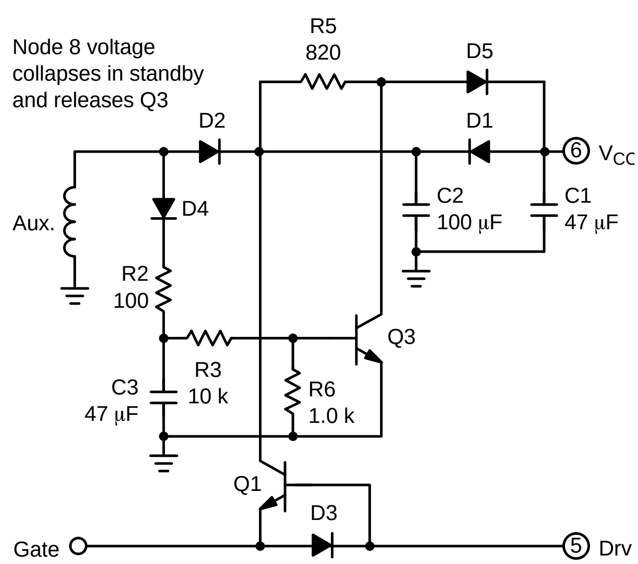

Figure 10. This Solution Upgrades Figure 3 Option by Disabling the DSS in Standby

The trick used to detect the standby or no–load condition, is to take benefit from the the weak energetic content of the burst pulses when the supply operates in standby. That is to say, if the refueling current circulating through D4 is diminished by a resistor (R2), then C3 will never be able to maintain a normal operating voltage (e.g. as the one at nominal load) and it we be severely reduced. In the example, we measured 15 V in normal load, and less than 3 V in standby. In normal operation, C3's voltage is high enough to forward bias Q3 via R3/R6. His collector pulling R5 terminal to ground, D5 is naturally blocked and the DSS plays its role: precise over load mode detection, and EMI jittering through its ripple. When the SMPS goes to standby, C3's level decreases until Q3 gets un–biased. Its collector no longer pulls R5 to the ground and D5 can pass all the auxiliary level developed across C2 to block the DSS. R5 value can be adjusted to avoid too much of wasted power as long as D5 stays blocked in nominal load operations. The standby power becomes as good as stated before: less than 100 mW at high line.

Thanks to this latest solution, you can:

- Drive the MOSFET of your choice: all the ON current is drawn from the auxiliary winding.
- Benefit from the DSS activity to build a precise over current detection and use its ripple for EMI jittering.
- Disable the DSS in no–load conditions and obtain one of the best standby power on the market.

Inserting a Resistor with Pin8 to Avoid Over–Dissipation of the Package

Some users like to use the SO–8 package mainly because of its small size. Unfortunately, the thermal resistance junction–to–ambient makes the exercise difficult because the DSS naturally dissipates heat (except if use some alternative solution as depicted below). The auxiliary winding option is still possible, but the best Over Current Protection (OCP) trip point is obtained with the DSS. The DSS being active, there is no other alternative than dissipating this heat through copper, or, move it to another component, e.g. a series resistor. By inserting a resistive element in series with pin8, every time the DSS turns on, you drop some voltage across the resistor (Figure 11) . You thus spread the total power between two components instead of one, lowering NCP1200 Tj inside the SO–8 package. The calculation is easy. You know by the data sheet that every time the DSS turns on, 4 mA flow inside pin8 at steady–state. If one keeps about 50 V minimum on pin8 to properly operate the DSS, the resistor value can be calculated through:

$$\text{Rdrop} \le \frac{\text{Vbulk min} - 50}{4\text{ m}}$$

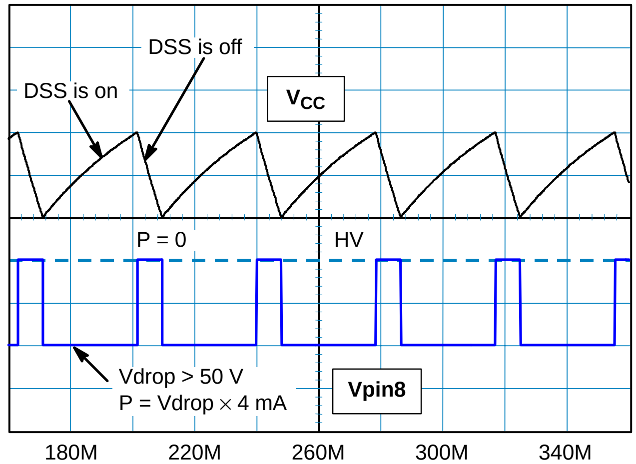

Figure 11. By Inserting a Resistor with Pin8, You Can Split the Power Between an Active and a Passive Component in Order to Keep Tj Lower

Below are two examples showing the benefits of inserting the resistor.

Case 1:

Single mains, 230 VAC ± 15%, NCP1200 average consumption is around 2.5 mA. DSS duty–cycle is 62%. V_{bulk} max = 374 V_{DC} and V_{bulk} min = 276 V_{DC}. Rseries = (276 – 50)/4 m = 56 kΩ.

1. Without the resistor, NCP1200 would dissipate (worse case): 374 x 2.5 m = 935 mW, incompatible with the SO–8. With an RtetaJA of 100°C/W, the maximum power the NCP1200D version can handle at an ambient of 40°C is: 125°C – 40°C/100 = 850 mW
2. By inserting the 56 kΩ resistor, we drop 56 k x 4 m = 224 V during the DSS activation. The power dissipated by the NCP1200 is therefore: Pinstant x DSS duty–cycle = (374 – 224) x 4 m x 0.62 = 372 mW. We can pass the limit and the resistor will dissipate 935 – 372 = 563 mW.

Case 2:

Universal mains, 90 – 27 5VAC, NCP1200 average consumption is around 2.5 mA. DSS duty–cycle is 62%. Vbulk max = 388 VDC and Vbulk min = 127 VDC. Rseries = (127 – 50)/4m = 19 kΩ.

1. Without the resistor, NCP1200 would dissipate (worse case): 388 x 2.5 m = 970 mW, incompatible with the SO–8.
2. By inserting the 19 kΩ resistor, we drop 19 k x 4 m = 76 V during the DSS activation. The power dissipated by the NCP1200 is therefore: Pinstant x DSS duty–cycle = (388 – 76) x 4 m x 0.62 = 773 mW. We can pass the limit and the resistor will dissipate 970 – 773 = 197 mW.

"When I Insert a Resistor in the Gate of My MOSFET, the Supply Becomes Instable"

The Leading Edge Blanking (LEB) circuitry has the role to clean the voltage appearing across the sense resistor. By discharging all the parasitic capacitors at turn–on, you create a current spike that can engender false tripping of the current comparator. To avoid this problem, NCP1200 includes a LEB calibrated at 250 ns. The LEB starts to blank the current sense information as soon as the driver goes high. Figure 12 displays the drive and gate signals when a resistor inserted between gate and driver is small. This represents a normal operating conditions where the gate follows the driver. However, inserting a larger resistor in series with the gate is a common practice when one wants to slow down the main switch, e.g. for EMI reasons. Unfortunately, the resistor delays the turn–on of the MOSFET and truncates the Leading Edge Blanking (LEB) which no longer plays its role (Figure 13). In that case, false triggers occur and instabilities takes place. The cure consists in adding an RC network between Rsense and the current sense pin (Figure 14).

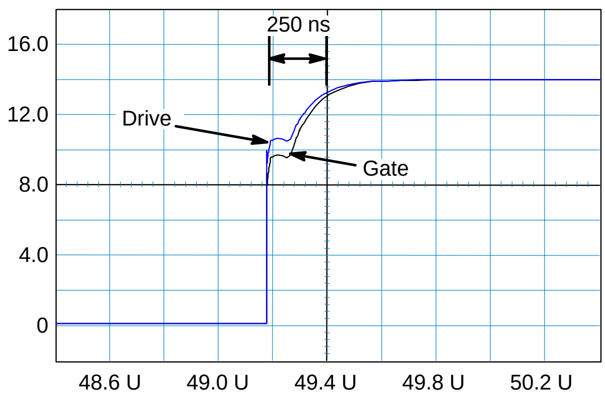

Figure 12. When the Gate Follows the Drive, the LEB Works Fine

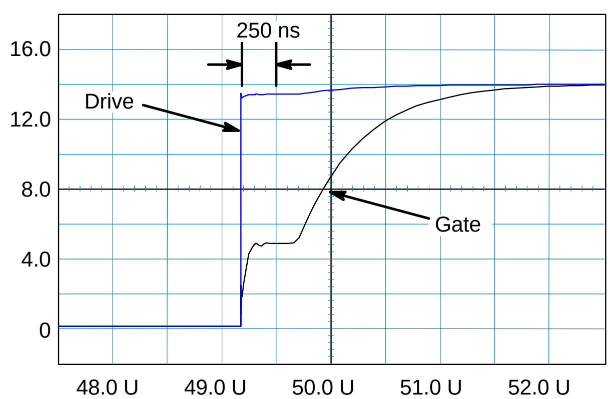

Figure 13. Delaying the Gate–Source Signal Produces the Effect of Truncating the LEB

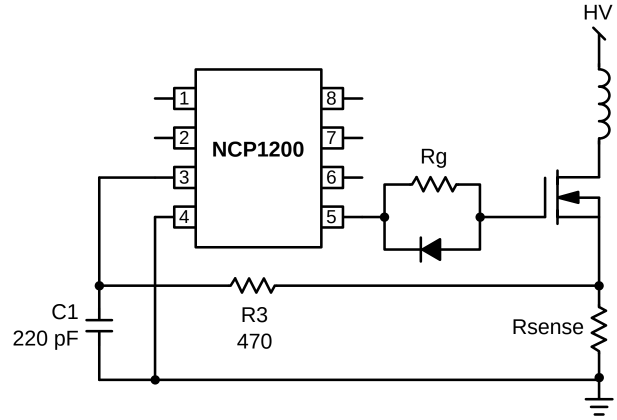

Figure 14. This Network Re–Enforces the LEB Action by Integrating the Sense Signal Whatever the Gate Delay

"What MOSFET's Size Can I Drive in Half–Wave Configuration?"

In some of the available application notes, we propose to wire pin8 not to the bulk capacitor but to the rectifying half–wave. This solution is acceptable for low gate–charge MOSFETs only, because the DSS current capability is divided by two in average (half–wave duty–cycle is around 50%). As a result, the DSS can only deliver 2 mA DC which divides between the controller (I_{CC1}) and the driver consumption, utilized to charge up the MOSFET's Qg. If we take the very worse case that appears at high temperature, the DSS minimum current is 2.8 mA which divided by two makes 1.4 mA. Removing I_{CC1} ($\approx$750 µA, this number goes down when T_j goes up), we have 650 µA with 100 µA left to charge the V_{CC} capacitor. As a result, with a 60 kHz version, the maximum Qg would be: 550 µA/60 k = 9 nC. This corresponds to a 1 A MOSFET or a 2 A MOSFET featuring low gate charge only. If you wire a bigger MOSFET, V_{CC} will collapse without the classical ripple 2 V due to the DSS operation. No ripple means no OCP because the 10 V error flag test has gone. (See application note AND8023/D for more detailed explanation.) In summary, we recommend half–wave operation only in configurations that guarantee proper DSS operation at any temperature.

"I Have Routed My 1200 with a Large Copper Area Around the Package. What Power Can I Dissipate?"

The maximum power accepted by the NCP1200 is given by:

$$Pmax = \frac{Tj\,max - Tamb\,max}{R\theta J - A} \qquad \text{(eq. 1)}$$

As you can see, you could define yourself two parameters in the formula: Tj*max* given by the data sheet, or the maximum operating temperature your Quality Department fixes, and finally Tamb*max*, given by your application. Unfortunately, you cannot determine $R_{\theta JA}$ because the copper area you added has actually changed it from the original data sheet specification. The best is to measure it with a simple method that has proven to be accurate enough for our purposes. First, you need a bare PCB featuring the copper area you have routed. It can be your final board without anything soldered on it. Then, you solder the NCP1200 (DIP8 or SO, depending on your selection) directly on the copper (please, without a socket). Once this is done, we need to find a Temperature Sensitive Parameter (TSP) to evaluate the junction temperature inside the package. One of the internal ESD zener diode represents a good choice. Before using it, we must calibrate it. Several solutions exist but the easiest one is to take a multi–meter in diode position offering sufficient resolution (3 or 4 digits are ok) and current stability during the measurement. The Agilent HP34401A can be a possible selection. The ESD diode connected to pin1 can be used but another one could also be wired, e.g. the current sense pin. Now, bias it in forward mode by connecting probe + to the ground and probe – to pin 1. At an ambient of 25°C, you should read something like $Vf \times \approx 720$ mV. The rest of the operation requires a precisely controlled heater to calibrate our junction. Put the NCP1200 under the heater's bell and measure the Vf at different points, e.g. every 10°C. At every step, wait at least a few minutes that the reading stabilizes before recording the point. If everything goes well, you should obtain a linear graph as Figure 15 shows.

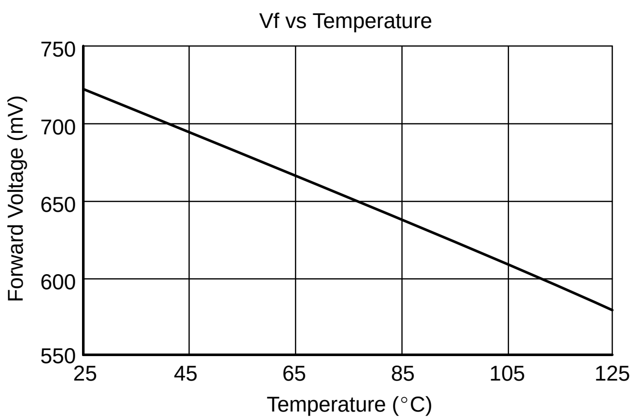

Figure 15. Collecting Data Points and Feeding a Spreadsheet Unveils the ESD Junction Temperature Behavior

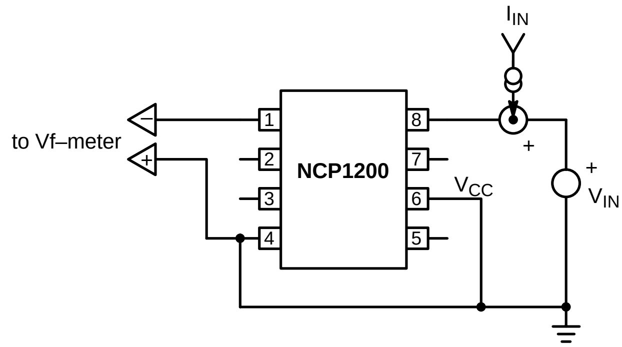

Figure 16. Next Step Is to Inject Power Into the Chip

With that graph on hand, we can now start measuring our $R_{\theta JA}$. On the same PCB board, make a short between V_{CC} and ground, leave all the other pin open but keep the Vf–meter connected. Do not bring too much of solder on the joints to be in same final industrial conditions (for instance wave soldering). Now, bring a DC source to pin8, normal polarity, that is to say, pin8 positive by respect to ground. Figure 16 shows the wiring diagram for best understanding where an ampere–meter has been inserted. Immerse all the 1200 PCB test fixture into an hermetic oven and select the ambient temperature at let's say 40°C. Turn the DC power supply on and start to increase the voltage. At a certain moment, the DSS turns on and the ampere–meter indicates a current. Increase the voltage until you reach a power value of 300 mW roughly ($V_{\_in}$ x I_in). Leave everything cooking for a while, until the V_f reading stabilizes. You will note that the current goes down a bit because of the DSS thermal effect (actually self–protective). After time has elapsed, suppose that you read V_f = 652 mV and Ptotal = 280 mW. From Figure 15, we extract the corresponding junction temperature given by our calibrated TSP: 652 mV $\rightarrow$ $T_j \times \approx 75$°C. From these numbers, we are able to calculate our thermal resistance junction–to–ambient resistor by:

$$R\theta J - A = \frac{Tj - Tamb}{Ptotal} \qquad \text{(eq. 2)}$$

which turns to be 125°C/W. A few remarks concerning the measure:

- Use a well temperature–controlled oven. Failure to stabilize the temperature in a quiet environment will engender large errors.
- Wait that the part has stopped its temperature excursion before taking the V_f point. DIP8 packages require longer time than SO–8.

"What Power Level Can I Expect from the NCP1200?"

The NCP1200 being a general purpose current–mode controller, you can virtually use it in any applications ranging from a few hundred of mW up to 100 W or more! The above design ideas will let you implement the solution best adapted to your application. The limiting factor is actually the power switch and the 1200 driving capability. In the simplest application schematic (no aux. winding) with the DSS working and a 3 A MOSFET featuring low gate charge, we have successfully built a 70 W universal mains application board exhibiting 81% efficiency at low line and 87% at high line. Associating an auxiliary winding and a single or dual bipolar stage (as described in the data sheet) will let you drive the MOSFET of your choice, e.g. a 10 A device, reducing the conduction losses and the heatsink size.

A Low–Cost Open Loop Offline Converter

In equipment requiring a stand–by mode, e.g. VCRs, TVs etc, you must still supply the microprocessor when everything is asleep in order to receive and interpret any wake–up signal from the remote control or from the broadcasting company. The power consumption of the system is rather low and classical Switch–Mode Power Supplies (SMPS) chips represent a clear overkill for a sub–1 W output levels. The active solution also needs to be cost effective compared to the standard structure using a metallic transformer. The idea behind the circuit is to get rid of the optocoupler which obviously impedes the total circuit cost.

Figure 17 schematic shows how the NCP1200 can simply drive an external 600 V MOSFET. The lack of auxiliary winding greatly simplifies the overall application circuitry: the V_{CC} is totally provided by the internal Dynamic Self Supply integrated in the controller.

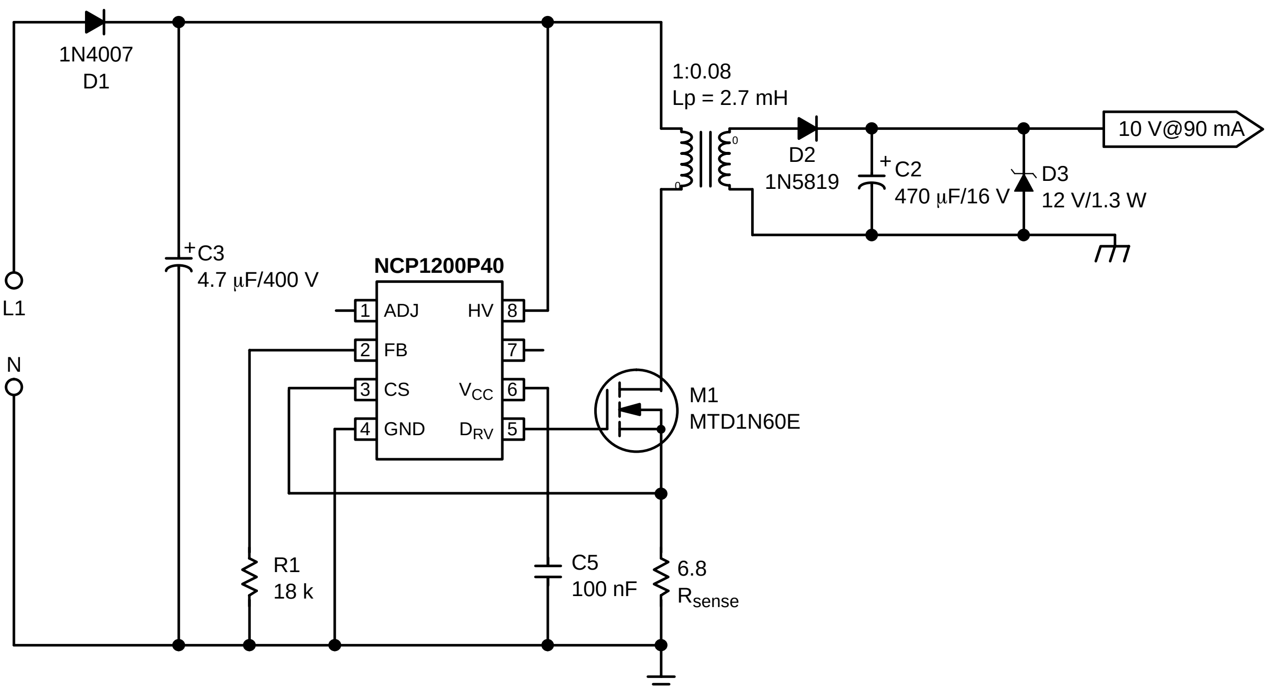

Figure 17. This Simplified Power Supply Delivers up to 1 W in Open–Loop

The peak current is regulated by the NCP1200 and allows operation over universal mains. Since the circuit operates at constant output power, the needed peak current can be extracted by the following formula:

$$I_p = \sqrt{\frac{2 \cdot P_{OUT}}{L_p \cdot F_{OSC}}} \quad \text{(eq. 3)}$$

With an internal error amplifier clipped at 1 V maximum, Rsense is evaluated using 1/Ipmax. In our example, a 40 kHz circuit combined with a 6.8 Ω sense element delivered up to 1 W continuous (Lp = 2.8 mH). You will recompute Rsense for lower or higher output power requirements. The 12 V output zener prevents from any overvoltage generation. R1 deactivates the internal short circuit protection which normally reacts upon feedback path loss.

Finally, thanks to its avalanche capability, the MTD1N60E does not require any clipping network and further eases the design. The transformer is available through different suppliers such as Eldor (Italy, eldor@eldor.it, ref. 2262.0058C) or Coilcraft (US, info@coilcraft.com, ref. Y8844–A). The efficiency was measured at 64% (low line, P_{out} = 866 mW) and 61% (high line, P_{out} = 1.08 W).

Brown–out Protection

Brown–out protection is a mean to prevent the SMPS operating from a low input voltage where conduction losses on the MOSFET could be lethal. There are different ways to stop the NCP120X operation, the easiest one being the FB pin pull–down to the ground. Figure 18 offers a simple circuit built with a couple of cheap bipolar devices implementing a Schmitt trigger circuit. The bulk voltage is sensed through R1 and R2 and Q4 starts to start conduction as soon as its base reaches the emitter voltage +0.7 V. The 3V9 zener diodes helps to: a) obtain a more precise level; b) decrease the temperature dependency contribution of the Vbe. The diode D2 introduces the necessary hysteresis. Please note that it might be necessary to reduce R6 around 1.5 kΩ with a NCP1200. This is because the internal collector resistor on a NCP1200 is 8 kΩ whereas it increases up to 20 kΩ on a NCP1200A (hence better standby performance). Therefore, a strong Q2/Q4 emitter resistor may be of too high value to drop Vpin2 below the skip level and efficiently stop the switching operation.

The switching levels can approximately be calculated via the following way:

Vin is growing up:

In that case, Q4 is blocked and Q2 is conducting, loading the NCP1200(A) feedback pin. As a result, the emitter of both transistors goes up to:

$$V(R6) = V_{openFB} \times \frac{R6}{R_{FB} + R6} \qquad \text{(eq. 4)}$$

where V_{openFB} is the open–loop pin2 level (4.8 V typical) and R_{FB} is the internal pull–up resistor, 8 kΩ for the NCP1200, 20 kΩ for the NCP1200A. To turn on Q4, one needs to generate a total base voltage of V_{be} + V(R6) which will be around 0.7 + 0.5 = 1.2 V for a NCP1200A. Considering the 3V9 zener diode in series, the total threshold voltage will be 3.9 + 1.2 = 5.1 V (Vth). With a divider made of R1 and R2, we create a division ratio of: R2/(R2 + R1) = 0.054, as a result, the turn–on voltage is simply: 5.1/0.054 = 94 V_{DC}.

To calculate the divider R1/R2 follow the steps:

1. first select a divider current, not too high to avoid degrading the standby power at high–line: 110 μA in our example.
2. then calculate the lower resistor R2 by: Vth/110 μ = 47 kΩ
3. suppose you would like to turn–on switching cycles at 94 V, then R1 is simply: (94 – Vth)/110 μ = 810 kΩ

Once triggered, Q2 is blocked and releases the feedback pin which now moves between 1.4 and 4.8 V.

Vin is decreasing:

Q4 being saturated, its emitter voltage V(R6) is now: [R6/(R6 + R7)] x V_{CC} = 0.260 V @ V_{CC} = 12 V. The new input threshold becomes 0.26 + 0.7 + 3.9 = 4.85 V. The divider ratio being 0.054, $V_{turn–off}$ = 4.85/0.054 = 89 V. D2 artificially increases this hysteresis and helps to shift the whole curve toward lower voltages. If the circuit offers the right levels without R3/D2, they simply can be omitted.

With Figure 18 circuit, we obtained a turn–on voltage of 100 V_{DC} with a turn–off bulk voltage of 80 V roughly. Please note that its obvious simplicity cannot compete against precise Brown–out circuits implementing comparators and reference voltages.

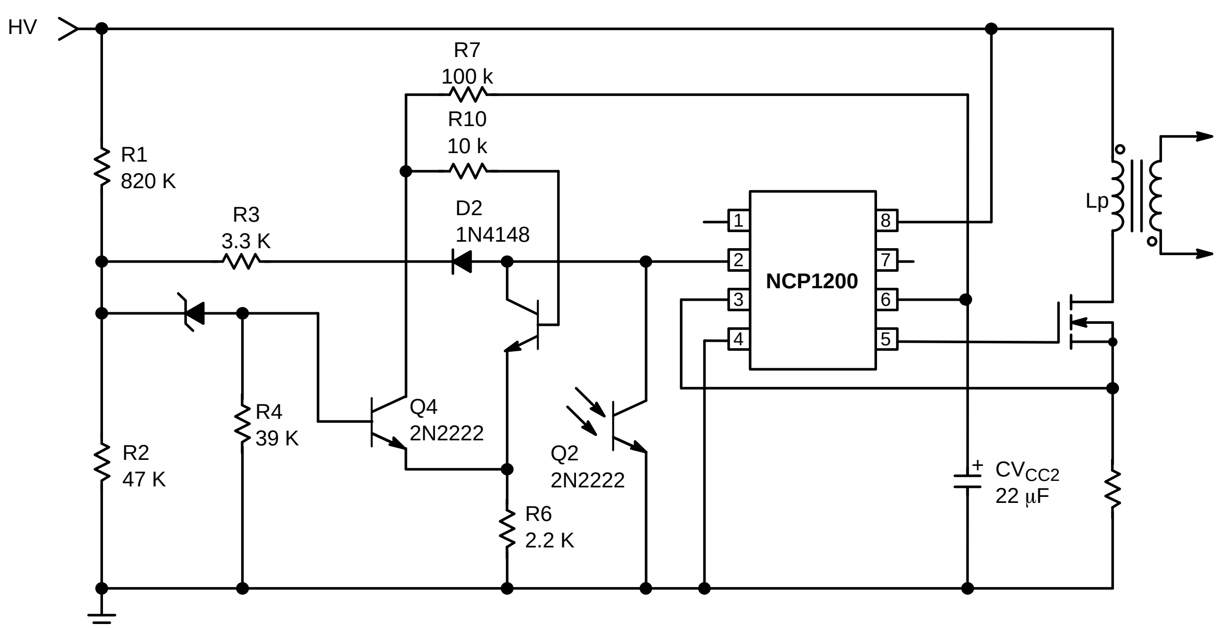

Figure 18. A Brown–out Circuilt Built with Two Transistors around the NCP1200A

Reducing the Burst in Overload Mode

Contributed by Eddie Suen, eddie.suen@onsemi.com

In some applications, it is desirable to reduce the average power delivered to the load when it presents a short–circuit. In the NCP1200 family, a built–in hiccup function reduces the power dissipation (and eliminate thermal issue) when the system is overloaded, short–circuited or even in presence of a broken optocoupler. The output current is thus fold back and it naturally reduces the stress to the output rectifier.

Figure 19 details the internal NCP1200 sources arrangement. When a short–circuit occurs, the V_{CC} waveform looks like what Figure 2 depicts: V_{CC} ramps up to 12 V, then switching takes place until I_{CC2} discharges the V_{CC} capacitor down to 10 V. Then switching stops and the latched–off phase is entered down to around 6.5 V where I_{CC1} drops to I_{CC3} = 350 µA (Figure 20):

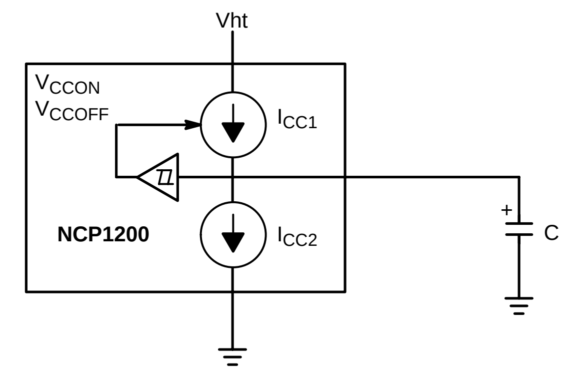

Figure 19. Internal NCP1200 SImplified Arrangement

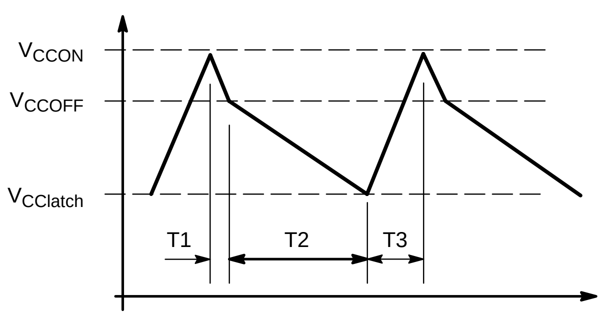

Figure 20. V_{CC} Waveform when the Optocoupler is Lost, e.g. During an Overload.

If:

I_{CC1} = 4 mA
I_{CC2} = 1.5 mA
I_{CC3} = 0.35 mA
V_{CCOFF} = 12 V
V_{CCON} = 10 V
$V_{CClatch}$ = 6.5 V

Using the equation C x V = I x T, we can compute each timing event:

$$T1 = \frac{C \times (V_{CCOFF} - V_{CCON})}{I_{CC2}} = \frac{22\mu F \times (12V - 10V)}{1.5mA} = 29ms$$

$$T2 = \frac{C \times (V_{CCON} - V_{CClatch})}{I_{CC}} = \frac{22\mu F \times (10V - 6.5V)}{0.35mA = 220ms}$$

$$T3 = \frac{C \times (V_{CCOFF} - V_{CClatch})}{(I_{CC1} - I_{CC3})} = \frac{22\mu F \times (12V - 6.5V)}{4mA - 0.35mA} = 33.2ms$$

Burst duty–cycle = T1/(T1 + T2 + T3) = 29 ms/(29 ms + 220 ms + 33.2 ms) = 10.3%

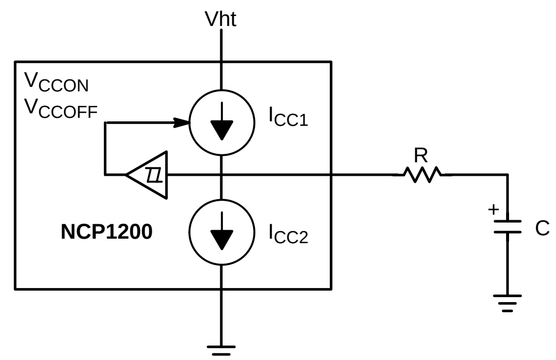

Figure 21. Inserting a Single Resistor in Series with the V_{CC} Capacitor Help Reducing the Burst Duty–Cycle

If we insert a 220 Ω resistor between NCP1200 V_{CC} and the capacitor (+) terminal as Figure 21 indicates, the NCP1200 V_{CC} pin waveform will behave like the blue line depicted by Figure 22 whereas the red line portrays the voltage evolution on the V_{CC} capacitor (+) terminal. The insertion of R creates an offset which helps dropping faster during the burst, without altering the latch–off phase as if a V_{CC} capacitor of smaller value was used.

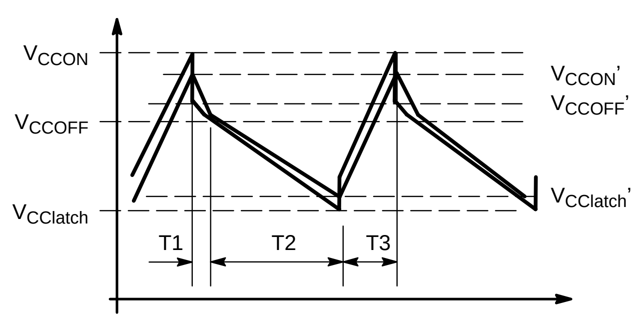

Figure 22. The Insertion of a Resistor Creates an Offset

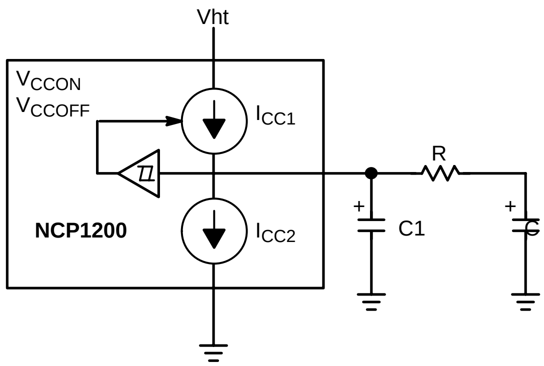

Figure 23. The Addition of C1 Ensures Safer Start–up Sequences

The red line will follow a new set of apparent V_{CCOFF}', V_{CCON}' and $V_{CClatch}$'. If we insert a 220 Ω resistor with our previous 22 µF capacitor, then we can compute the new burst duty–cycle:

$V_{CCOFF}' = V_{CCOFF} - R \times (I_{CC1} - I_{CC3})$
$= 12\text{ V} - 220\ \Omega \times (4\text{ mA} - 0.35\text{ mA}) = 11.2\text{ V}$
$V_{CCON}' = V_{CCON} + R \times I_{CC2}$
$= 10\text{ V} + 220\ \Omega \times 1.5\text{ mA} = 10.33\text{ V}$
$V_{CClatch}' = V_{CClatch} + R \times I_{CC3}$
$= 6.5\text{ V} + 220\ \Omega \times 0.35\text{ mA} = 6.58\text{ V}$

Then the new timing will be :

$T1' = (C \times (V_{CCOFF}' - V_{CCON}'))/I_{CC2}$
$= (22\ \mu\text{F} \times (11.2\text{ V} - 10.33\text{ V}))/1.5\text{ mA} = 12.76\text{ ms}$
$T2' = (C \times (V_{CCON}' - V_{CClatch}'))/I_{CC3}$
$= (22\ \mu\text{F} \times (10.33\text{ V} - 6.58\text{ V}))/0.35\text{ mA} = 236\text{ ms}$
$T3' = (C \times (V_{CCOFF}' - V_{CClatch}'))/(I_{CC1} - I_{CC3})$
$= (22\ \mu\text{F} \times (11.2\text{ V} - 6.58\text{ V}))/(4\text{ mA} - 0.35\text{ mA})$
$= 27.8\text{ ms}$

New Duty cycle will be: T1'/(T1' + T2' + T3') = 12.76 ms/(12.76 ms + 236 ms + 27.8 ms) = 4.6%

Further increasing R, drastically reduces the burst duty–cycle. Finally, when V_{CCOFF}' is approaching V_{CCON}', duty–cycle will be close to zero. On one hand, we will significantly improve the hiccup performance but to the detriment of possible erratic behavior... So, to improve the start–up sequence, we recommend to add a small capacitor C1 (1 µF), placed directly across V_{CC} pin and ground as Figure 19 shows. This significantly improves the startup sequence while filtering spikes and glitches.

Please note that since the delta between V_{CCON}' and V_{CCOFF}' is reduced, V_{CC} waveform in normal DSS operation will have lower amplitude but higher frequency. Also, designer may need to increase the capacitance of the V_{CC} capacitor, and ensure T1' is longer than the rise up time of output voltages. So as to avoid a false over–current to occur during power up.

Primary Regulated Converters

Despite its absence of internal error amplifier, the NCP1200 can easily be implemented in a primary regulated power supply. A typical example is a TV set converter delivering 80 W from a 230 VAC ± 15% network. In this application, the auxiliary winding is used to reflect the output voltage only, whereas the self–supply of the controller is ensured by its DSS. This brings several advantages such as: a) an excellent overload/short–circuit protection independent of any badly coupled auxiliary winding; b) the ability to easily implement secondary reconfiguration without caring of the primary section self–supply; c) a strong auxiliary winding filter can be placed to improve the load regulation without affecting the self–supply of the controller since the DSS does it already. Figure 24 shows the implemented schematic used to build the converter. In lack of error amplifier, a 12 V zener diode and a small NPN transistor permanently monitor the auxiliary winding. This DC level is obtained further to a filtering action from L1 and C1, which efficiently remove any spurious pulses induced by the primary leakage inductance (see Figure 4). The 40 kHz switching operation eases the EMI filtering while reducing the switching losses on the MOSFET. Csnubb slows down $V_{ds(t)}$ and contributes to lowering the video noise. The short–circuit protection is present and offers a true overload protection independent of the auxiliary level. Despite its simplicity, Figure 25 and 26 give a good idea of the converter performance in load regulation and step response.

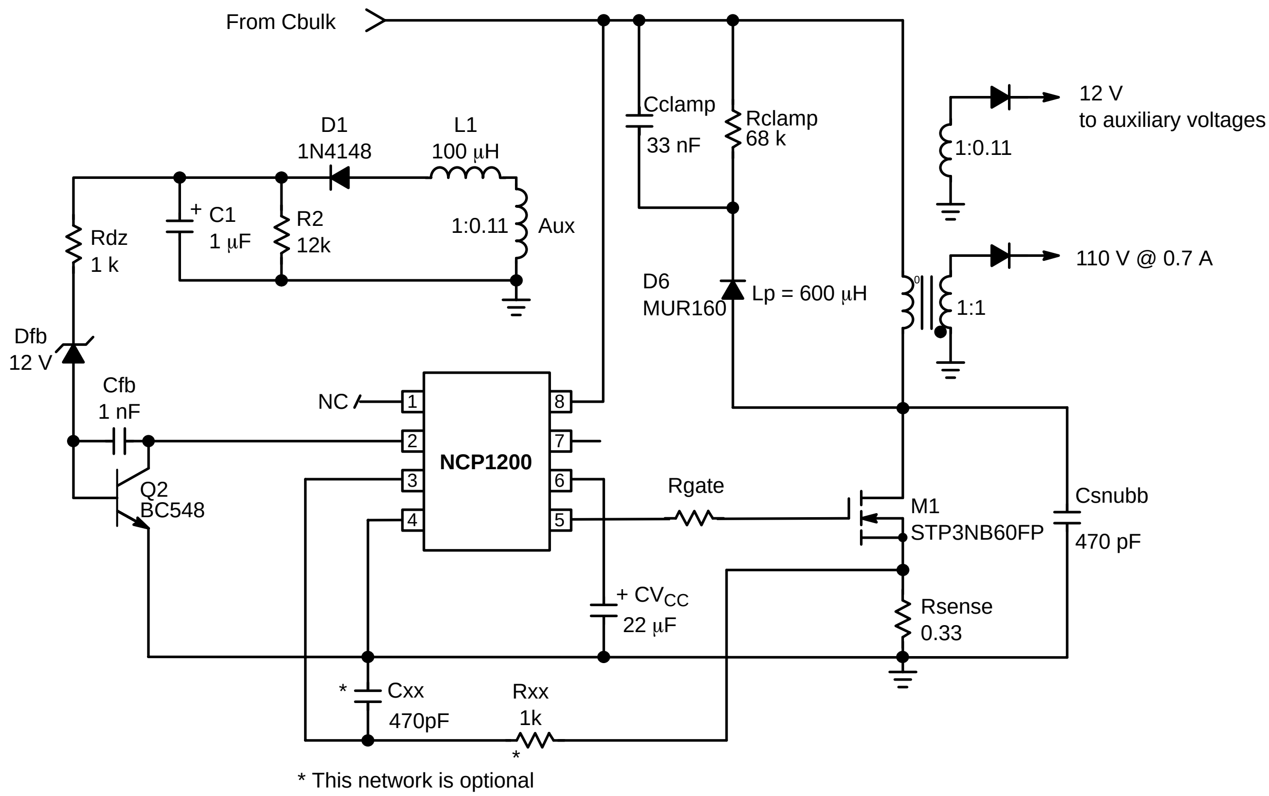

Figure 24. A Simple Transistor Associated with a Zener Diode Offers Good Regulating Results

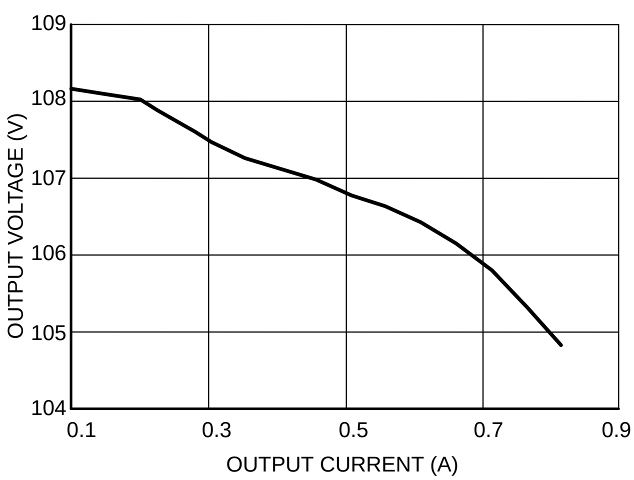

Figure 25. Static Load Response at 325 VDC Input

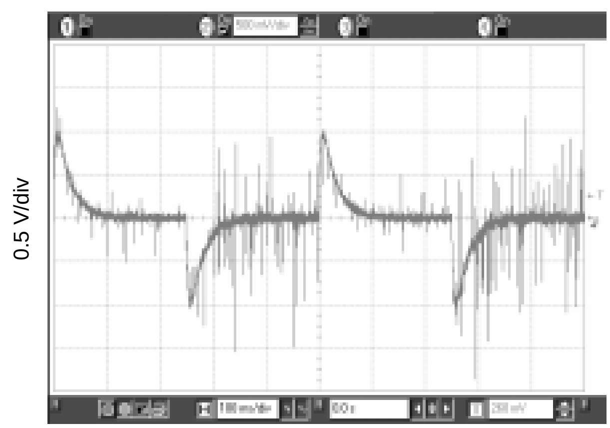

Figure 26. Dynamic Step Load Response, Same 325 VC

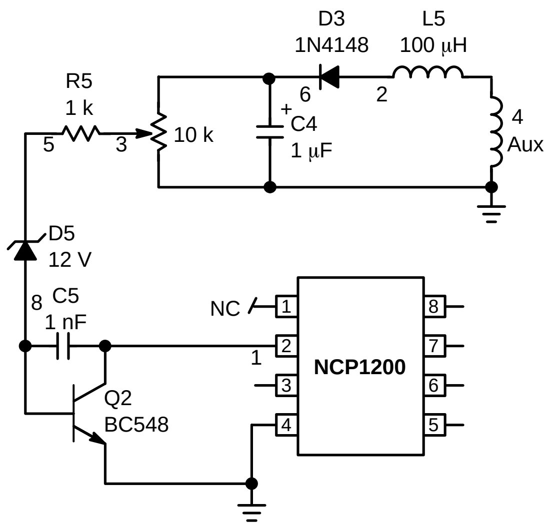

Figure 27. A Simple Pot–Meter Offers an Easy Mean to Adjust the Output Voltage

The output voltage can be adjusted by either changing: a) the turn–ratios between the auxiliary winding and the secondary power windings; b) the zener breakdown voltage; c) inserting a potentiometer as indicated by Figure 27.

Improving Short–Circuit Protection with an Auxiliary Winding

In many applications, the NCP1200'DSS is disabled to implement a classical self–supply through the auxiliary winding. However, a precise short–circuit protection trip point becomes difficult to implement since the auxiliary V_{CC} must: a) collapse to start the burst operation in presence of an overload; b) be kept high enough in standby (where the skip frequency can be very low) to self–power the controller and not authorize the DSS activation.

As Figure 4 has shown, the primary leakage inductance strongly degrades the auxiliary V_{CC}. This situation can sometimes be so bad that the V_{CC} does not collapse at all in presence of a true output short–circuit. Figure 5 offers a possible solution but experience shows that the diode series resistance of 22 Ω heavily limits the refueling peak current in standby (remember, the bunch frequency can be extremely low, tens of milliseconds, especially when you target around 100 mW of input power) and the self–supply collapses, despite a bigger V_{CC} capacitor.

Figure 28 offers a possible solution where a damped LC network is installed after the auxiliary connection. The inductor series resistance shall be low enough to avoid introducing further ohmic losses (which limit the peak current in the V_{CC} capacitor). The damping elements 1.5 kΩ/10 nF prevent any peaking once the inductor is installed which could easily exceed the controller breakdown voltage. Thanks to the implemented values, the dissipation is low at high line.

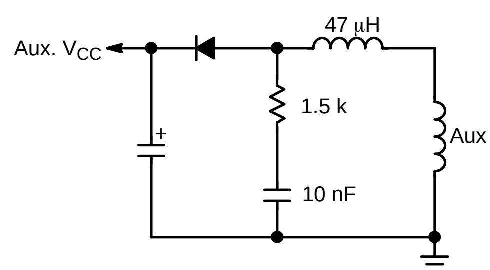

Figure 28. A Simple LC Network Helps to Filter Out the Primary Leakage Spike Without Disturbing the Self–Supply in Standby

For more information on this device, please visit our website at: www.onsemi.com/pub/ncp1200

Notes

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