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AND8045/D

Enhanced V^2™ Multiphase SMPS for Microprocessors

ON Semiconductor™

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APPLICATION NOTE

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Introduction

Today's microprocessors require demanding power supply requirements for their core voltage (V–core). They have low input voltages and high input currents as well as large dynamic changes in load. Input voltages have been trending from 2.5 V towards 1.2 V just over a couple of years. The input currents have gone the opposite direction, with a trend from just 15 A to 80 A. Adding on top of this is the tolerance the processor places on the input voltage for dynamic changes in load, where a change of 100 mV for a modest current load change of 20 A at 20 A/usec has now gone to 60 mV for a current step of 65 A at 400 A/usec.

There is also the matter of input supply voltages going from 5 V to 12 V at the same time. The only viable topology for meeting these requirements is the buck converter. And since the amount of current that can be supplied typically from a synchronous buck is 20–30 A, a multiphase buck is needed for 60–80 A. There are many references one can review for what multiphase buck converters are and what they are intended to do.

Another approach that has been adopted in the design of multiphase converters is adaptive voltage positioning (AVP). This has the benefit of reducing the overall output voltage change when a load current step occurs. Figure 1 shows how the output of the supply "adapts" itself to "position" its "voltage" to the level where the initial output change has occurred instead of trying to return to the initial value:

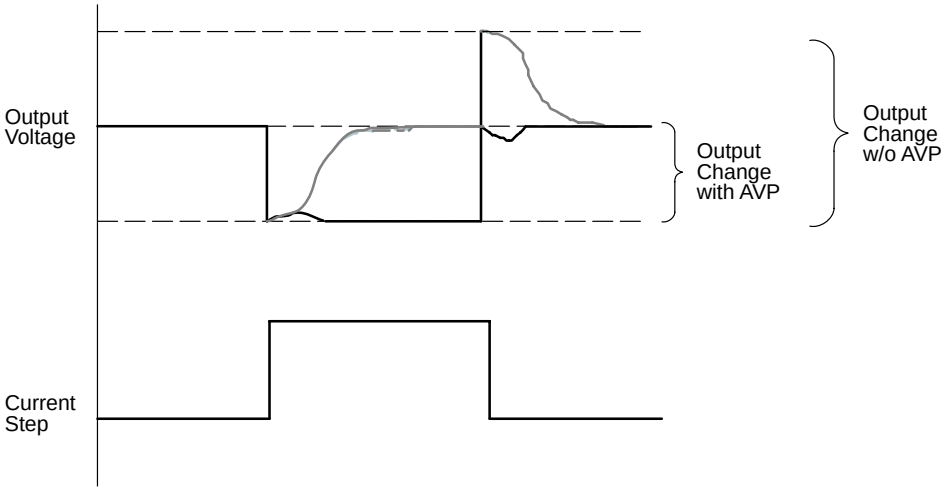

Figure 1. Output Change for Change in Output Current

From this figure, one can see that with AVP, the total change in output voltage can be cut in half. Another way of viewing AVP is to think of the power supply as having a finite output "droop resistance".

One method of implementing AVP is to actually put a droop resistor in the output. But this adds thermal loss to the system as well as being a passive, open loop resistance. Another approach is to provide the droop actively, which means measuring the current and providing active control of the output voltage.

The multiphase Enhanced V^2 devices offered by ON Semiconductor provide an active control method for implementing AVP into a single or multiphase buck converter for these power supply applications. These

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devices can be used for embedded designs (VR) or as part of voltage regulator modules (VRM). It is the intent of this design guide to explain the basics needed for implementing these devices.

Before this can be done, we need to look at the supply requirements and all of the variables associated with meeting these.

V–core Specification

V–core specifications are based upon the μP and platform. It is given as a load line with maximum and minimum limits based on the load current. Figure 2 shows a typical load line diagram and the associated parameters of interest.

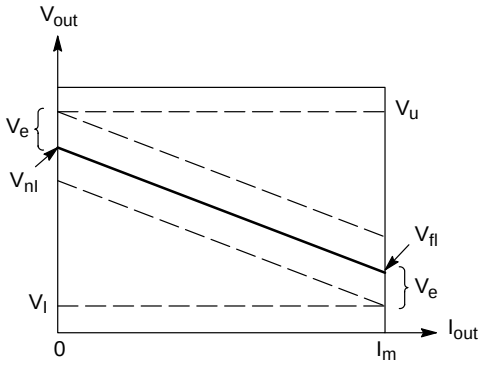


Figure 2. Load Line Characteristics

One needs to determine the load line characteristics based on the platform. Then the following terms can be computed:

$$V_e = V_u - V_{nl} = V_{fl} - V_l$$
$$V_d = V_{nl} - V_{fl}$$
$$R_o = V_d / I_m$$

I_m – Full–load Current
R_o – Droop Resistance
V_d – Droop Voltage
V_e – Processor Minimum Voltage Limit
V_{fl} – Nominal Full–load Voltage
V_{nl} – Nominal No–load Voltage
V_u – Processor Maximum Voltage Limit

VR Controller Design for Enhanced V^2 Type Controllers

A VR controller needs to be chosen based on the VID code and platform. The controllers have been set–up around VRM standards and the one closest matching the platform should be used.

The following block diagram in Figure 3 is representative of all the Enhanced V^2 controllers and will be used for the basis of the VR design.

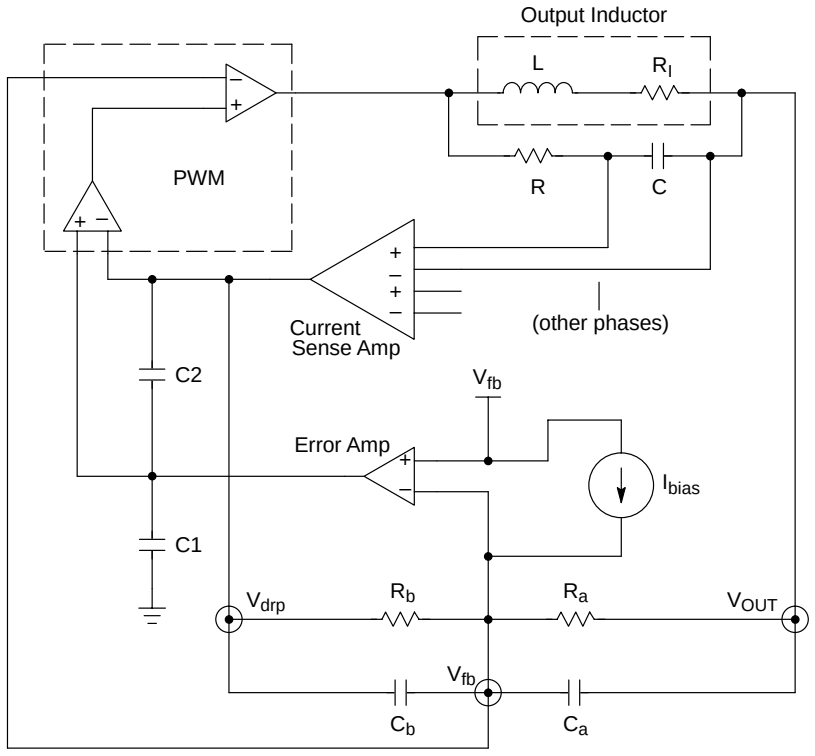


Figure 3. Enhanced V^2 Controller Topology

The Enhanced V^2 controller works as follows:

1. A sense voltage is generated using the RC and is differentially measured by the controller (for each phase). This signal is proportional to the current in the inductor. All of the phases are summed together and this becomes the V_{drp} signal. This signal is also the PWM ramp.
2. The output voltage (V_{out}) and V_{drp} are combined at the input to the error amp (V_{fb}). The error amp works to control the output voltage such that the voltage at V_{fb} is held constant.
3. I_{bias} is used to generate an output voltage difference (through R_a) from the V_{fb} setting for setting up the no–load output.
4. The ratio of R_b and R_a determines the amount of V_{drp} signal (which is proportional to current) that is fed to the output, thus determining the droop voltage.
5. C_1 and C_2 are used for compensating the error amplifier to get the proper output response for transients. They are also used during soft start (C_1+C_2).
6. C_a and C_b are used for compensating the error amp for dynamic response.
7. V_{fb} is also fed directly into the PWM for fast transient response. An immediate change in the output voltage shows up at V_{fb} before the error amp can compensate and input to the PWM for instant controller response.

The expression describing to overall output voltage is;

$$V_{out} = V_{fb} - I_{fb}R_a - I_{out}\left(A_S R_l \frac{R_a(1 + sL/R_l)(1 + sC_bR_b)}{R_b(1 + sCR)(1 + sC_aR_a)}\right)$$

Values for the electronic components shown need to be determined. This is based on the following design equations:

$$R_a = \frac{(V_{fb} - V_{nl})}{I_{fb}}$$

$$CR \le \frac{V_{fb} \cdot \left(1 - \frac{V_{fb}}{V_{cc}}\right)}{f_s \cdot V_{ramp}}$$

$$R_l(max) \le \frac{N}{I_m}\left(V_{ipeak} - \frac{V_{fb} \cdot \left(1 - \frac{V_{fb}}{V_{cc}}\right)}{2f_s \cdot RC}\right)$$

$$R_b = A_s \cdot \frac{I_m}{N} \cdot R_l \cdot \frac{R_a}{(V_{nl} - V_{fl})}$$

A_s – Current Sense to Vdrp Gain
V_{cc} – Input Supply Voltage
V_{fb} – Feedback Set–point Voltage
V_{ramp} – Minimum PWM Ramp
V_{ipeak} – Peak Current Sense Voltage
f_s – Switching Frequency
N – Number of Phases

- The device and VID setting determine the value of V_{fb}. Ibias is used for setting the initial no load output based on V_{fb} and determines the value R_a.
- CR is chosen to produce the necessary PWM ramp for the controller and depends on the device (V_{ramp}), the selected V_{fb} voltage, the input supply (V_{cc}), and the switching frequency (f_s). It is recommended to keep the value for R < 15 K to minimize the impedance seen by the current sense amplifier.
- The value of the inductor resistance is limited by the pulse current limit in the device (V_{ipeak}) and needs to be less then this value.
- The value of R_b is based on the desired droop voltage and the current sense gain of the device (A_s).

The following design equations are used for determining the output error one can expect from the design. It is based on the device and the component selection. It details each of the error components as well as the ripple.

Initial output error:

$$\varepsilon_{fb} \cdot V_{fb}$$

No load droop error:

$$(\varepsilon_{ib} + \varepsilon_{ra}) \cdot (I_{fb} \cdot R_a)$$

Full load droop error:

$$(\varepsilon_{ra} + \varepsilon_{rb} + \varepsilon_{ac} + \varepsilon_{rl}) \cdot \left(\frac{R_a}{R_b} \cdot A_S \cdot I_m \cdot R_l\right)$$

Output ripple error:

$$\frac{V_{fb}}{(2f_S \cdot L)} \cdot \left(1 - \frac{NV_{fb}}{V_{cc}}\right) \cdot \left(\frac{R_a}{R_b} \cdot A_S \cdot \frac{L}{CR} + R_o\right)$$

Output droop offset error:

$$\frac{R_a}{R_b} \cdot V_{os}$$

ε_{fb} – Feedback Voltage VID Set Point Error
ε_{Ib} – Feedback Bias Current Error
ε_{ra} – Resistor (R_a) Error
ε_{ab} – Resistor (R_b) Error
ε_{ac} – Current Sense to V_{drp} Gain Error
ε_{rl} – Inductor Eesistance Error (including over temperature)
V_{os} – V_{drp} Offset Voltage
R_o – Droop Resistance
L – Output Inductor Value

The values for C_1 and C_2 will be determined after the output capacitor selection has been made for the VR design. The values of C_a and C_b are determined as follows;

$$C_a = \frac{1}{R_a}(L/R_l) \qquad C_b = \frac{1}{R_b}(CR)$$

Once these definitions have been made, the output voltage expression now becomes;

$$V_{out} = V_{nl} - I_{out}R_o$$

Fortunately, a spreadsheet program exists for each controller type to aid in designing the correct values for the components to use as well as determining the error associated with the design. A design example later in this guide will demonstrate the use of these design equations.

It is now necessary to look at the overall design of the VR for proper output capacitor selection and final controller design.

VR Circuit Model

Figure 4 shows an electronic model of the VR supply with the controller, bulk capacitors, and high frequency capacitors represented.

For an MP SMPS to achieve the load line characteristics shown if Figure 2, it must have a constant output impedance ($Z_o = R_o$) as a function of frequency so the transient and static response of the supply matches the load line. In reality, there is an upper frequency limit where the output will look inductive. Let's look at the high frequency end first.

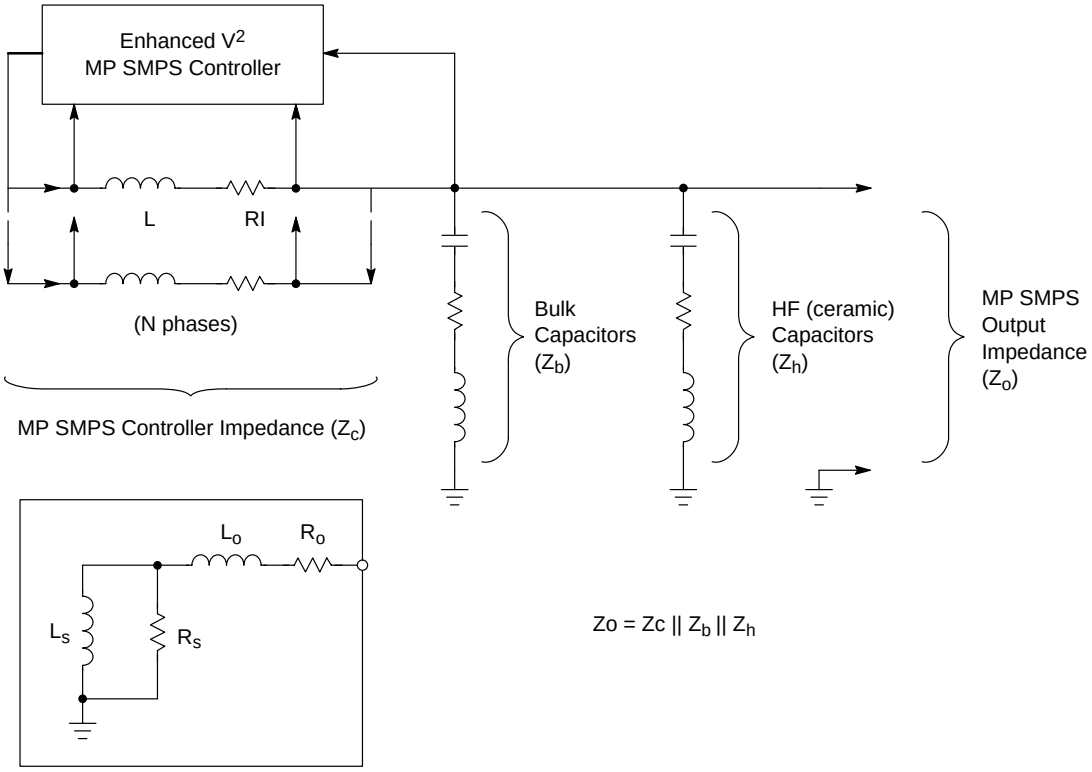


Figure 4. Multiphase Switch Mode Power Supply (MP SMPS) Electronic Model

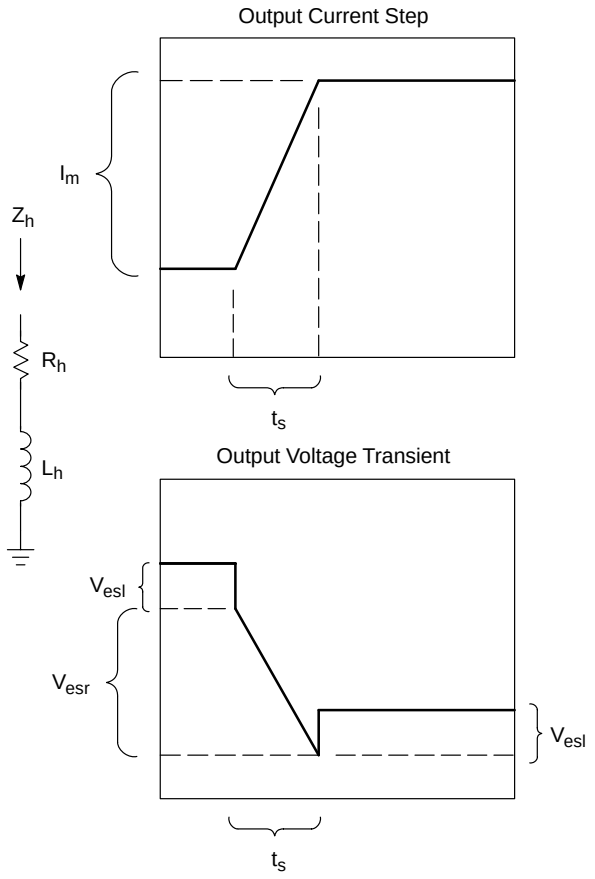


Figure 5. VR Output Response for Slew–Rate Limited Current Step

High Frequency Capacitor Specification

At the high end of the frequency spectrum, the output of the VR appears as the series combination of the ESR and ESL of the high frequency capacitors. Figure 5 shows the current step response of the processor and the corresponding output voltage change.

Comparing the output response to the load line requirements, the following design guidelines can be created for the high frequency capacitor;

$$S_i = I_m/t_s$$
$$V_{esl} = L_h \cdot S_i \le V_e$$
$$\therefore L_h \le V_e/S_i$$
$$V_{esr} = I_m \cdot R_h = V_d$$
$$\therefore R_h \approx R_o$$

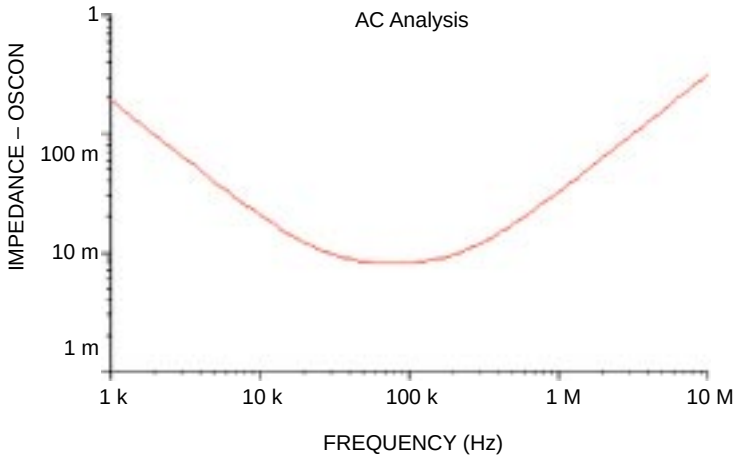
S_i – Current Slew Rate (specified for processor)
L_h – ESL of High Frequency Capacitor
R_h – ESR of High Frequency Capacitor

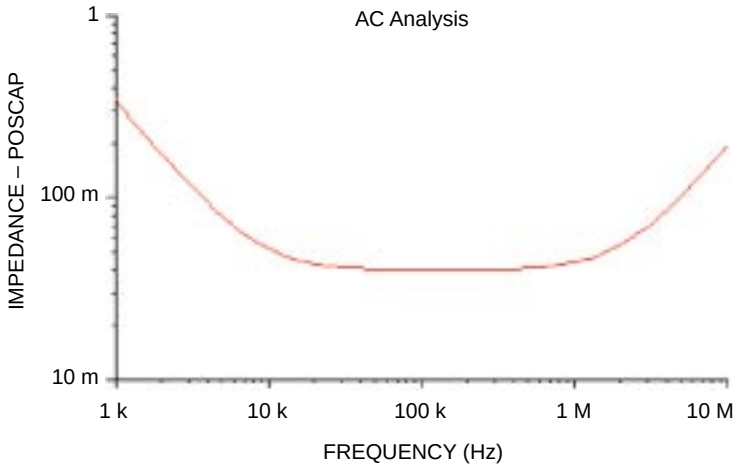
With the values of R_h and L_h known, a type of capacitor needs to be selected. One method of doing this is to look at the “high frequency knee” required of the capacitor:

$$F_{high} = \frac{R_h}{2\pi \cdot L_h}$$

One needs to choose a capacitor type close to this value, where F_{high} is the high 3dB frequency. Figure 6, details several types of capacitors and the parasitics associated with them.

	OSCON (4 V, E/F case)	POSCAP (D4 case)	X5R Ceramic (6.3 V, 1206)
Capacitance	560/820 μF	680 μF/2.5 V, 470 μF/4 V	10 μF
ESR	10/8 m	40 m	20 m
Low 3dB F (kHz)	28/24	5.9/8.5	800
ESL	5 nH	3 nH	1.6 nH
High 3dB F (MHz)	0.32/.25	2.1	2.0





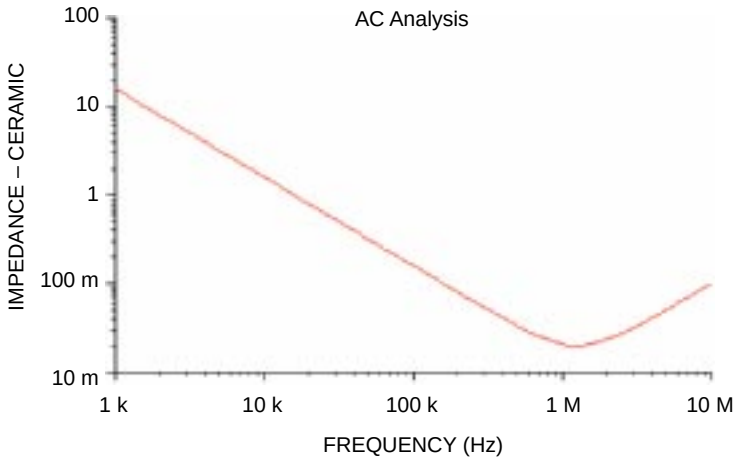


Figure 6. Characteristics of Several Capacitor Types

Once a capacitor is selected, the number of capacitors required is based on how many in parallel does it take to get L_h and R_h. Typically, more will be needed for parasitics associated with the PCB.

VR Controller Output Impedance

The model for the output impedance of a Enhance V^2 controller and it's corresponding frequency response is shown in Figure 7.

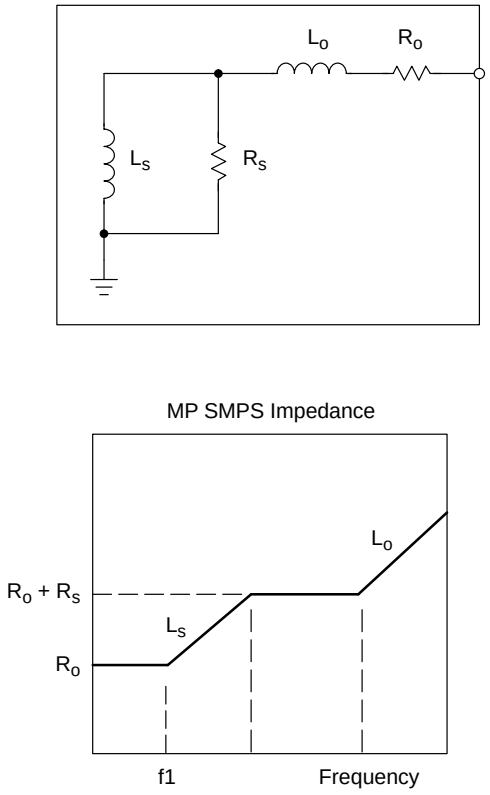


Figure 7. Enhanced V^2 Controller Output Impedance

The main parameters of interest are the frequency location (f1) and the value R_o (which we already know and have designed around). The value of f1 will be determined in the following section and will be set using C_1 and C_2. Notice the VR controller is used for controlling the impedance of the VR output at lower frequencies. The frequency point f1 typically has a maximum limit based on the controller and design.

The following expressions show the relationship of the VR controller design and the parameters shown in the impedance model:

$$L_o = \frac{1}{N \cdot f_s}\left(\frac{L}{CR} + R_o\right)$$

$$R_S = (1 - K_c) \cdot \left(R_o + \frac{A_S \cdot L}{CR}\right)$$

$$L_S = \frac{C_m}{g_m} \cdot R_S$$

$$R_o = \frac{A_S \cdot R_I \cdot R_a}{R_b}$$

$$K_c = \frac{C_2}{C_1 + C_2} \qquad C_m = C_1 + C_2$$

These are given as reference and are not intended to be directly used by the designer.

Bulk Capacitor Specification

At this point, we have selected high frequency capacitors for the high frequency impedance of the VR and designed the controller for the low frequency end. Based on the type of controller and high frequency capacitors, there will likely be a need for bulk capacitors. These are to handle making the VR impedance be the value desired (R_o) at frequencies in the range greater than the f1 of the controller and less then the lower 3 dB frequency of the high frequency capacitor.

Figure 8 shows a typical impedance plot where the impedance of the VR controller and high frequency capacitors are combined. These values on the plot are based on the design example given later.

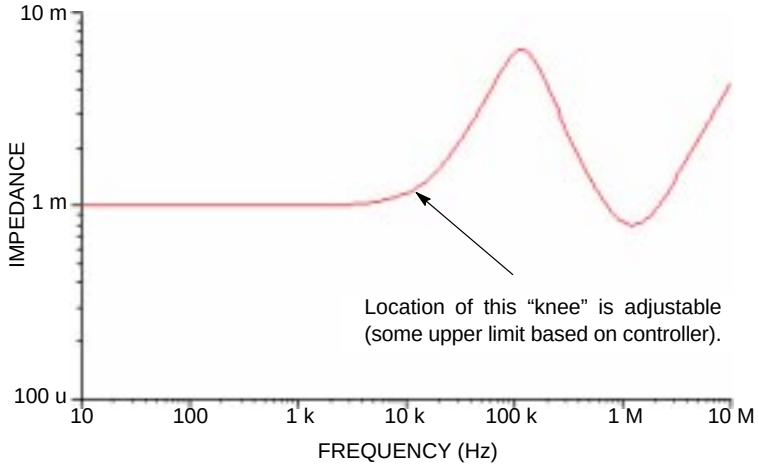


Figure 8. VR Output Impedance for VR Controller and High Frequency Capacitors

Notice that we need to provide bulk capacitors for a given frequency range. This range depends on the limit f1 and the lower 3 dB frequency of the high frequency capacitors. It is desirable to have these points coincide with another capacitor type so we can achieve a flat impedance response. Choosing a bulk capacitor that has its upper 3 dB point that is close to the lower 3dB point of the high frequency capacitor can do this. The VR controller's f1 point is then set to be close to the lower 3 dB point of the bulk capacitors. Using the following expression does this;

$$C_1 = \frac{g_m}{2\pi f_{low}} - C_m$$

C_m – Comp Capacitance
g_m – Error Amp Transconductance
f_{low} – Lower 3dB of Bulk Capacitors

Here, the values for g_m and C_m are dependent on the controller being used.

The amount of bulk capacitors will depend on their ESR (R_b) and the $R_o + R_s$ of the controller. The value of the output impedance appears as the parallel combination of R_b and $R_o + R_s$, and wants to be R_o. Solving for R_b based on this yields:

$$R_{bulk} = R_o\left(1 + \frac{1}{(1 - K_c)\left(1 + A_s\frac{L}{CRR_o}\right)}\right)$$

Knowing the value of R_{bulk}, one can determine the number of bulk capacitors required in parallel to get this value. More may be required based on capacitor variations and PCB parasitics.

Complete VR Output Impedance Response

Figure 9 shows the complete response for the output impedance of a VR that has been properly designed. It also shows the individual contributions of the VR controller, bulk capacitors, and high frequency capacitors.

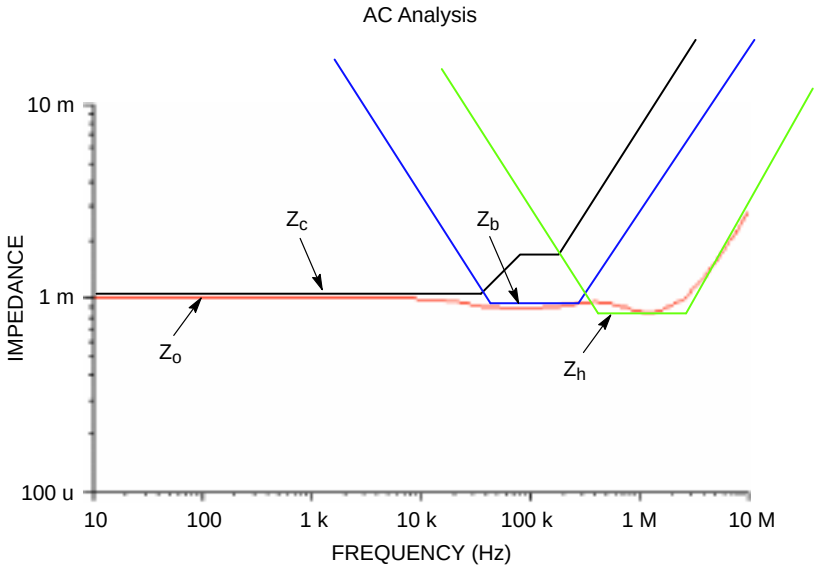


Figure 9. Complete VR Output Impedance Response

This concludes the design analysis. An actual design will show how this approach is used.

Example VR Design

For a design example, the following load line is used:

$V_u = 1.475$ V
$V_l = 1.34375$ V
$V_e = 25$ mV
$I_m = 65$ A
$S_i = 350$ A/μs

The CS5323 controller is chosen since it is designed around the VRM 9.0 standard (which is the closest match to this example) and has the MOSFET gate drivers external (makes layout more flexible). The gate drivers chosen are the CS1205.

A switching frequency of 250 kHz is chosen for minimizing the thermal loss on the FETs and for getting the transient response with the minimum of output capacitors. One can use the spreadsheet program to determine the optimal frequency based on output errors, output ripple, and inductor. The thermal losses will be presented in the "Thermal Management" section.

Figure 11 shows the spreadsheet values used for this design.

The load line parameters and VID setting are entered as well as the input supply voltage (12 V). The values for R and C are then determined (15 kΩ and 0.02 μF).

The maximum value for the inductor resistance is shown. A minimum value is also shown based on having a large enough signal for the current sense input to the CS5323. A value is input of 2.8 mΩ based on a chosen inductor.

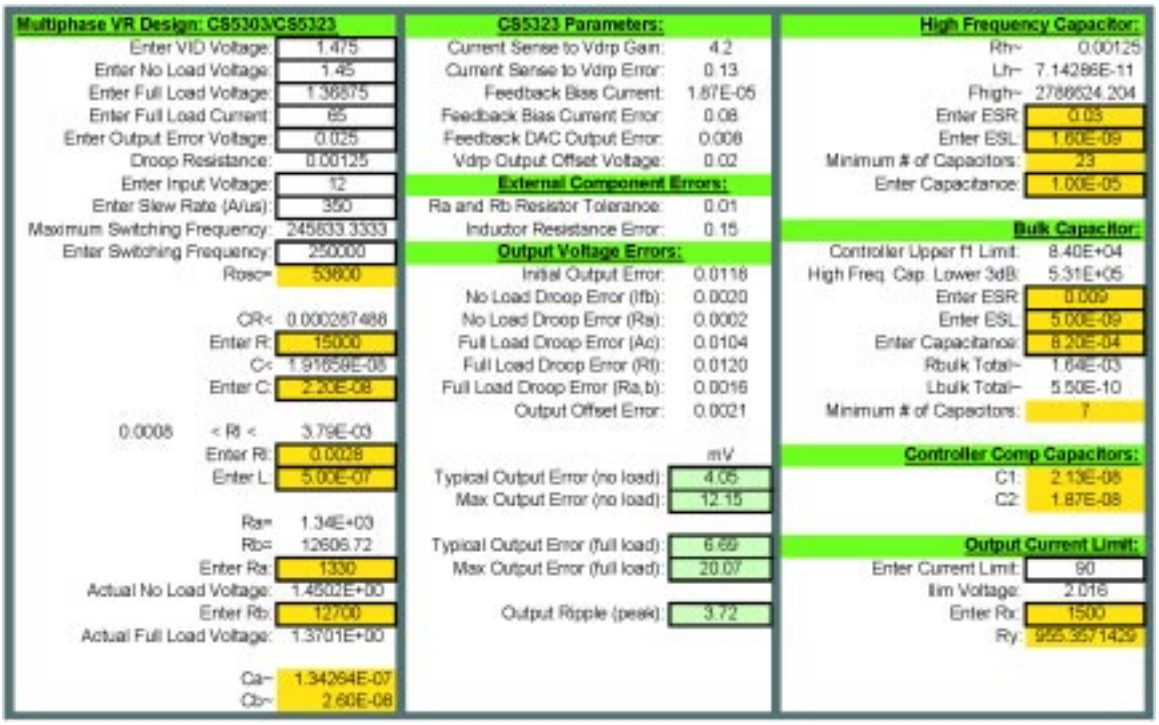


Figure 10. CS5323 Example V^R Design

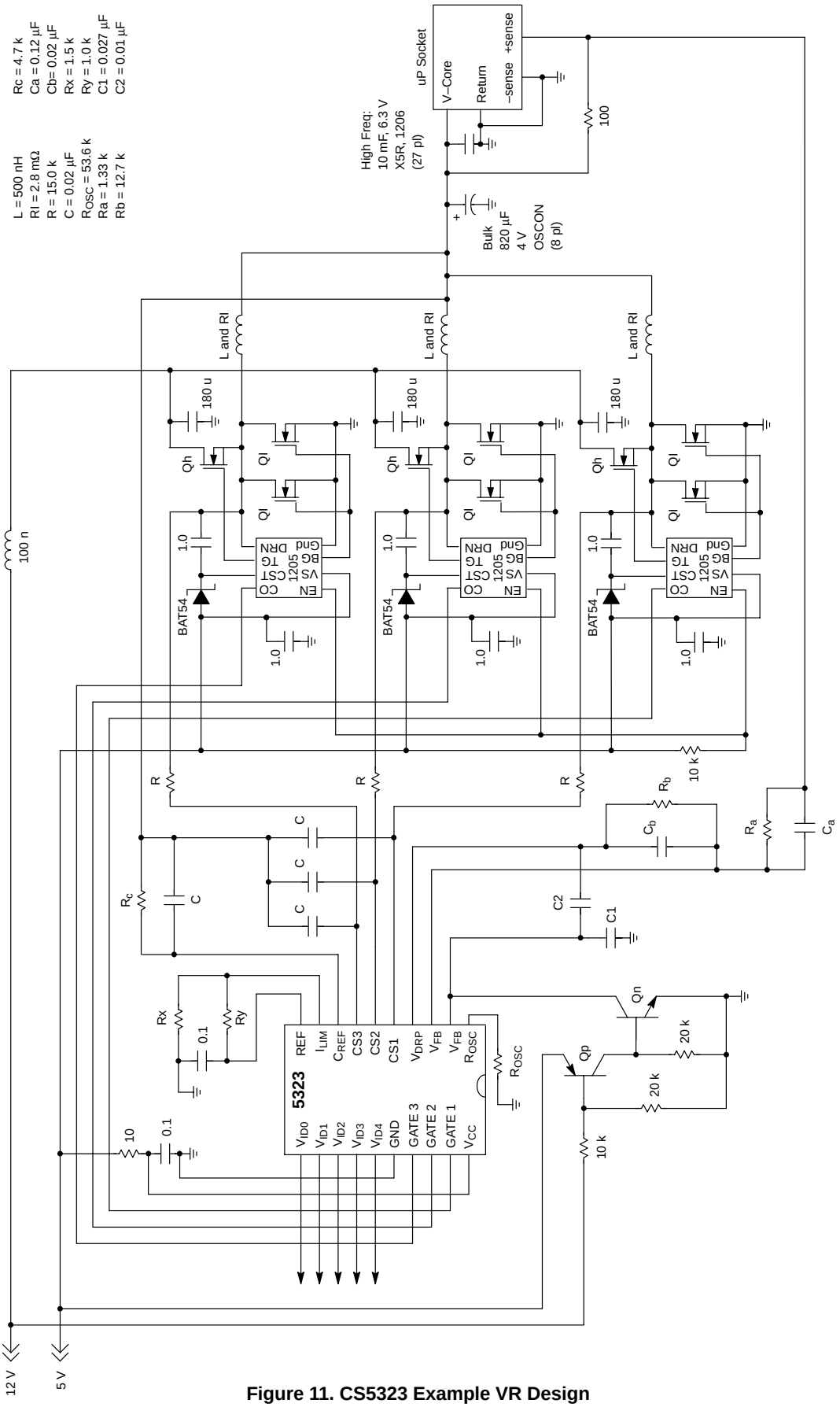


Figure 11. CS5323 Example VR Design

NOTE:
Since the Enhanced V^2 uses the inductor as a sense element, one needs to know a little about the inductor. One needs to know the inductor resistance, and since it changes 0.3%/C with temperature, it should be measured at the nominal operating temperature to minimize it's error. Notice an error of +/–15% was used in the analysis with the output error remaining below the required value. This value of tolerance is easily obtainable based on the inductor wire tolerance and typical thermal changes.

A good method for determining inductor resistance at nominal operating temperature is to do the following;

1. Hook up a precision current source to the inductor, with the inductor sitting by itself in a room temp environment (no airflow, inductor standing in air).
2. Set a current through the inductor at 70% of maximum load.
3. Wait 20 minutes for the inductor to heat up and then measure the voltage drop right at the inductor.
4. Calculate the inductor's resistance by dividing the measured voltage by the current.

For the inductance of the inductor, use what is supplied by the vendor or calculate it knowing the number of turns (round up for partial turns) and the core material.

Once a design is completed around a particular inductor, only inductors with the same nominal inductance and resistance can be used in that design.

The value of inductance entered (500 nH) was based on wanting a ripple of 5 mV peak or less for the output error to remain below 25 mV total.

Shown on the spreadsheet are the errors associated with the design based on the CS5323 and the component values. The total error is the combination of the ripple and static errors and must be kept below the required error. By changing component values, one can change the magnitude of this error.

The nominal values for R_a and R_b are computed, with the actual values used being entered (732 and 6.34 K in this case with 1% resistors). The nominal values for C_a and C_b (0.24 μF and 0.047 μF) are then computed (one only needs to choose the closest capacitor value to the ones shown, with 0.22 μF and 0.047 μF actually used for this design).

The right side of the spreadsheet has been set up for determining the requirements of the high frequency and bulk capacitors. Based on the design and the value computed for Fhigh on the high frequency capacitors, a X5R 10 μF, 1206, 6.3 V capacitor comes close to meeting this requirement. After putting in the ESR and ESL for this component, the number of capacitors required is found (22 in parallel for this design). Typically, for the sake of PCB parasitics, about 20% more will be needed (27 are actually used in the final design). The capacitor's value is also entered.

Once the high frequency capacitors are chosen, the bulk capacitors need to at least cover the range from the controller's f1 limit and the lower 3 dB frequency of the high frequency capacitors. 820 μF, 4 V OSCONs are a good match for this, with the ESR, ESL, and capacitance values being entered. The minimum number of capacitors is then found to meet the VR specifications (7, with 8 actually used).

Also computed are the values for the Comp capacitors C_1 and C_2 for the VR controller (one only needs to choose the closest capacitor value to the ones shown, with 0.027 μF and 0.01 μF actually used for this design).

There is also a current limit function in the CS5323 that will limit the total output of the VR. It is based on setting a reference voltage at the Ilim pin and is based on the following:

$$I_{lim} = \frac{V_{lim}}{A_{lim} \cdot R_I}$$

Entering a limit of 90 A and selecting Rx to be 1.5 K, Ry is found to be 1 K.

Figure 11 shows the final schematic for the CS5323 based VR supply.

Note that the resistor going to the CSREF pin is to minimize offset errors created by the bias and offset currents from the CS amplifiers. Its value is given as Rc = R/3. The capacitor around this resistor is for noise compensation, with its value being C.

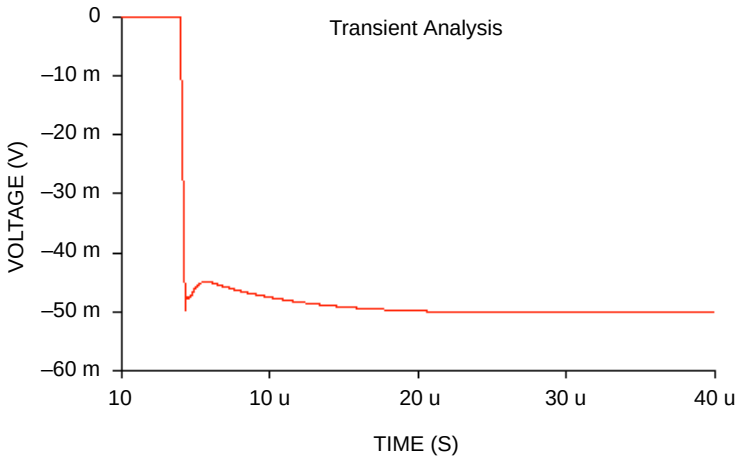


Figure 12. Simulated Transient Response for 45A step

Figure 9 is the simulated impedance response for this VR design. Figures 12 and 13 show simulated and actual output transient (45A step) responses for the VR design. It can be seen that the design is performing as specified.

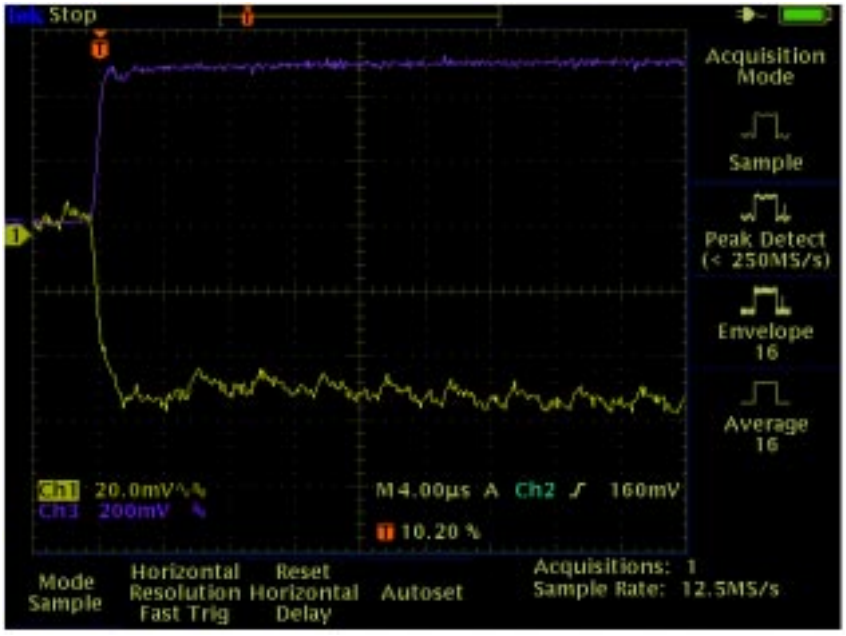


Figure 13. Actual Transient Response for 45A Step

Another circuit that includes a Power Good output as well as a Disable function is shown in Figure 13. The device used here is the CS5301, which has power good per VRM 9.0 specifications. This particular device also has the gate drivers internal.

The circuit design shown is for the same load line used for the design example. A spread sheet program similar to the one shown in Figure 11 was used for the CS5301.

Several other devices are available for various circuit topologies and ON Semiconductor should be contacted for more details.

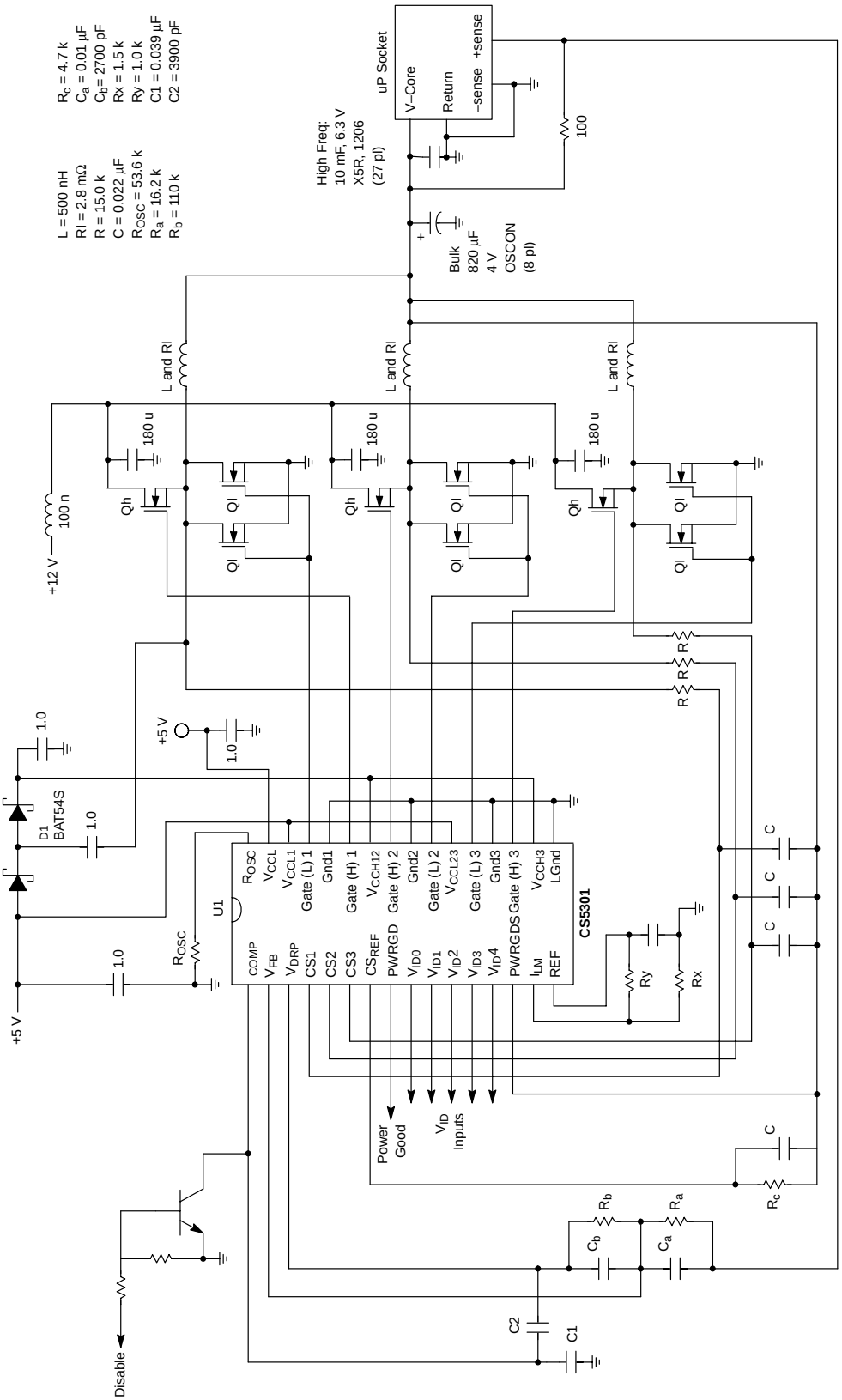


Figure 14. Example CS5301 VR with Power Good and Disable

Layout Recommendations

The layout of the VR supply becomes important for keeping the PCB parasitics from affecting the performance of the design. For the Enhanced V^2 controller, the following guidelines should be adhered to:

1. All high frequency capacitors should be located as close as possible to the μP socket. This includes placing of components “inside” of the socket. Figure 15 details the approach for this.
2. All components associated with the controller should be mounted as close as possible to the controller with minimal trace lengths. Figure 16 details the components this refers to.
3. The MOSFET drivers, MOSFETs, and inductors should be mounted together as close as possible per phase. This also includes the input supply filter capacitor for each phase. These will be referred to as “phase drivers”.
4. Each of the “phase drivers” should be somewhat equally spaced from the μP socket.
5. The bulk capacitors should be mounted between the “phase drivers” and the μP socket, being mounted as close as possible to the socket. If the “phase drivers” are separated from each other substantially, the bulk capacitors should be divided up among them. Figure 17 details one example of “phase drivers”/bulk capacitor placement.
6. All trace lengths associated with the power supply delivery to the μP socket (V_{out} and return) should be as short as possible, as wide as possible, and multi–layered (with interleaved layers) to minimize the trace resistance and inductance.
7. For the feedback to the Enhanced V^2 controller and the controller itself, follow the steps and diagram outlined in Figure 18.

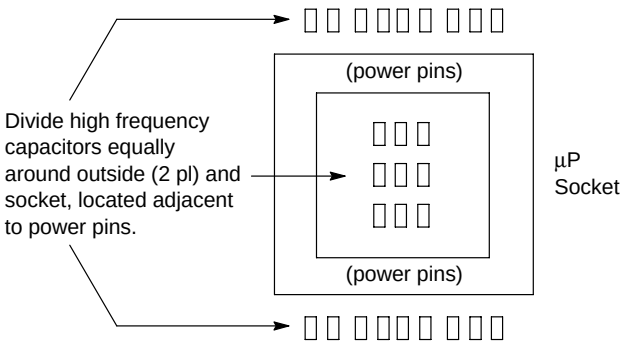


Figure 15. High Frequency Capacitor to Socket Placement

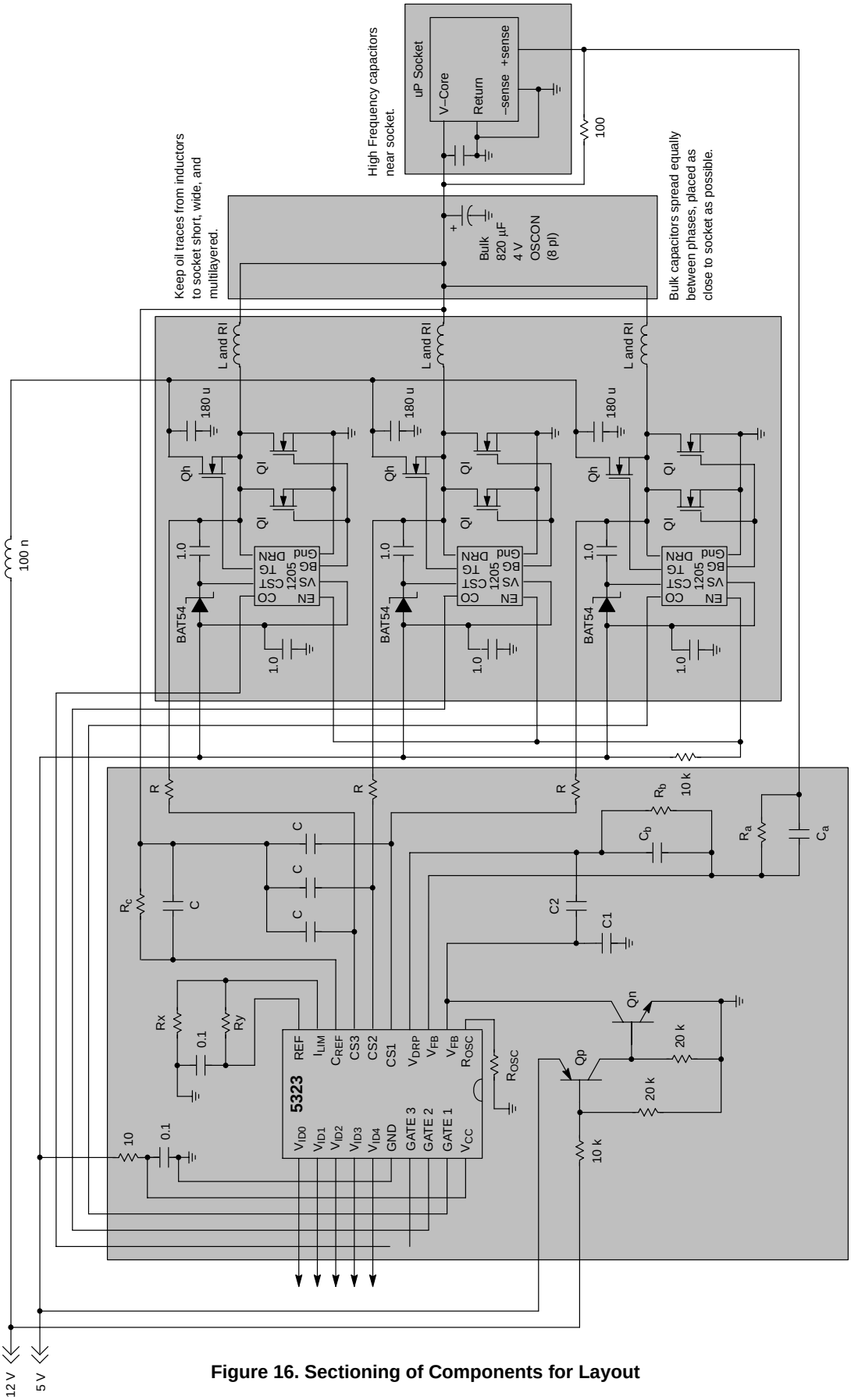


Figure 16. Sectioning of Components for Layout

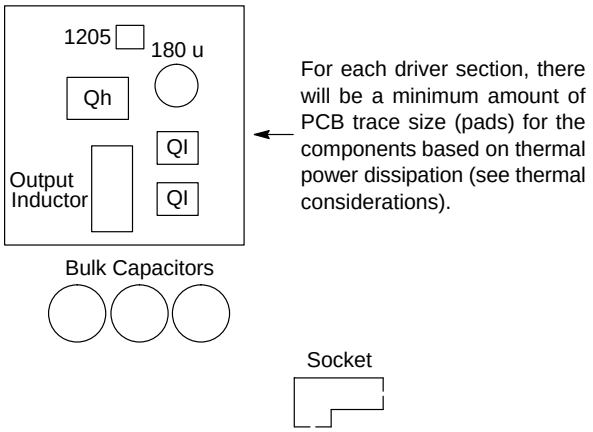


Figure 17. Phase Driver Layout

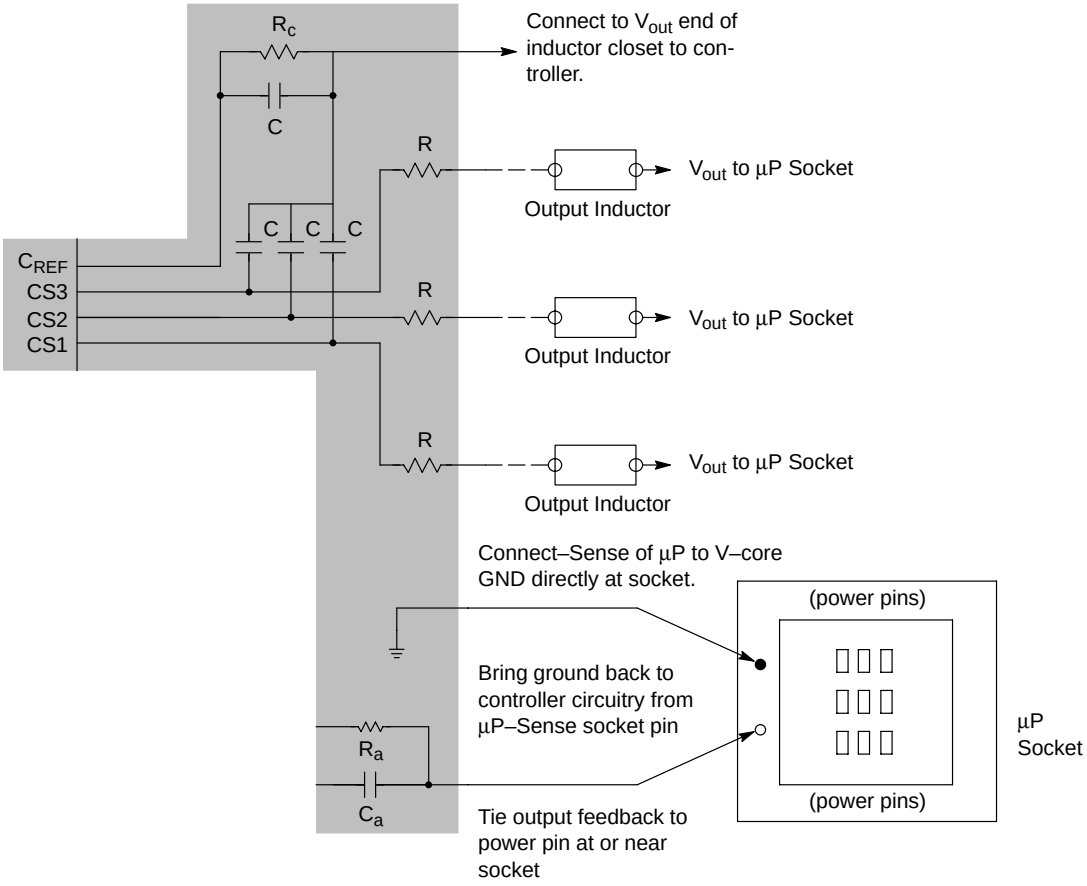


Figure 18. Layout for Connections to Controller Circuitry

The last recommendation is to route the gate driver lines from the controller away from the V_{fb}, Comp, and V_{drp} pins of the controller.

Thermal Considerations

From a power dissipation standpoint, the controller and gate drivers, although they will have thermal losses, do not require any special considerations.

The main components requiring attention during the design process are the high side and low side MOSFETs and output inductor. A thermal analysis on a per phase basis will show the main contributors to the losses:

$$P_{switch} = Q_o \cdot f_s \cdot V_{cc} \approx \frac{I_m}{3N}(t_{on} + t_{off})\, f_s \cdot V_{cc}$$

$$P_{condhigh} = D \cdot \left(\frac{I_m}{N}\right)^2 \cdot R_{dshigh}$$

$$P_{high} = P_{switch} + P_{condhigh}$$

$$P_{low} \approx P_{condlow} = (1 - D) \cdot \left(\frac{I_m}{N}\right)^2 \cdot R_{dslow}$$

$$D = \frac{V_{fb}}{V_{cc}}$$

P_{switch} – Switching Losses for High Side FET(s)
$P_{condhigh}$ – Conduction Losses for High Side FET(s)
P_{high} – Total Losses for High Side FET(s)
P_{low} – Total Losses for Low Side FET(s)
Q_o – Total Net Charge Displaced at Switching Node
D – Duty Cycle
R_{dshigh} – On Resistance for High Side FET(s)
R_{dslow} – On Resistance for Low Side FET(s)

The losses shown above are for the MOSFETs at the maximum output current. One needs to consider these losses based on how much PCB space is available (heatsink), cost (number of FETs/quality of FETs) and ambient. For most designs, the maximum PCB temperature and size of trace available for heatsinking will determine the limit for the maximum loss.

If need be, MOSFETs can be paralleled, where the total on resistance becomes the parallel combination.

As an example, a maximum PCB temperature of 105°C is assumed with a maximum ambient temperature of 55°C. This means a rise of 50°C is allowed. The following is a dual layer, 1 oz. cu PCB thermal resistance model based on size of pad area (of each layer):

$R_{\theta pa}$ ~ 20 – 30°C/W (1 sq. in.)
$R_{\theta pa}$ ~ 15 – 20°C/W (2 sq. in.)
$R_{\theta pa}$ – Thermal Resistance, PCB to Ambient

Let's assume we have 2 sq. in. of PCB pad area per phase for the FETs and that the thermal resistance is 15°C/W. This means we can have 3.33 W of power dissipation per phase. It is recommended to divide this equally between the high and low side FETs, thus making $P_{low} = P_{high} = 1.66$ W.

For our example design, we had $I_m = 65$, $V_{fb} = 1.5$, $V_{cc} = 12$, and $f_s = 250$ kHz. This yields the following:

$R_{dslow} \approx 4.3\ m\Omega$
$R_{dshigh}\ (m\Omega) + .33\ (t_{on} + t_{off})(nsec) \approx 27.6$

Before selecting a device, one must choose a FET based on the Rds specification at maximum junction temperature. For a case temperature of 105°C, most junctions will be around 5–10C hotter. Assuming 120°C junction, three 12 mΩ (at $V_{gs} = 4.5$ V, $T_j = 120°C$) low side DPak MOSFETs and one $(t_{on} + t_{off}) = 40$ nsec, 12 mΩ high side DPak ($V_{gs} = 4.5$, $T_j = 120°C$) were found to work.

The other component not mentioned so far is the inductor. Most of its thermal loss goes directly into the air, but it is desirable to keep the temperature rise minimized. A rough estimate for thermal resistance to ambient on an inductor designed for 20 A would be about 45°C/W, with the losses being:

$$P_{inductor} = \left(\frac{I_m}{N}\right)^2 \cdot R_l$$

For our example, we find the inductor's temperature rise to be 60°C. In fact, during test, the rise was slightly higher due to the inductor being soldered to the same pads that were doing the heat sinking for the FETs.

This thermal analysis is simple but gives one a feel for what is needed in the way of MOSFETs and PCB area. Due to the complexity of thermal dissipation in the PCB's environment, one should build and measure the actual temperature rises to make sure.

One last note on thermal issues is for the bulk and input supply capacitors. These capacitors need to be able to handle the ripple currents that will be flowing through them. In the case of multiple capacitors, divide the current up equally through each of them.

The RMS currents for the input and output are as follows:

$$I_{rmsinput} \approx D \cdot I_m \cdot \sqrt{\frac{1}{ND} - 1}$$

$$I_{rmsoutput} \approx \frac{1}{3}\frac{V_{fb}}{(2f_s \cdot L)} \cdot (1 - ND)$$

Fine Tuning Design

The previous design approach is intended for creating a solution close to the requirements of the V–core. But as with any complex analog design, there is usually some adjustments that need to be made. The variabilities depend on layout and component parasitics that enter into the performance.

The following is a straight forward method of “fine tuning” the components in the design to provide desired results. Due to component variability, one should look at a minimum of 3 circuit builds to determine the nominal adjustments to be made for the final design.

Set up the circuit to be tested with a DVM and oscilloscope to the output. Make sure to only have one ground from the scope hooked up or current may flow in the ground and cause errors. Have the scope set to DC input and set its offset so a resolution of at least 100mV/div is used and the output is visible on the screen.

1. No load output voltage:
   Using a DVM, measure the output voltage with no load. If this value is off from the expected value, adjust R_a until the nominal value is reached. Once this is set, mark this DC level on the scope with a cursor.
2. Full load output voltage:
   Using a DVM, measure the output voltage with full DC load. If this value is off from the expected value, adjust R_b until the nominal value is reached. Once this is set, mark this DC level on the scope with another cursor.
3. Transient response:
   Using a transient test tool (usually supplied with processor development kit), set it up for producing a current load step from a low current (typically 1 A) to maximum load at the slew rate being designed for. Set the current step at about 500 Hz with a duty cycle of 10%. One should see a response on the scope similar to that shown in Figure 19.
4. Error Amp compensation adjustment:
   Looking at scope, determine if there is a “bump” (green or blue trace) in the output. Adjust C_1 and C_2 to flatten out this bump. If you see the blue trace, make C_2 slightly larger and C_1 slightly smaller. If you see the green trace, do the opposite (if C_2 is already 0, just make C_1 larger).
5. Feedback compensation adjustment:
   Once the bump is removed, look to see if the transient response is larger or smaller than the DC level (this is the orange or pink trace). Make CA slightly larger if the AC gain (orange) is too large or slightly smaller if the AC gain (pink) is too small.
6. Optimal response:
   Once the output response resembles the red trace, the controller has been optimized for the design from a static and dynamic response.

NOTE:
If the output of the design appears to be jittering slightly, make the previous adjustments first, since they may solve this problem. If the problem persists, decrease the value of the RC across the inductor until the output jitter is acceptable and re–enter this new value into the spreadsheet and proceed again with the design.

Figure 20 shows an optimized response example. The current step is 1 to 60 A, with the horizontal cursors representing the no load and full load lines.

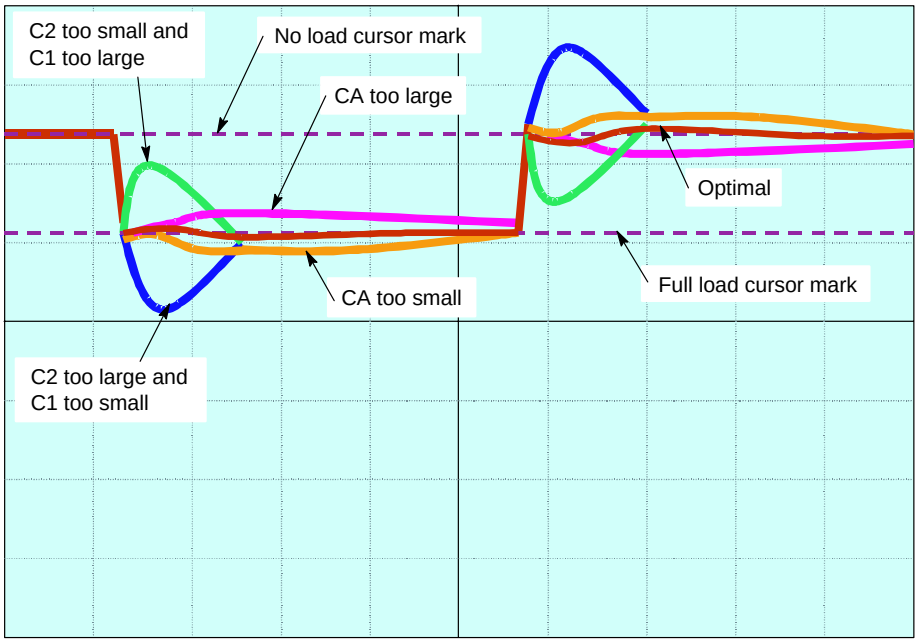


Figure 19. Transient Response Scope Plot for Fine Tune Analysis

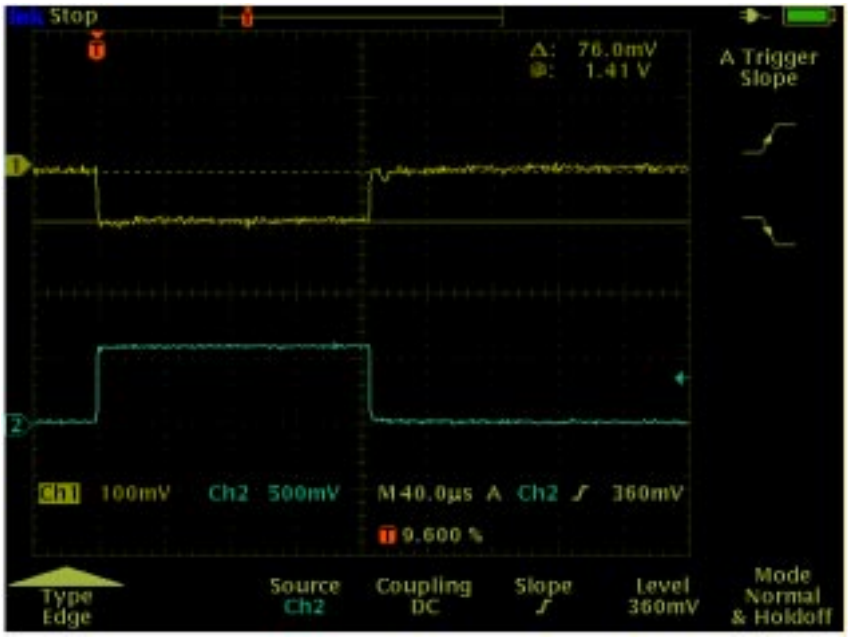


Figure 20. Optimized Enhance V^2 Design Scope Plot

Conclusion

This design guide is intended to give the designer the basics for using our Enhanced V^2 devices. There will however always be unknowns that will mess up any design. If you encounter any issues with using these devices, contact the factory for guidance.

There are also reference boards and designs available for all of our devices. These are intended to give the design engineer a starting platform for looking at and playing with our devices.

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