Low Voltage ECLinPS™ and ECLinPS Lite SPICE Modeling Kit

150Prepared by
Senad Lomigora and Paul Shockman
ON Semiconductor Broadband Application Engineers

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APPLICATION NOTE

Objective

The objective of this kit is to extend the information given in Application Note AN1503 for ECLinPS and ECLinPS Lite I/O spice modeling kit to the low voltage family of ECLinPS and ECLinPS Lite devices. The kit will provide enough circuit schematic and SPICE parameter information to allow a system level interconnect simulation to be performed using the Low Voltage ECLinPS and ECLinPS Lite device families. The Low Voltage ECLinPS and ECLinPS Lite are the additions to ON Semiconductor's highest performance ECL/PECL family of products. The families have packaged gate delays of 300 ps and output edge rates as low as 175 ps like the standard ECLinPS and ECLinPS Lite families, only at power supply levels of 3.3 V. The addition of these families extends the capabilities of the state–of–the–art in ECL/PECL to low voltage applications with no decrease in AC performance. **The kit is not intended to provide information necessary to perform circuit level modeling on individual Low Voltage ECLinPS and ECLinPS Lite devices.** If additional information is necessary, contact the factory application engineers.

Schematic Information

The kit contains representatives of input and output schematics, netlists, and waveform used for the Low Voltage ECLinPS and ECLinPS Lite devices. This application note will be modified as new devices are added. It should be noted that circuits can be used single ended by replacing INB with V_{BB} voltage source. Table 1 describes the nomenclature used for modeling the schematics and netlists in Low Voltage ECLinPS and ECLinPS Lite.

Table 1. Schematics and Netlist Nomenclature

Parameter	Function Description
V_{CC}	3.3 V for LVPECL and 0 V for LVECL
V_{EE}	-3.3 V for LVPECL and 0 V for LVECL
V_{BB}	Output Voltage Reference (Refer to Device Data Sheet)
V_{CS}	Internally Generated Voltage (≈V_{EE}+1.1V±50mV)
GND	Ground 0 V
IN	True Input to CKT
INB	Inverted Input to CKT
Q	True Output of CKT
QB	Inverted Output of CKT

Package

A worst-case model for various package types is included to improve the accuracy of the system model (refer to Table 2). The package model represents the parasitics as they are measured a sizable distance from an AC ground pin. If typical values are desired, reduce the inductance and capacitance parameters of the package model by 20%. The package models should be placed on all external inputs to an input model, all external outputs for an output model, and the V_{CC} line. Since the current in the V_{EE} pin is a constant, package model for V_{EE} pin is not necessary.

Table 2. Available Packages

Package Model	Page Number
8-Lead TSSOP	15
8-Lead SOIC	13
20-Lead TSSOP	23
20-Lead SOIC	17
28-Lead PLCC	36
32-Lead TQFP	28
52-Lead TQFP	36

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Input Buffer

The “TYPICAL INBUF” schematic and netlist are representing the input structure of device for Low Voltage ECLinPS and ECLinPS Lite families (see Figure 3). The schematic require the addition of ESD and package models to be accurate; but are otherwise functionally correct. It is unnecessary to include an ESD or Package model for the V_{BB} pins of the models because V_{BB} is intended as an internal node for most applications (see Figure 8). If V_{BB} is modeled as an external node, it is usually bypassed because it is a constant voltage, and adding ESD and Package parameters provide no additional benefit. ESD Schematics can be seen in Figures 6, 7, 9.

Output Buffer

There are three basic output structures for the Low Voltage ECLinPS and ECLinPS Lite device families. One is a simple standard 50 Ω drive ECL output used in the standard ECLinPS device and has about 3.5 mA of switch current. The second is the bandwidth enhanced ECLinPS Lite structure used to allow the bandwidth of the devices to be increased. Because the bandwidth of standard ECLinPS devices is limited by their rise and fall times, the limitation can be minimized by simply increasing switch current in the output buffer. The increased current charges and discharges parasitic capacitances rapidly and the current density is set to allow the device to perform at peak Fτ, thus the structure bandwidth is optimized. The enhanced output draws 7.0 mA of switch current.

Temperature Compensation Network (TCN) for 100K

The LVE and LVEL families are only offered in a 100K temperature and voltage compensated format. The temperature compensation network should be added to the output buffer schematics for proper modeling. Two different schematic structures can be seen in Figure 10. Any input or output that is driving or being driven by an off chip signal should include the ESD and package models. The output buffers show differential inputs and outputs. If it is necessary to simulate a single ended output; the load resistor, package model, ESD structure and output emitter follower, of the unused output, may be eliminated to simplify the system model. If an output is driven directly, instead of with an input cell there are two ways to do so, either differentially or single ended. Table 3 shows the necessary parameters to be met for correct SPICE modeling.

SPICE Netlist

The netlists are organized as a group of subcircuits. In each subcircuit model netlist, the model name is followed by a list of external node interconnects. Subcircuit models such as the Input or Output Buffer, Package, and “Input ESD / Resistor” should connect to supplies through hierarchical, passed parameters such as V_{CC}, V_{EE}, V_{CS}, etc., for proper simulation and not separately attached to independent power supplies.

SPICE Parameter Information

In addition to the schematics and netlists is a listing of the SPICE parameters for the transistors referenced in the schematics and netlists. These parameters represent a typical device of a given transistor. Varying the typical parameters will affect the DC and AC performance of the structures; but for the type of modeling intended by this note, the actual delay times are not necessary and are not modeled, as a result variation of the device parameters are meaningless. The performance levels are more easily varied by other methods and will be discussed in the next section. The resistors referenced in the schematics are polysilicon and have no parasitic capacitance in the real circuit and none is required in the model. The schematics display the only devices needed in the SPICE netlists.

Modeling Information

The bias drivers for the devices are not included as they are unnecessary for interconnect simulations and their use results in a large increase in model complexity and simulation time. The internal reference voltages (V_{BB}, V_{CS}, etc.) should be driven with ideal constant voltage sources. Table 3 summarizes the levels required, as well as some typical input parameters; and since the LVE/LVEL families are 100K type, the levels are the same for all temperatures and power supplies if the power supply is negative. If LVPECL mode is used, the levels vary one to one with the power supply; but are constant as a function of temperature.

The schematics and SPICE parameters will provide a typical output waveshape, which can be seen in Figure 11. Simple adjustments can be made to the models allowing output characteristics to simulate conditions at or near the corners of the data book specifications. Consistent cross–point voltages need to be maintained.

Table 3. Parameters

Mode	Structure	IN	INB	tr/tf (20 - 80%)	V_{CC}	V_{EE}
LVPECL	Differential	+1.1 V - +0.7 V	+0.7 V - +1.1 V	180 ps	+3.3 V	0 V
	Single Ended	+1.3 V - +0.7 V	+2.0V	180 ps		
LVECL	Differential	-1.2 V - -1.6 V	-1.6 V - -1.2 V	180 ps	0 V	-3.3 V
	Single Ended	-1.0 V - -1.6 V	-1.3 V	180 ps		

- To adjust rise and fall times

Produce the desired rise and fall times output slew rates by adjusting collector load resistors to change the gates tail current. The V_{CS} voltage will affect the tail current in the output differential, which will interact with the load resistor and collector resistor to determine tr and tf at the output.

- To adjust the V_{OH}

Adjust the V_{OH} and V_{OL} level by the same amount by varying V_{CC}. The output levels will follow changes in V_{CC} at a 1:1 ratio.

- To adjust the V_{OL} only

Adjust the V_{OL} level independently of the V_{OH} level by increasing or decreasing the collector load resistance. Note that the V_{OH} level will also change slightly due to a I BASE R drop across the collector load resistor. The V_{OL} can be changed by varying the V_{CS} supply, and therefore the gate current through the current source resistor.

Summary

The information included in this kit provides adequate information to run a SPICE level system interconnect simulation. The block diagram in Figure 1 illustrates a typical situation, which can be modeled using the information in this kit. Device input and output models are presented in Table 4 for LVEL and Table 5 for LVE devices.

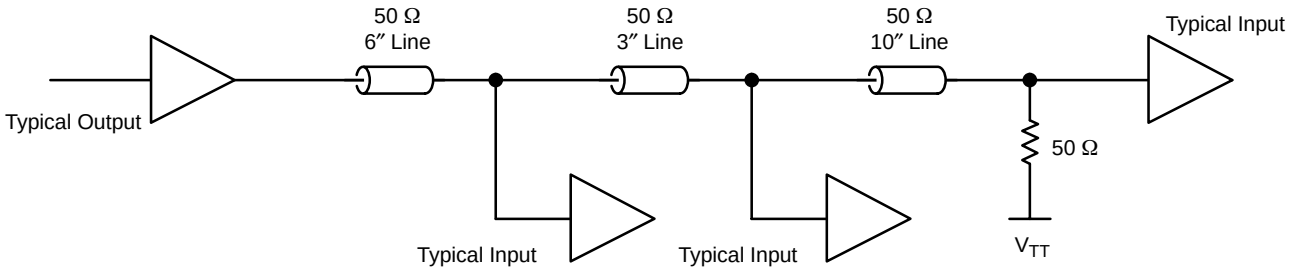

Figure 1. Typical Application for I/O SPICE Modeling Kit

Table 4. LVEL I/O SELECTION

Device	Function	All Inputs	Output
LVEL01	3.3V ECL 4 input OR/NOR	TYPICAL_INBUF	01OBUF
LVEL05	3.3V ECL 2 input Diff. AND/NAND	TYPICAL_INBUF	01OBUF
LVEL11	3.3V ECL 2:1 Differential Fanout Buffer	TYPICAL_INBUF	01OBUF
LVEL12	3.3V ECL Low Impedance Driver	TYPICAL_INBUF	01OBUF
LVEL13	3.3V ECL Dual 1:3 Fanout Buffer	TYPICAL_INBUF	02OBUF
LVEL14	3.3V ECL 1:5 Clock Distribution Chip	TYPICAL_INBUF	02OBUF
LVEL16	3.3V ECL Differential Receiver	TYPICAL_INBUF	01OBUF
LVEL17	3.3V ECL Quad Differential Receiver	TYPICAL_INBUF	02OBUF
LVEL29	3.3V ECL Dual Diff. Data and Clock D Flip-Flop With Set and Reset	TYPICAL_INBUF	02OBUF
LVEL30	3.3V ECL Triple D Flip-Flop With Set and Reset	TYPICAL_INBUF	02OBUF
LVEL31	3.3V ECL D Flip-Flop With Set and Reset	TYPICAL_INBUF	01OBUF
LVEL32	3.3V ECL 2 Divider	TYPICAL_INBUF	01OBUF
LVEL33	3.3V ECL 4 Divider	TYPICAL_INBUF	01OBUF
LVEL37	3.3V ECL 1:4 1/2 Clock Fanout Duffer	TYPICAL_INBUF	01OBUF
LVEL38	3.3V ECL 2/4, 4/6 Clock Generation Chip	TYPICAL_INBUF	02OBUF
LVEL39	3.3V ECL 2, 4/6 Clock Generation Chip	TYPICAL_INBUF	02OBUF
LVEL40	3.3V ECL Differential Phase-Frequency Detector	TYPICAL_INBUF	02OBUF
LVEL51	3.3V ECL Differential Clock D Flip-Flop	TYPICAL_INBUF	01OBUF
LVEL56	3.3V ECL 2:1 Multiplexer	TYPICAL_INBUF	03OBUF
LVEL58	3.3V ECL Dual Differential 2:1 Multiplexer	TYPICAL_INBUF	01OBUF
LVEL59	3.3V ECL Triple 2:1 Multiplexer	TYPICAL_INBUF	03OBUF
LVEL90	3.3V/5V Triple LVPECL/PECL Input to -3.3V ECL Output Transistor	TYPICAL_INBUF	02OBUF
LVEL91	-3.3V/-5V Triple ECL Input to LVPECL Output Transistor	TYPICAL_INBUF	02OBUF
LVEL92	5V Triple PECL Input to LVPECL Output Translator	TYPICAL_INBUF	02OBUF

Table 5. LVE I/O SELECTION

Device	Function	All Inputs	Output
LVE111	3.3V ECL 1:9 Differential Clock Driver	TYPICAL_INBUF	02OBUF
LVE164	3.3V ECL 16:1 Multiplexer	TYPICAL_INBUF	02OBUF
LVE210	3.3V ECL Dual 1:4, 1:5 Differential Fanout Buffer	TYPICAL_INBUF	02OBUF
LVE222	3.3V ECL 1:15 Differential 1/2 Clock Divider	TYPICAL_INBUF	02OBUF
LVE310	3.3V ECL 2:8 Differential Fanout Buffer	TYPICAL_INBUF	02OBUF

TYPICAL INBUF

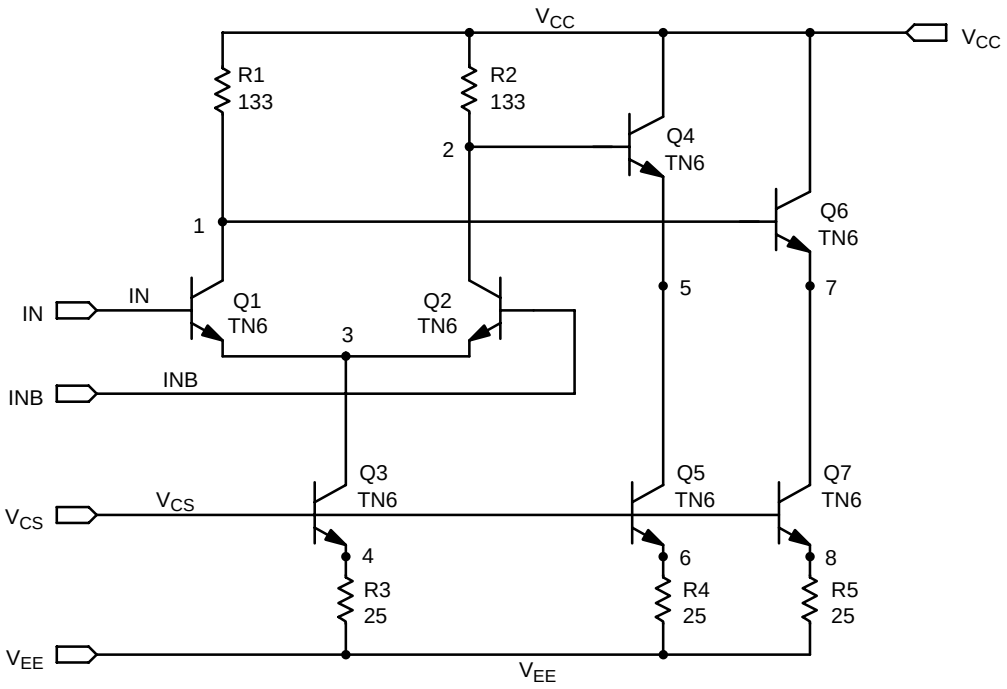

Figure 2. TYPICAL_INBUF

```
.SUBCKT TYPICAL_INBUF IN INB VCS VCC VEE
Q1 1 IN 3 TN6
Q2 2 INB 3 TN6
Q3 3 VCS 4 TN6
Q4 VCC 2 5 TN6
Q5 5 VCS 6 TN6
Q6 VCC 1 7 TN6
Q7 7 VCS 8 TN6
R1 VCC 1 133
R2 VCC 2 133
R3 4 VEE 25
R4 8 VEE 25
R5 6 VEE 25
.ENDS TYPICAL_INBUF
```

01OBUF

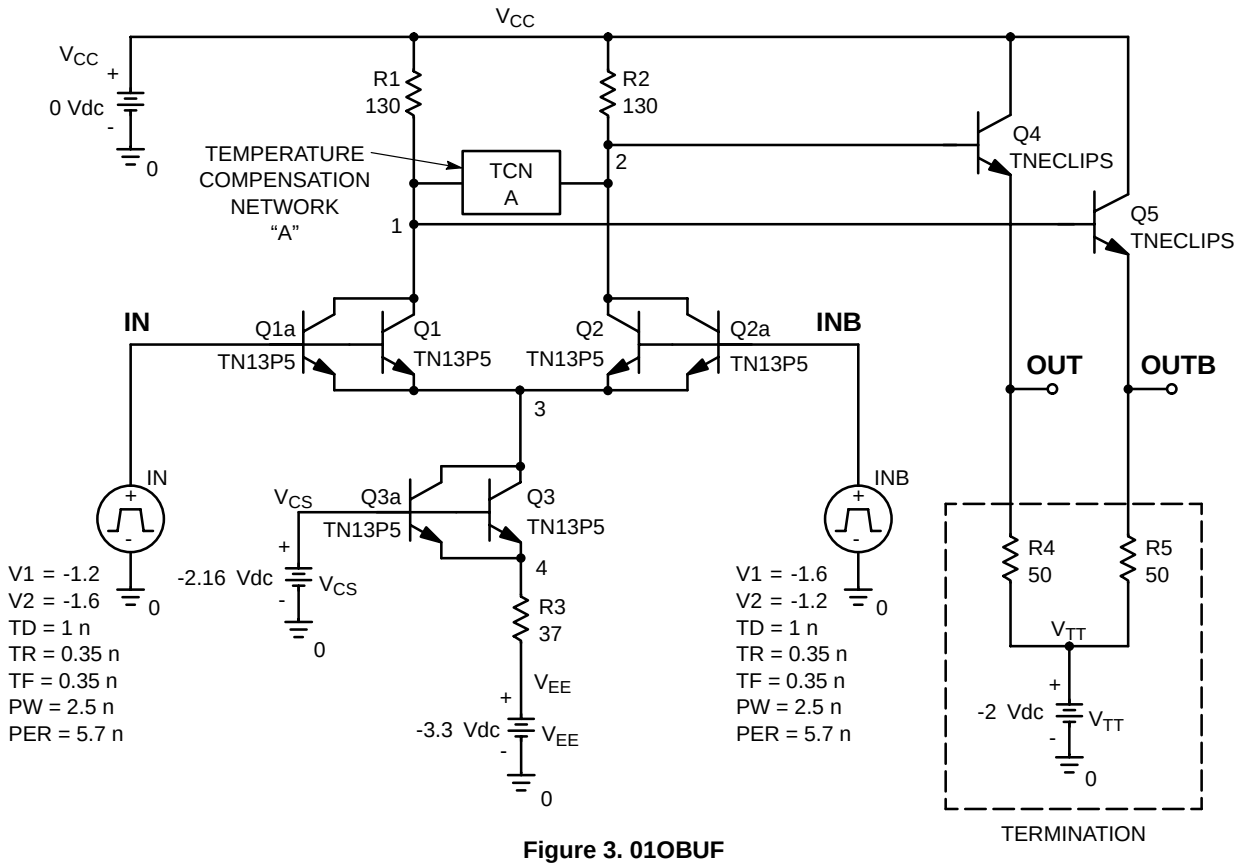

Figure 3. 01OBUF

```
.SUBCKT 01OBUF IN INB VCS VCC OUT OUTB VEE VTT
Q_Q1 1 IN 3 TN13P5
Q_Q1a 1 IN 3 TN13P5
Q_Q2 2 INB 3 TN13P5
Q_Q2a 2 INB 3 TN13P5
Q_Q3 3 VCS 4 TN13P5
Q_Q3a 3 VCS 4 TN13P5
Q_Q4 VCC 2 OUT TNECLIPS
Q_Q5 VCC 1 OUTB TNECLIPS
R_R1 1 VCC 130
R_R2 2 VCC 130
R_R3 VEE 4 37
R_R4 VTT OUT 50
R_R5 VTT OUTB 50
V_IN IN 0 +PULSE –1.2 –1.6 1n 0.35n 0.35n 2.5n 5.7n
V_INB INB 0 +PULSE –1.6 –1.2 1n 0.35n 0.35n 2.5n 5.7n
V_VCC VCC 0 0 Vdc
V_VEE VEE 0 –3.3 Vdc
V_VTT VTT 0 –2 Vdc
V_VCS VCS 0 –2.16 Vdc
.END 01OBUF
```

02OBUF

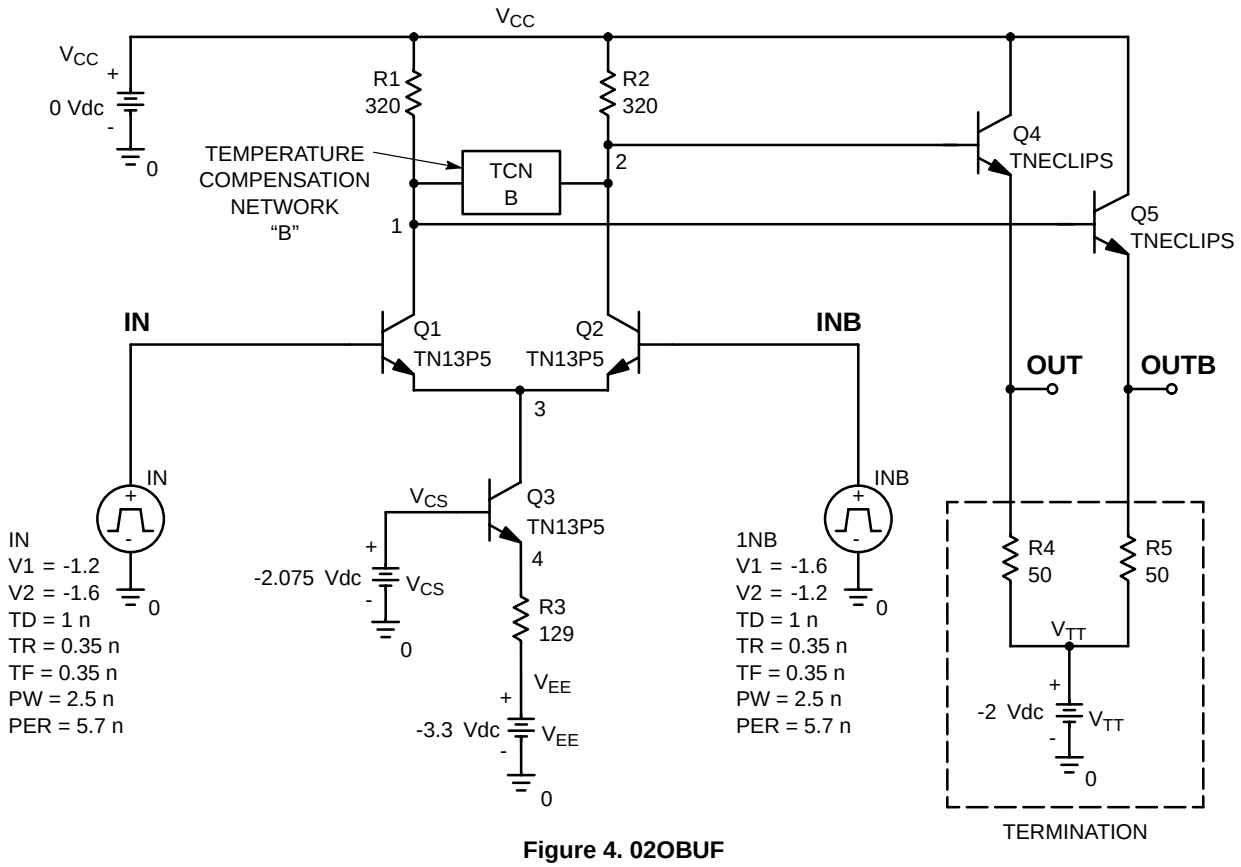

Figure 4. 02OBUF

```
.SUBCKT 02OBUF IN INB VCC VCS VEE VTT OUT OUTB
Q_Q1 1 IN 3 TN13P5
Q_Q2 2 INB 3 TN13P5
Q_Q3 3 VCS 4 TN13P5
Q_Q4 VCC 2 OUT TNECLIPS
Q_Q5 VCC 1 OUTB TNECLIPS
R_R1 1 VCC 320
R_R2 2 VCC 320
R_R3 VEE 4 129
R_R4 VTT OUT 50
R_R5 VTT OUTB 50
V_INB INB 0 +PULSE –1.6 –1.2 1n 0.35n 0.35n 2.5n 5.7n
V_IN IN 0 +PULSE –1.2 –1.6 1n 0.35n 0.35n 2.5n 5.7n
V_VCC VCC 0 0Vdc
V_VEE VEE 0 –3.3 Vdc
V_VTT VTT 0 –2 Vdc
V_VCS VCS 0 –2.075 Vdc
.END 02OBUF
```

03OBUF

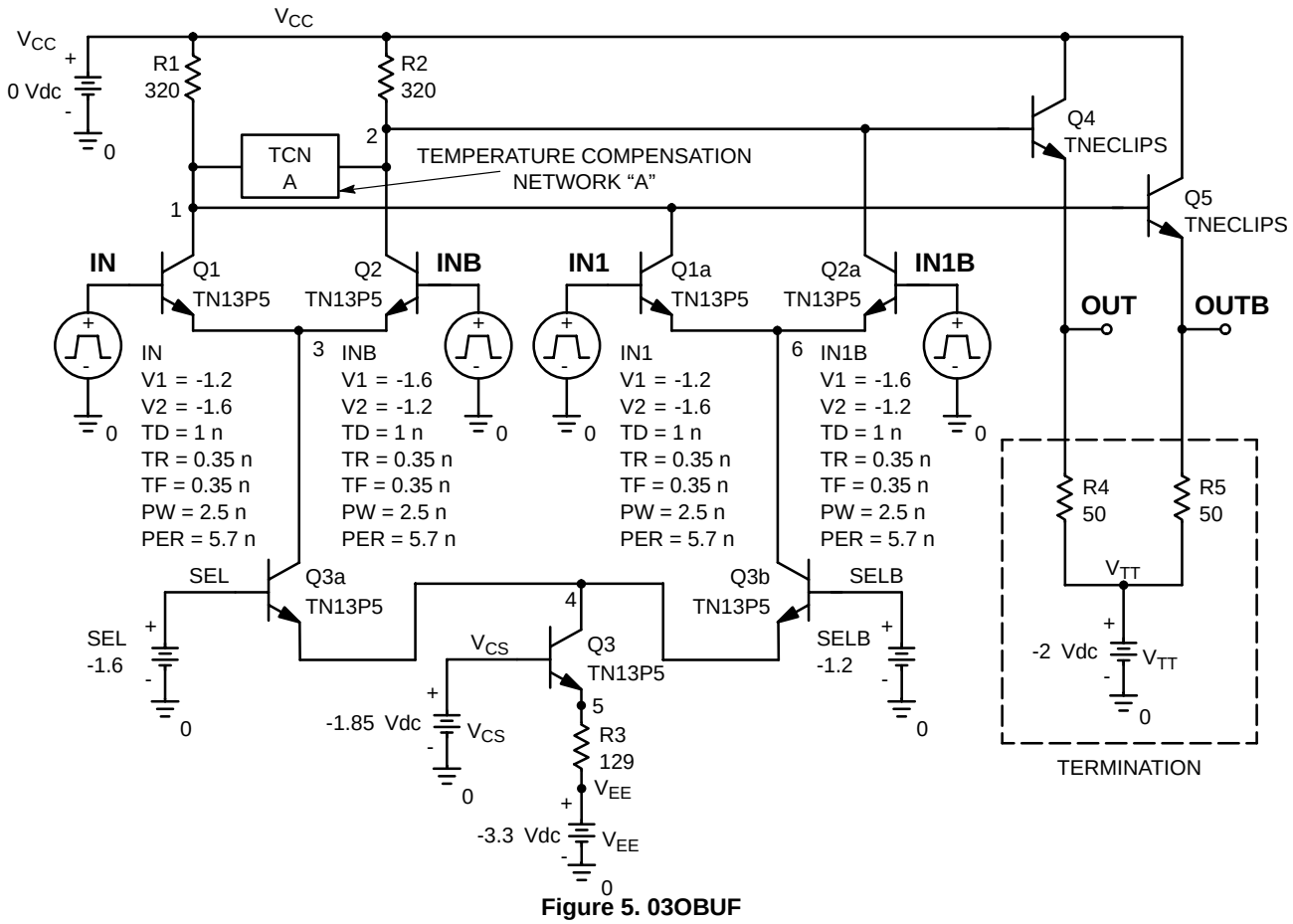

Figure 5. 03OBUF

```
.SUBCKT 03OBUF IN INB VCS VCC INI INIB SEL SELB VEE VTT
Q_Q1 1 IN 3 TN13P5
Q_Q2 2 INB 3 TN13P5
Q_Q3 4 VCS 5 TN13P5
Q_Q4 VCC 2 OUT TNECLIPS
Q_Q5 VCC 1 OUTB TNECLIPS
Q_Q1a 1 IN1 6 TN13P5
Q_Q2a 2 IN1B 6 TN13P5
Q_Q3a 3 SEL 4 TN13P5
Q_Q3b 6 SELB 4 TN13P5
R_R1 1 VCC 320
R_R2 2 VCC 320
R_R3 VEE 5 129
R_R4 VTT OUT 50
R_R5 VTT OUTB 50
V_IN IN 0 +PULSE –1.2 –1.6 1n 0.35n 0.35n 2.5n 5.7n
V_INB INB 0 +PULSE –1.6 –1.2 1n 0.35n 0.35n 2.5n 5.7n
V_IN1 IN1 0 +PULSE –1.2 –1.6 1n 0.35n 0.35n 2.5n 5.7n
V_IN1B IN1B 0 +PULSE –1.6 –1.2 1n 0.35n 0.35n 2.5n 5.7n
V_SEL SEL 0 –1.6
V_SELB SELB 0 –1.2
V_VCC VCC 0 0 Vdc
V_VEE VEE 0 –3.3 Vdc
V_VTT VTT 0 –2 Vdc
V_VCS VCS 0 –1.85 Vdc
.END 03OBUF
```

```
The following will hold for all ESD structures:
* PIN - end attached to the package
* CKT - end attached to CKT input
* VEE - is attached to most negative power rail
* VCC - is attached to most positive power rail
```

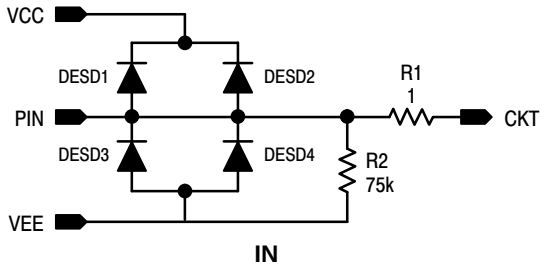

Figure 6. Input ESD with Pulldown Resistor

```
************************************************
**USE for the IN pin of a differential pair
.SUBCKT IN_ESD VCC VEE PIN CKT
DESD1 PIN VCC CBVCC
DESD2 PIN VCC CBVCC
DESD3 VEE PIN CBSUB
DESD4 VEE PIN CBSUB
R1 PIN CKT 1
R2 PIN VEE 75K
.ENDS IN_ESD
************************************************
```

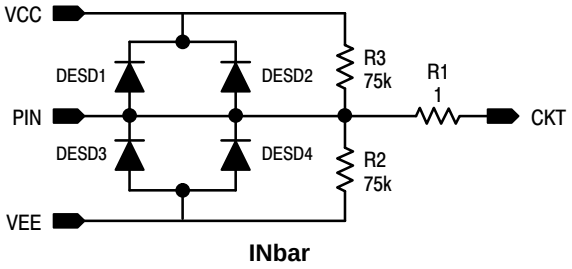

Figure 7. Input Bar ESD with Pulldown/Pullup Resistors

```
************************************************
**USE for the INB pin of a differential pair
.SUBCKT INB_ESD VCC VEE PIN CKT
DESD1 PIN VCC CBVCC
DESD2 PIN VCC CBVCC
DESD3 VEE PIN CBSUB
DESD4 VEE PIN CBSUB
R1 PIN CKT 1
R2 PIN VEE 75K
R3 VCC PIN 75K
.ENDS INB_ESD
************************************************
```

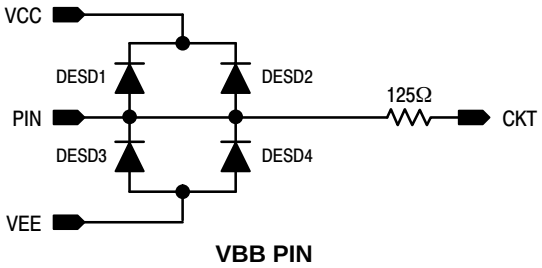

Figure 8. V_{BB} Pin ESD Structure

```
*****************************************************
**USE for VBB pins
*****************************************************
**USE for the IN pin of a differential pair
.SUBCKT VBB_ESD VCC VEE PIN CKT
DESD1 PIN VCC CBVCC
DESD2 PIN VCC CBVCC
DESD3 VEE PIN CBSUB
DESD4 VEE PIN CBSUB
R1 PIN CKT 125
.ENDS VBB_ESD
*******************************************************
```

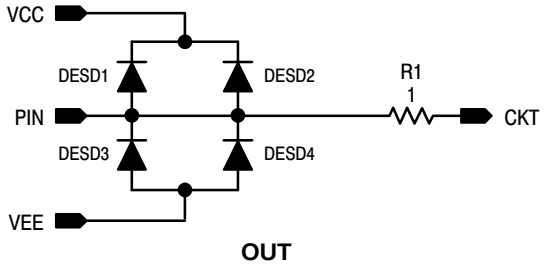

Figure 9. Output Pin ESD Structure

```
*****************************************************
**USE for the output
*****************************************************
**USE for the IN pin of a differential pair
.SUBCKT OUT_ESD VCC VEE PIN CKT
DESD1 PIN VCC CBVCC
DESD2 PIN VCC CBVCC
DESD3 VEE PIN CBSUB
DESD4 VEE PIN CBSUB
R1 PIN CKT 1
.ENDS OUT_ESD
*******************************************************
```

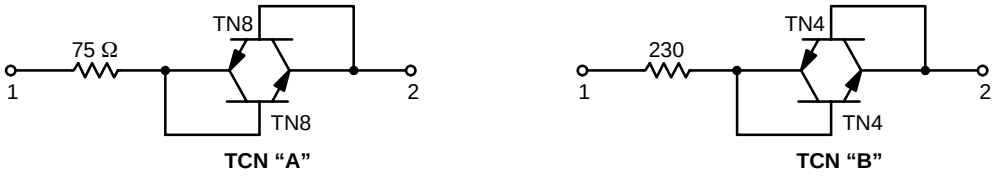

Figure 10. Temperature Compensation Network Structure

OUTPUT WAVEFORM

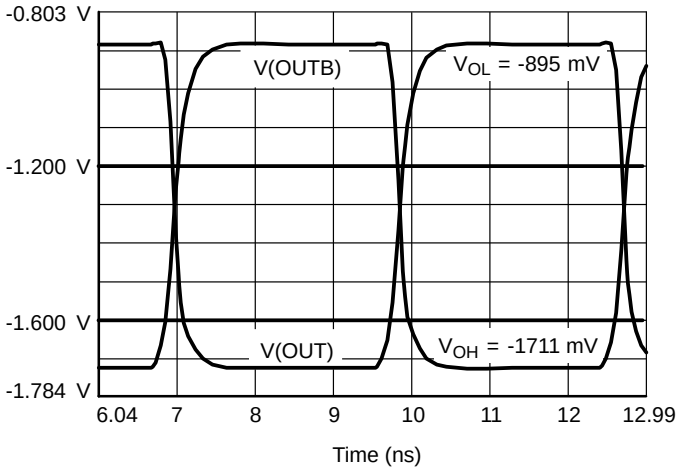

Figure 11. Simplified Model Output Waveform

*************Transistor and Diodes Nominal Spice Models*********************

```
.MODEL TN13P5 NPN (IS=2.09e-17 BF=120 NF=1 VAF=30 IKF=25.7mA
+ ISE=1.09e-15 BR=10 NE=2 VAR=5 IKR=2.25mA IRB=32.2uA RB=122.6
+ RBM=42.2 RE=5.44 RC=32.8 CJE=67.4fF VJE=0.9 MJE=0.4 XTB=0.73
+ CJC=53.8fF VJC=0.67 MJC=0.32 XCJC=0.3 CJS=103fF VJS=0.6 MJS=0.4
+ FC=0.9 TF=8pS TR=1nS XTF=10 VTF=1.4V ITF=67.5mA
+ ISC=0 EG=1.11 XTI=4.0 PTF=0 KF=0 AF=1 NR=1 NC=2)
**************************************************************************
.MODEL TNECLIPS NPN
+(IS = 2.27E-16 BF = 120 NF = 1 VAF = 30 IKF = 279mA
+ ISE = 1.19E-14 BR = 10 NE = 2 VAR = 5 IKR = 24.4mA
+ IRB = 349uA RB = 15.98 RBM = 4.17 RE = .501 RC = 11.1
+ CJE = 611fF VJE = .9 MJE = .4 XTB = 0.73
+ CJC = 440fF VJC = .67 MJC = .32 XCJC= .3
+ CJS = 668fF VJS = .6 MJS = .4 FC = .9
+ TF = 8pS TR = 1nS XTF = 10 VTF = 1.4V ITF = 733mA
+ ISC=0 EG=1.11 XTI=4.0 PTF=0 KF=0 AF=1 NR=1 NC=2)
**************************************************************************
.MODEL TN4 NPN
+(IS = 5.27E-18 BF = 120 NF = 1 VAF = 30 IKF = 6.48mA
+ ISE = 2.75E-16 BR = 10 NE = 2 VAR = 5 IKR = 567uA
+ IRB = 8.1uA RB = 461.6 RBM =142.5 RE = 21.6 RC = 83.1
+ CJE = 19.9fF VJE = .9 MJE = .4 XTB = 0.73
+ CJC = 25.1fF VJC = .67 MJC = .32 XCJC= .3
+ CJS = 49.6fF VJS = .6 MJS = .4 FC = .9
+ TF = 8pS TR = 1nS XTF = 10 VTF = 1.4V ITF = 17.0mA
+ ISC=0 EG=1.11 XTI=5.2 PTF=0 KF=0 AF=1 NR=1 NC=2)
**************************************************************************
.MODEL TN6 NPN
+(IS = 8.56E-18 BF = 120 NF = 1 VAF = 30 IKF = 10.5mA
+ ISE = 4.48E-16 BR = 10 NE = 2 VAR = 5 IKR = 922uA
+ IRB = 13.2uA RB = 291.4 RBM = 95.0 RE = 13.3 RC = 62.7
+ CJE = 29.9fF VJE = .9 MJE = .4 XTB = 0.73
+ CJC = 31.2fF VJC = .67 MJC = .32 XCJC= .3
+ CJS = 60.9fF VJS = .6 MJS = .4 FC = .9
+ TF = 8pS TR = 1nS XTF = 10 VTF = 1.4V ITF = 27.6mA
+ ISC=0 EG=1.11 XTI=5.2 PTF=0 KF=0 AF=1 NR=1 NC=2)
**************************************************************************
.MODEL TN8 NPN
+(IS = 1.18E-17 BF =120 NF = 1 VAF =30 IKF =14.6mA
+ ISE = 6.20e-16 BR =10 NE = 2 VAR = 5 IKR =1.28mA
+ IRB = 18.2uA RB = 213.1 RBM = 71.2 RE = 9.60 RC = 50.4
+ CJE = 39.9fF VJE = .9 MJE = .4 XTB = 0.73
+ CJC = 37.2fF VJC = .67 MJC = .32 XCJC = .3
+ CJS = 83.5fF VJS =.6 MJS = .4 FC = .9
+ TF = 8pS TR = 1nS XTF = 10 VTF = 1.4V ITF = 48.9mA
+ ISC = 0 EG =1.11 XTI = 5.2 PTF = 0 KF = 0 AF = 1 NR = 1 NC =2)
*** ECLinPS Lite ESD Diodes
.MODEL CBVCC D
+ ( IS = 1.00E-15 CJO = 527fF Vj = 0.545 M = 0.32 BV = 14.5
+ IBV = 0.1E-6 XTI = 5 TT = 1nS )
.MODEL CBSUB D
+ ( IS = 1.00E-15 CJO = 453fF TT = 1nS )
**************************************************************************
```

```
------------------------------------------------------------------------
Package: SO-8

* SPICE subcircuit file of coupled transmission lines
*
* Transmission line model
*
* Conductor number-pin designation cross reference:
*   Conductor     Pin
*       1           1
*       2           2
*       3           3
*       4           4
*       5           5
*       6           6
*       7           7
*       8           8
*
* number of lumps:      1
* FASTEST APPLICABLE EDGE RATE:         0.076 ns
* COMPRESSION OF SUBCIRCUITS PERFORMED: discard ratio is 0.050
* Connect chip side to N**I and board side to N**O
*
.SUBCKT LINES N01I N01O N02I N02O N03I N03O N04I N04O
+ N05I N05O N06I N06O N07I N07O N08I N08O
L01WB   N01I    N01M    1.367e-09
L01     N01M    N01O    7.794e-10
C01     N01M    0       2.445e-13
L02WB   N02I    N02M    1.287e-09
L02     N02M    N02O    5.473e-10
C02     N02M    0       1.888e-13
L03WB   N03I    N03M    1.287e-09
L03     N03M    N03O    5.473e-10
C03     N03M    0       1.901e-13
L04WB   N04I    N04M    1.367e-09
L04     N04M    N04O    7.723e-10
C04     N04M    0       2.443e-13
L05WB   N05I    N05M    1.367e-09
L05     N05M    N05O    7.710e-10
C05     N05M    0       2.478e-13
L06WB   N06I    N06M    1.287e-09
L06     N06M    N06O    5.489e-10
C06     N06M    0       1.916e-13
L07WB   N07I    N07M    1.287e-09
L07     N07M    N07O    5.495e-10
C07     N07M    0       1.930e-13
L08WB   N08I    N08M    1.367e-09
L08     N08M    N08O    7.786e-10
C08     N08M    0       2.451e-13
K0102   L01     L02     0.1687
K0102WB L01WB   L02WB   0.3400
C0102   N01O    N02O    3.674e-14
K0103   L01     L03     0.0702
K0103WB L01WB   L03WB   0.1847
K0203   L02     L03     0.1822
K0203WB L02WB   L03WB   0.3505
C0203   N02O    N03O    3.521e-14
K0204   L02     L04     0.0682
K0204WB L02WB   L04WB   0.1847
K0304   L03     L04     0.1694
K0304WB L03WB   L04WB   0.3400
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C0304   N03O    N04O    3.675e-14
K0305WB L03WB   L05WB   0.1847
K0405WB L04WB   L05WB   0.3455
K0406WB L04WB   L06WB   0.1847
K0506   L05     L06     0.1697
K0506WB L05WB   L06WB   0.3400
C0506   N05O    N06O    3.720e-14
K0507   L05     L07     0.0682
K0507WB L05WB   L07WB   0.1847
K0607   L06     L07     0.1824
K0607WB L06WB   L07WB   0.3505
C0607   N06O    N07O    3.570e-14
K0608   L06     L08     0.0702
K0608WB L06WB   L08WB   0.1847
K0708   L07     L08     0.1691
K0708WB L07WB   L08WB   0.3400
C0708   N07O    N08O    3.632e-14
.ENDS LINES
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------------------------------------------------------------------------
Package: TSSOP-8

* SPICE subcircuit file of coupled transmission lines
*
* Transmission line model
*
* Conductor number-pin designation cross reference:
* counter-clockwise
*   Conductor     Pin
*       1           1
*       2           2
*       3           3
*       4           4
*       5           5
*       6           6
*       7           7
*       8           8
*
* number of lumps:      1
* FASTEST APPLICABLE EDGE RATE:         0.048 ns
* COMPRESSION OF SUBCIRCUITS PERFORMED: discard ratio is 0.050
*
R_SHORT 0 gnd 0.0001
*
X_777 N01I N01O N02I N02O N03I N03O N04I N04O
+ N05I N05O N06I N06O N07I N07O N08I N08O gnd PACKAGE
*
.SUBCKT PACKAGE N01I N01O N02I N02O N03I N03O N04I N04O
+ N05I N05O N06I N06O N07I N07O N08I N08O gnd
R01WB   N01I    N01W    4.727e-02
L01WB   N01W    N01R    1.158e-09
R01     N01R    N01C    9.680e-04
C01     N01C    gnd     8.978e-14
L01     N01C    N01O    7.466e-10
R02WB   N02I    N02W    3.815e-02
L02WB   N02W    N02R    9.835e-10
R02     N02R    N02C    9.680e-04
C02     N02C    gnd     7.711e-14
L02     N02C    N02O    7.466e-10
R03WB   N03I    N03W    3.815e-02
L03WB   N03W    N03R    9.835e-10
R03     N03R    N03C    9.680e-04
C03     N03C    gnd     7.704e-14
L03     N03C    N03O    7.465e-10
R04WB   N04I    N04W    4.727e-02
L04WB   N04W    N04R    1.158e-09
R04     N04R    N04C    9.680e-04
C04     N04C    gnd     8.983e-14
L04     N04C    N04O    7.460e-10
R05WB   N05I    N05W    4.727e-02
L05WB   N05W    N05R    1.158e-09
R05     N05R    N05C    9.680e-04
C05     N05C    gnd     8.983e-14
L05     N05C    N05O    7.460e-10
R06WB   N06I    N06W    3.815e-02
L06WB   N06W    N06R    9.835e-10
R06     N06R    N06C    9.680e-04
C06     N06C    gnd     7.704e-14
L06     N06C    N06O    7.465e-10
R07WB   N07I    N07W    3.815e-02
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L07WB   N07W    N07R    9.835e-10
R07     N07R    N07C    9.680e-04
C07     N07C    gnd     7.711e-14
L07     N07C    N07O    7.466e-10
R08WB   N08I    N08W    4.727e-02
L08WB   N08W    N08R    1.158e-09
R08     N08R    N08C    9.680e-04
C08     N08C    gnd     8.978e-14
L08     N08C    N08O    7.466e-10
K0102   L01     L02     0.2481
K0102WB L01WB   L02WB   0.1729
C0102   N01C    N02C    2.283e-14
K0103   L01     L03     0.1067
K0103WB L01WB   L03WB   0.0598
K0104   L01     L04     0.0593
K0203   L02     L03     0.2479
K0203WB L02WB   L03WB   0.1463
C0203   N02C    N03C    2.136e-14
K0204   L02     L04     0.1068
K0204WB L02WB   L04WB   0.0598
K0304   L03     L04     0.2481
K0304WB L03WB   L04WB   0.1729
C0304   N03C    N04C    2.279e-14
K0506   L05     L06     0.2481
K0506WB L05WB   L06WB   0.1513
C0506   N05C    N06C    2.279e-14
K0507   L05     L07     0.1068
K0507WB L05WB   L07WB   0.0615
K0508   L05     L08     0.0593
K0607   L06     L07     0.2479
K0607WB L06WB   L07WB   0.1729
C0607   N06C    N07C    2.136e-14
K0608   L06     L08     0.1067
K0608WB L06WB   L08WB   0.0615
K0708   L07     L08     0.2481
K0708WB L07WB   L08WB   0.1513
C0708   N07C    N08C    2.283e-14
.ENDS PACKAGE
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----------------------------------------------------------------------
Package: SO-20

* SPICE subcircuit file of coupled transmission lines
*
* Transmission line model
*
* Conductor number-pin designation cross reference:
*   Conductor     Pin
*       1           1
*       2           2
*       3           3
*       4           4
*       5           5
*       6           6
*       7           7
*       8           8
*       9           9
*      10          10
*      11          11
*      12          12
*      13          13
*      14          14
*      15          15
*      16          16
*      17          17
*      18          18
*      19          19
*      20          20
*
* number of lumps:      1
* FASTEST APPLICABLE EDGE RATE:         0.275 ns
* COMPRESSION OF SUBCIRCUITS PERFORMED: discard ratio is 0.050
*
.SUBCKT PACKAGE N01I N01O N02I N02O N03I N03O N04I N04O
+ N05I N05O N06I N06O N07I N07O N08I N08O N09I N09O
+ N10I N10O N11I N11O N12I N12O N13I N13O N14I N14O
+ N15I N15O N16I N16O N17I N17O N18I N18O N19I N19O
+ N20I N20O BD_GND
R01WB   N01I    N01W    3.732e-02
L01WB   N01W    N01R    9.678e-10
R01     N01R    N01C    1.700e-02
C01     N01C    BD_GND  4.680e-13
L01     N01C    N01O    3.814e-09
R02WB   N02I    N02W    8.086e-02
L02WB   N02W    N02R    1.822e-09
R02     N02R    N02C    1.300e-02
C02     N02C    BD_GND  1.924e-13
L02     N02C    N02O    2.724e-09
R03WB   N03I    N03W    9.122e-02
L03WB   N03W    N03R    2.033e-09
R03     N03R    N03C    9.000e-02
C03     N03C    BD_GND  1.377e-13
L03     N03C    N03O    1.814e-09
R04WB   N04I    N04W    7.878e-02
L04WB   N04W    N04R    1.780e-09
R04     N04R    N04C    8.000e-02
C04     N04C    BD_GND  1.484e-13
L04     N04C    N04O    1.551e-09
R05WB   N05I    N05W    6.634e-02
L05WB   N05W    N05R    1.531e-09
R05     N05R    N05C    7.000e-02
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C05     N05C    BD_GND  1.635e-13
L05     N05C    N05O    1.508e-09
R06WB   N06I    N06W    6.634e-02
L06WB   N06W    N06R    1.531e-09
R06     N06R    N06C    7.000e-02
C06     N06C    BD_GND  1.584e-13
L06     N06C    N06O    1.508e-09
R07WB   N07I    N07W    7.878e-02
L07WB   N07W    N07R    1.780e-09
R07     N07R    N07C    8.000e-02
C07     N07C    BD_GND  1.476e-13
L07     N07C    N07O    1.553e-09
R08WB   N08I    N08W    4.976e-02
L08WB   N08W    N08R    1.206e-09
R08     N08R    N08C    9.000e-02
C08     N08C    BD_GND  1.322e-13
L08     N08C    N08O    1.820e-09
R09WB   N09I    N09W    8.086e-02
L09WB   N09W    N09R    1.822e-09
R09     N09R    N09C    1.300e-02
C09     N09C    BD_GND  1.864e-13
L09     N09C    N09O    2.725e-09
R10WB   N10I    N10W    7.256e-02
L10WB   N10W    N10R    1.655e-09
R10     N10R    N10C    1.700e-02
C10     N10C    BD_GND  4.681e-13
L10     N10C    N10O    3.814e-09
R11WB   N11I    N11W    3.732e-02
L11WB   N11W    N11R    9.678e-10
R11     N11R    N11C    1.700e-02
C11     N11C    BD_GND  4.761e-13
L11     N11C    N11O    3.795e-09
R12WB   N12I    N12W    8.086e-02
L12WB   N12W    N12R    1.822e-09
R12     N12R    N12C    1.300e-02
C12     N12C    BD_GND  1.888e-13
L12     N12C    N12O    2.745e-09
R13WB   N13I    N13W    9.122e-02
L13WB   N13W    N13R    2.033e-09
R13     N13R    N13C    9.000e-02
C13     N13C    BD_GND  1.346e-13
L13     N13C    N13O    1.879e-09
R14WB   N14I    N14W    7.878e-02
L14WB   N14W    N14R    1.780e-09
R14     N14R    N14C    8.000e-02
C14     N14C    BD_GND  1.496e-13
L14     N14C    N14O    1.436e-09
R15WB   N15I    N15W    6.634e-02
L15WB   N15W    N15R    1.531e-09
R15     N15R    N15C    7.000e-02
C15     N15C    BD_GND  1.550e-13
L15     N15C    N15O    1.464e-09
R16WB   N16I    N16W    6.634e-02
L16WB   N16W    N16R    1.531e-09
R16     N16R    N16C    7.000e-02
C16     N16C    BD_GND  1.568e-13
L16     N16C    N16O    1.465e-09
R17WB   N17I    N17W    7.878e-02
L17WB   N17W    N17R    1.780e-09
R17     N17R    N17C    8.000e-02
C17     N17C    BD_GND  1.492e-13
L17     N17C    N17O    1.437e-09
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R18WB   N18I    N18W    9.122e-02
L18WB   N18W    N18R    2.033e-09
R18     N18R    N18C    9.000e-02
C18     N18C    BD_GND  1.346e-13
L18     N18C    N18O    1.892e-09
R19WB   N19I    N19W    8.086e-02
L19WB   N19W    N19R    1.822e-09
R19     N19R    N19C    1.300e-02
C19     N19C    BD_GND  1.880e-13
L19     N19C    N19O    2.767e-09
R20WB   N20I    N20W    7.256e-02
L20WB   N20W    N20R    1.655e-09
R20     N20R    N20C    1.700e-02
C20     N20C    BD_GND  4.712e-13
L20     N20C    N20O    3.825e-09
K0102   L01     L02     0.4539
K0102WB L01WB   L02WB   0.1239
C0102   N01C    N02C    2.674e-13
K0103   L01     L03     0.2557
K0104   L01     L04     0.1742
K0105   L01     L05     0.1290
K0106   L01     L06     0.1011
K0107   L01     L07     0.0834
K0108   L01     L08     0.0636
K0111   L01     L11     -0.0789
K0112   L01     L12     -0.0755
K0113   L01     L13     -0.0716
K0114   L01     L14     -0.0594
K0115   L01     L15     -0.0669
K0116   L01     L16     -0.0657
K0117   L01     L17     -0.0672
K0118   L01     L18     -0.0625
K0203   L02     L03     0.3964
K0203WB L02WB   L03WB   0.1239
C0203   N02C    N03C    1.529e-13
K0204   L02     L04     0.2341
K0205   L02     L05     0.1587
K0206   L02     L06     0.1206
K0207   L02     L07     0.0974
K0208   L02     L08     0.0760
K0209   L02     L09     0.0554
K0211   L02     L11     -0.0743
K0212   L02     L12     -0.0723
K0213   L02     L13     -0.0707
K0214   L02     L14     -0.0604
K0215   L02     L15     -0.0678
K0216   L02     L16     -0.0677
K0217   L02     L17     -0.0685
K0218   L02     L18     -0.0682
K0304   L03     L04     0.3767
K0304WB L03WB   L04WB   0.1239
C0304   N03C    N04C    1.006e-13
K0305   L03     L05     0.2211
K0306   L03     L06     0.1564
K0307   L03     L07     0.1219
K0308   L03     L08     0.0956
K0309   L03     L09     0.0762
K0310   L03     L10     0.0639
K0311   L03     L11     -0.0654
K0312   L03     L12     -0.0662
K0313   L03     L13     -0.0688
K0314   L03     L14     -0.0614
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K0315   L03     L15     -0.0683
K0316   L03     L16     -0.0692
K0317   L03     L17     -0.0684
K0318   L03     L18     -0.0730
K0319   L03     L19     -0.0609
K0320   L03     L20     -0.0501
K0405   L04     L05     0.3731
K0405WB L04WB   L05WB   0.1239
C0405   N04C    N05C    8.137e-14
K0406   L04     L06     0.2290
K0407   L04     L07     0.1637
K0408   L04     L08     0.1218
K0409   L04     L09     0.0976
K0410   L04     L10     0.0836
K0411   L04     L11     -0.0645
K0412   L04     L12     -0.0673
K0413   L04     L13     -0.0722
K0414   L04     L14     -0.0658
K0415   L04     L15     -0.0724
K0416   L04     L16     -0.0733
K0417   L04     L17     -0.0708
K0418   L04     L18     -0.0763
K0419   L04     L19     -0.0673
K0420   L04     L20     -0.0597
K0506   L05     L06     0.3775
K0506WB L05WB   L06WB   0.1239
C0506   N05C    N06C    8.844e-14
K0507   L05     L07     0.2293
K0508   L05     L08     0.1565
K0509   L05     L09     0.1208
K0510   L05     L10     0.1013
K0511   L05     L11     -0.0636
K0512   L05     L12     -0.0679
K0513   L05     L13     -0.0742
K0514   L05     L14     -0.0683
K0515   L05     L15     -0.0737
K0516   L05     L16     -0.0741
K0517   L05     L17     -0.0704
K0518   L05     L18     -0.0760
K0519   L05     L19     -0.0684
K0520   L05     L20     -0.0622
K0607   L06     L07     0.3743
K0607WB L06WB   L07WB   0.1239
C0607   N06C    N07C    7.898e-14
K0608   L06     L08     0.2214
K0609   L06     L09     0.1591
K0610   L06     L10     0.1293
K0611   L06     L11     -0.0607
K0612   L06     L12     -0.0668
K0613   L06     L13     -0.0752
K0614   L06     L14     -0.0700
K0615   L06     L15     -0.0741
K0616   L06     L16     -0.0742
K0617   L06     L17     -0.0690
K0618   L06     L18     -0.0754
K0619   L06     L19     -0.0697
K0620   L06     L20     -0.0652
K0708   L07     L08     0.3762
K0708WB L07WB   L08WB   0.1239
C0708   N07C    N08C    1.016e-13
K0709   L07     L09     0.2343
K0710   L07     L10     0.1746
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K0711   L07     L11     -0.0581
K0712   L07     L12     -0.0657
K0713   L07     L13     -0.0756
K0714   L07     L14     -0.0707
K0715   L07     L15     -0.0736
K0716   L07     L16     -0.0730
K0717   L07     L17     -0.0667
K0718   L07     L18     -0.0735
K0719   L07     L19     -0.0692
K0720   L07     L20     -0.0661
K0809   L08     L09     0.3970
K0809WB L08WB   L09WB   0.1239
C0809   N08C    N09C    1.545e-13
K0810   L08     L10     0.2564
K0812   L08     L12     -0.0591
K0813   L08     L13     -0.0723
K0814   L08     L14     -0.0685
K0815   L08     L15     -0.0698
K0816   L08     L16     -0.0693
K0817   L08     L17     -0.0624
K0818   L08     L18     -0.0702
K0819   L08     L19     -0.0681
K0820   L08     L20     -0.0670
K0910   L09     L10     0.4542
K0910WB L09WB   L10WB   0.1239
C0910   N09C    N10C    2.677e-13
K0913   L09     L13     -0.0675
K0914   L09     L14     -0.0688
K0915   L09     L15     -0.0687
K0916   L09     L16     -0.0693
K0917   L09     L17     -0.0618
K0918   L09     L18     -0.0723
K0919   L09     L19     -0.0742
K0920   L09     L20     -0.0759
K1011WB L10WB   L11WB   0.1239
K1013   L10     L13     -0.0616
K1014   L10     L14     -0.0675
K1015   L10     L15     -0.0668
K1016   L10     L16     -0.0685
K1017   L10     L17     -0.0609
K1018   L10     L18     -0.0731
K1019   L10     L19     -0.0773
K1020   L10     L20     -0.0803
K1112   L11     L12     0.4562
K1112WB L11WB   L12WB   0.1239
C1112   N11C    N12C    2.679e-13
K1113   L11     L13     0.2725
K1114   L11     L14     0.1533
K1115   L11     L15     0.1161
K1116   L11     L16     0.0901
K1117   L11     L17     0.0702
K1118   L11     L18     0.0567
K1213   L12     L13     0.4103
K1213WB L12WB   L13WB   0.1239
C1213   N12C    N13C    1.538e-13
K1214   L12     L14     0.2091
K1215   L12     L15     0.1398
K1216   L12     L16     0.1055
K1217   L12     L17     0.0812
K1218   L12     L18     0.0684
K1314   L13     L14     0.3577
K1314WB L13WB   L14WB   0.1239
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C1314   N13C    N14C    1.026e-13
K1315   L13     L15     0.2088
K1316   L13     L16     0.1474
K1317   L13     L17     0.1074
K1318   L13     L18     0.0930
K1319   L13     L19     0.0693
K1320   L13     L20     0.0578
K1415   L14     L15     0.3383
K1415WB L14WB   L15WB   0.1239
C1415   N14C    N15C    7.843e-14
K1416   L14     L16     0.1987
K1417   L14     L17     0.1302
K1418   L14     L18     0.1078
K1419   L14     L19     0.0825
K1420   L14     L20     0.0715
K1516   L15     L16     0.3631
K1516WB L15WB   L16WB   0.1239
C1516   N15C    N16C    9.179e-14
K1517   L15     L17     0.1988
K1518   L15     L18     0.1480
K1519   L15     L19     0.1072
K1520   L15     L20     0.0918
K1617   L16     L17     0.3380
K1617WB L16WB   L17WB   0.1239
C1617   N16C    N17C    7.810e-14
K1618   L16     L18     0.2096
K1619   L16     L19     0.1419
K1620   L16     L20     0.1183
K1718   L17     L18     0.3595
K1718WB L17WB   L18WB   0.1239
C1718   N17C    N18C    1.034e-13
K1719   L17     L19     0.2122
K1720   L17     L20     0.1565
K1819   L18     L19     0.4140
K1819WB L18WB   L19WB   0.1239
C1819   N18C    N19C    1.536e-13
K1820   L18     L20     0.2766
K1920   L19     L20     0.4603
K1920WB L19WB   L20WB   0.1239
C1920   N19C    N20C    2.679e-13
.ENDS PACKAGE
--------------------------------------------------------------------------
```

```
----------------------------------------------------------------------
Package: TSSOP-20

* SPICE subcircuit file of coupled transmission lines
*
* Transmission line model
*
* Conductor number-pin designation cross reference:
*   Conductor     Pin
*       1           1
*       2           2
*       3           3
*       4           4
*       5           5
*       6           6
*       7           7
*       8           8
*       9           9
*      10          10
*      11          11
*      12          12
*      13          13
*      14          14
*      15          15
*      16          16
*      17          17
*      18          18
*      19          19
*      20          20
*
* number of lumps: 1
* FASTEST APPLICABLE EDGE RATE:  0.114 ns
* Equivalent bandwidth:                3.07GHz
* COMPRESSION OF SUBCIRCUITS PERFORMED: discard ratio is 0.050
*
**CONNECT CHIP SIDE TO N**I AND BOARD SIDE TO N**O
* ECLinPS PLUS usage requires the input nodes used in the subcircuit call
* statement(X_777) that are tied to global ports(VCC, VCCO, and VEE internal
* to the die) to have the same global names in the subcircuit call statement(X_777).
* For example, if VCC is wirebonded to pin 20 for a certain design, then N20I
* should be relabeled to VCC.  Again, the change needs only to be incorporated
* in the X_777 subcircuit callout statement.  Since this requires a change to
* the netlist below, it is necessary for each design to have a copy of this file with
* the appropriate changes made that are required for that design.
*
R_SHORT 0 gnd 0.0001
X_777 N01I N01O N02I N02O N03I N03O N04I N04O
+ N05I N05O N06I N06O N07I N07O N08I N08O N09I N09O
+ N10I N10O N11I N11O N12I N12O N13I N13O N14I N14O
+ N15I N15O N16I N16O N17I N17O N18I N18O N19I N19O
+ N20I N20O gnd PACKAGE
.SUBCKT PACKAGE N01I N01O N02I N02O N03I N03O N04I N04O
+ N05I N05O N06I N06O N07I N07O N08I N08O N09I N09O
+ N10I N10O N11I N11O N12I N12O N13I N13O N14I N14O
+ N15I N15O N16I N16O N17I N17O N18I N18O N19I N19O
+ N20I N20O gnd
R01WB N01I N01W 5.225e-02
L01WB N01W N01R 1.254e-09
R01 N01R N01C 2.100e-03
C01 N01C gnd 1.840e-13
L01 N01C N01O 1.603e-09
```

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R02WB N02I N02W 5.473e-02
L02WB N02W N02R 1.303e-09
R02 N02R N02C 2.500e-03
C02 N02C gnd 8.995e-14
L02 N02C N02O 1.187e-09
R03WB N03I N03W 5.266e-02
L03WB N03W N03R 1.262e-09
R03 N03R N03C 2.500e-03
C03 N03C gnd 7.204e-14
L03 N03C N03O 9.073e-10
R04WB N04I N04W 3.690e-02
L04WB N04W N04R 9.599e-10
R04 N04R N04C 2.100e-03
C04 N04C gnd 8.838e-14
L04 N04C N04O 9.053e-10
R05WB N05I N05W 3.151e-02
L05WB N05W N05R 8.581e-10
R05 N05R N05C 1.700e-03
C05 N05C gnd 9.879e-14
L05 N05C N05O 9.065e-10
R06WB N06I N06W 3.151e-02
L06WB N06W N06R 8.581e-10
R06 N06R N06C 1.700e-03
C06 N06C gnd 9.879e-14
L06 N06C N06O 9.065e-10
R07WB N07I N07W 3.690e-02
L07WB N07W N07R 9.599e-10
R07 N07R N07C 2.100e-03
C07 N07C gnd 8.838e-14
L07 N07C N07O 9.053e-10
R08WB N08I N08W 5.266e-02
L08WB N08W N08R 1.262e-09
R08 N08R N08C 2.500e-03
C08 N08C gnd 7.204e-14
L08 N08C N08O 9.073e-10
R09WB N09I N09W 5.473e-02
L09WB N09W N09R 1.303e-09
R09 N09R N09C 2.500e-03
C09 N09C gnd 8.995e-14
L09 N09C N09O 1.187e-09
R10WB N10I N10W 5.225e-02
L10WB N10W N10R 1.254e-09
R10 N10R N10C 2.100e-03
C10 N10C gnd 1.840e-13
L10 N10C N10O 1.603e-09
R11WB N11I N11W 5.225e-02
L11WB N11W N11R 1.254e-09
R11 N11R N11C 2.100e-03
C11 N11C gnd 1.840e-13
L11 N11C N11O 1.603e-09
R12WB N12I N12W 5.473e-02
L12WB N12W N12R 1.303e-09
R12 N12R N12C 2.500e-03
C12 N12C gnd 8.995e-14
L12 N12C N12O 1.187e-09
R13WB N13I N13W 5.266e-02
L13WB N13W N13R 1.262e-09
R13 N13R N13C 2.500e-03
C13 N13C gnd 7.204e-14
L13 N13C N13O 9.073e-10
R14WB N14I N14W 3.690e-02
L14WB N14W N14R 9.599e-10
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R14 N14R N14C 2.100e-03
C14 N14C gnd 8.838e-14
L14 N14C N14O 9.053e-10
R15WB N15I N15W 3.151e-02
L15WB N15W N15R 8.581e-10
R15 N15R N15C 1.700e-03
C15 N15C gnd 9.879e-14
L15 N15C N15O 9.065e-10
R16WB N16I N16W 3.151e-02
L16WB N16W N16R 8.581e-10
R16 N16R N16C 1.700e-03
C16 N16C gnd 9.879e-14
L16 N16C N16O 9.065e-10
R17WB N17I N17W 3.690e-02
L17WB N17W N17R 9.599e-10
R17 N17R N17C 2.100e-03
C17 N17C gnd 8.838e-14
L17 N17C N17O 9.053e-10
R18WB N18I N18W 5.266e-02
L18WB N18W N18R 1.262e-09
R18 N18R N18C 2.500e-03
C18 N18C gnd 7.204e-14
L18 N18C N18O 9.073e-10
R19WB N19I N19W 5.473e-02
L19WB N19W N19R 1.303e-09
R19 N19R N19C 2.500e-03
C19 N19C gnd 8.995e-14
L19 N19C N19O 1.187e-09
R20WB N20I N20W 5.225e-02
L20WB N20W N20R 1.254e-09
R20 N20R N20C 2.100e-03
C20 N20C gnd 1.840e-13
L20 N20C N20O 1.603e-09
K0102 L01 L02 0.2780
K0102WB L01WB L02WB 0.2168
C0102 N01C N02C 1.222e-13
K0103 L01 L03 0.1016
K0103WB L01WB L03WB 0.0788
K0104 L01 L04 0.0559
K0120WB L01WB L20WB 0.1061
K0119WB L01WB L19WB 0.0542
K0203 L02 L03 0.2333
K0203WB L02WB L03WB 0.1970
C0203 N02C N03C 7.150e-14
K0204 L02 L04 0.1006
K0204WB L02WB L04WB 0.0729
K0205 L02 L05 0.0577
K0220WB L02WB L20WB 0.0542
K0304 L03 L04 0.2384
K0304WB L03WB L04WB 0.1787
C0304 N03C N04C 5.860e-14
K0305 L03 L05 0.1055
K0305WB L03WB L05WB 0.0542
K0306 L03 L06 0.0577
K0405 L04 L05 0.2370
K0405WB L04WB L05WB 0.1281
C0405 N04C N05C 5.812e-14
K0406 L04 L06 0.0939
K0407 L04 L07 0.0583
K0506 L05 L06 0.1951
K0506WB L05WB L06WB 0.0908
C0506 N05C N06C 3.558e-14
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K0507 L05 L07 0.0939
K0508 L05 L08 0.0577
K0607 L06 L07 0.2370
K0607WB L06WB L07WB 0.1281
C0607 N06C N07C 5.812e-14
K0608 L06 L08 0.1055
K0608WB L06WB L08WB 0.0542
K0609 L06 L09 0.0577
K0708 L07 L08 0.2384
K0708WB L07WB L08WB 0.1787
C0708 N07C N08C 5.860e-14
K0709 L07 L09 0.1006
K0709WB L07WB L09WB 0.0729
K0710 L07 L10 0.0559
K0809 L08 L09 0.2333
K0809WB L08WB L09WB 0.1970
C0809 N08C N09C 7.150e-14
K0810 L08 L10 0.1016
K0810WB L08WB L10WB 0.0788
K0910 L09 L10 0.2780
K0910WB L09WB L10WB 0.2168
C0910 N09C N10C 1.222e-13
K0911WB L09WB L11WB 0.0542
K1011WB L10WB L11WB 0.1061
K1012WB L10WB L12WB 0.0542
K1112 L11 L12 0.2780
K1112WB L11WB L12WB 0.2168
C1112 N11C N12C 1.222e-13
K1113 L11 L13 0.1016
K1113WB L11WB L13WB 0.0788
K1114 L11 L14 0.0559
K1213 L12 L13 0.2333
K1213WB L12WB L13WB 0.1970
C1213 N12C N13C 7.150e-14
K1214 L12 L14 0.1006
K1214WB L12WB L14WB 0.0729
K1215 L12 L15 0.0577
K1314 L13 L14 0.2384
K1314WB L13WB L14WB 0.1787
C1314 N13C N14C 5.860e-14
K1315 L13 L15 0.1055
K1315WB L13WB L15WB 0.0542
K1316 L13 L16 0.0577
K1415 L14 L15 0.2370
K1415WB L14WB L15WB 0.1281
C1415 N14C N15C 5.812e-14
K1416 L14 L16 0.0939
K1417 L14 L17 0.0583
K1516 L15 L16 0.1951
K1516WB L15WB L16WB 0.0908
C1516 N15C N16C 3.558e-14
K1517 L15 L17 0.0939
K1518 L15 L18 0.0577
K1617 L16 L17 0.2370
K1617WB L16WB L17WB 0.1281
C1617 N16C N17C 5.812e-14
K1618 L16 L18 0.1055
K1618WB L16WB L18WB 0.0542
K1619 L16 L19 0.0577
K1718 L17 L18 0.2384
K1718WB L17WB L18WB 0.1787
C1718 N17C N18C 5.860e-14
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K1719 L17 L19 0.1006
K1719WB L17WB L19WB 0.0729
K1720 L17 L20 0.0559
K1819 L18 L19 0.2333
K1819WB L18WB L19WB 0.1970
C1819 N18C N19C 7.150e-14
K1820 L18 L20 0.1016
K1820WB L18WB L20WB 0.0788
K1920 L19 L20 0.2780
K1920WB L19WB L20WB 0.2168
C1920 N19C N20C 1.222e-13
.ENDS PACKAGE
--------------------------------------------------------------------------
```

```
------------------------------------------------------------------
Package: 32-TQFP

* SPICE subcircuit file of coupled transmission lines
*
* Transmission line model
*
* Conductor number-pin designation cross reference:
*   Conductor     Pin
*       1           1
*       2           2
*       3           3
*       4           4
*       5           5
*       6           6
*       7           7
*       8           8
*       9           9
*      10          10
*      11          11
*      12          12
*      13          13
*      14          14
*      15          15
*      16          16
*      17          17
*      18          18
*      19          19
*      20          20
*      21          21
*      22          22
*      23          23
*      24          24
*      25          25
*      26          26
*      27          27
*      28          28
*      29          29
*      30          30
*      31          31
*      32          32
*
* number of lumps: 1
* FASTEST APPLICABLE EDGE RATE:  0.135 ns
* Equivalent bandwidth:                 2.6   GHz
* COMPRESSION OF SUBCIRCUITS PERFORMED: discard ratio is 0.050
*
**CONNECT CHIP SIDE TO N**I AND BOARD SIDE TO N**O
* ECLinPS PLUS usage requires the input nodes used in the subcircuit call
* statement(X_777) that are tied to global ports(VCC, VCCO, and VEE internal
* to the die) to have the same global names in the subcircuit call statement(X_777).
* For example, if VCC is wirebonded to pin 1, 9, 16, and 32 for a certain design, then
* N01I, N09I, N16I, and N32I should be relabeled to VCC.  Again, the change needs only to
* be incorporated in the X_777 subcircuit callout statement.  Since this requires a change
* to the netlist below, it is necessary for each design to have a copy of this file with
* the appropriate changes made that are required for that design.
*
R_SHORT 0 ground 0.0001
*
X_777 N01I N01O N02I N02O N03I N03O N04I N04O
+ N05I N05O N06I N06O N07I N07O N08I N08O N09I N09O
+ N10I N10O N11I N11O N12I N12O N13I N13O N14I N14O
```

```
+ N15I N15O N16I N16O N17I N17O N18I N18O N19I N19O
+ N20I N20O N21I N21O N22I N22O N23I N23O N24I N24O
+ N25I N25O N26I N26O N27I N27O N28I N28O N29I N29O
+ N30I N30O N31I N31O N32I N32O ground PACKAGE
*
.SUBCKT PACKAGE N01I N01O N02I N02O N03I N03O N04I N04O
+ N05I N05O N06I N06O N07I N07O N08I N08O N09I N09O
+ N10I N10O N11I N11O N12I N12O N13I N13O N14I N14O
+ N15I N15O N16I N16O N17I N17O N18I N18O N19I N19O
+ N20I N20O N21I N21O N22I N22O N23I N23O N24I N24O
+ N25I N25O N26I N26O N27I N27O N28I N28O N29I N29O
+ N30I N30O N31I N31O N32I N32O ground
*
R01WB N01I N01W 5.432e-02
L01WB N01W N01R 1.295e-09
R01 N01R N01C 1.560e-03
C01 N01C ground 2.813e-13
L01 N01C N01O 1.584e-09
R02WB N02I N02W 4.976e-02
L02WB N02W N02R 1.206e-09
R02 N02R N02C 1.330e-03
C02 N02C ground 1.308e-13
L02 N02C N02O 1.437e-09
R03WB N03I N03W 4.810e-02
L03WB N03W N03R 1.174e-09
R03 N03R N03C 1.170e-03
C03 N03C ground 1.235e-13
L03 N03C N03O 1.321e-09
R04WB N04I N04W 4.561e-02
L04WB N04W N04R 1.126e-09
R04 N04R N04C 1.100e-03
C04 N04C ground 1.207e-13
L04 N04C N04O 1.259e-09
R05WB N05I N05W 4.561e-02
L05WB N05W N05R 1.126e-09
R05 N05R N05C 1.100e-03
C05 N05C ground 1.207e-13
L05 N05C N05O 1.259e-09
R06WB N06I N06W 4.810e-02
L06WB N06W N06R 1.174e-09
R06 N06R N06C 1.170e-03
C06 N06C ground 1.235e-13
L06 N06C N06O 1.321e-09
R07WB N07I N07W 4.976e-02
L07WB N07W N07R 1.206e-09
R07 N07R N07C 1.330e-03
C07 N07C ground 1.308e-13
L07 N07C N07O 1.437e-09
R08WB N08I N08W 5.432e-02
L08WB N08W N08R 1.295e-09
R08 N08R N08C 1.560e-03
C08 N08C ground 2.813e-13
L08 N08C N08O 1.584e-09
R09WB N09I N09W 5.432e-02
L09WB N09W N09R 1.295e-09
R09 N09R N09C 1.560e-03
C09 N09C ground 2.813e-13
L09 N09C N09O 1.584e-09
R10WB N10I N10W 4.976e-02
L10WB N10W N10R 1.206e-09
R10 N10R N10C 1.330e-03
C10 N10C ground 1.308e-13
```

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L10 N10C N10O 1.437e-09
R11WB N11I N11W 4.810e-02
L11WB N11W N11R 1.174e-09
R11 N11R N11C 1.170e-03
C11 N11C ground 1.235e-13
L11 N11C N11O 1.321e-09
R12WB N12I N12W 4.561e-02
L12WB N12W N12R 1.126e-09
R12 N12R N12C 1.100e-03
C12 N12C ground 1.207e-13
L12 N12C N12O 1.259e-09
R13WB N13I N13W 4.561e-02
L13WB N13W N13R 1.126e-09
R13 N13R N13C 1.100e-03
C13 N13C ground 1.207e-13
L13 N13C N13O 1.259e-09
R14WB N14I N14W 4.810e-02
L14WB N14W N14R 1.174e-09
R14 N14R N14C 1.170e-03
C14 N14C ground 1.235e-13
L14 N14C N14O 1.321e-09
R15WB N15I N15W 4.976e-02
L15WB N15W N15R 1.206e-09
R15 N15R N15C 1.330e-03
C15 N15C ground 1.308e-13
L15 N15C N15O 1.437e-09
R16WB N16I N16W 5.432e-02
L16WB N16W N16R 1.295e-09
R16 N16R N16C 1.560e-03
C16 N16C ground 2.813e-13
L16 N16C N16O 1.584e-09
R17WB N17I N17W 5.432e-02
L17WB N17W N17R 1.295e-09
R17 N17R N17C 1.560e-03
C17 N17C ground 2.813e-13
L17 N17C N17O 1.584e-09
R18WB N18I N18W 4.976e-02
L18WB N18W N18R 1.206e-09
R18 N18R N18C 1.330e-03
C18 N18C ground 1.308e-13
L18 N18C N18O 1.437e-09
R19WB N19I N19W 4.810e-02
L19WB N19W N19R 1.174e-09
R19 N19R N19C 1.170e-03
C19 N19C ground 1.235e-13
L19 N19C N19O 1.321e-09
R20WB N20I N20W 4.561e-02
L20WB N20W N20R 1.126e-09
R20 N20R N20C 1.100e-03
C20 N20C ground 1.207e-13
L20 N20C N20O 1.259e-09
R21WB N21I N21W 4.561e-02
L21WB N21W N21R 1.126e-09
R21 N21R N21C 1.100e-03
C21 N21C ground 1.207e-13
L21 N21C N21O 1.259e-09
R22WB N22I N22W 4.810e-02
L22WB N22W N22R 1.174e-09
R22 N22R N22C 1.170e-03
C22 N22C ground 1.235e-13
L22 N22C N22O 1.321e-09
R23WB N23I N23W 4.976e-02
```

```
L23WB N23W N23R 1.206e-09
R23 N23R N23C 1.330e-03
C23 N23C ground 1.308e-13
L23 N23C N23O 1.437e-09
R24WB N24I N24W 5.432e-02
L24WB N24W N24R 1.295e-09
R24 N24R N24C 1.560e-03
C24 N24C ground 2.813e-13
L24 N24C N24O 1.584e-09
R25WB N25I N25W 5.432e-02
L25WB N25W N25R 1.295e-09
R25 N25R N25C 1.560e-03
C25 N25C ground 2.813e-13
L25 N25C N25O 1.584e-09
R26WB N26I N26W 4.976e-02
L26WB N26W N26R 1.206e-09
R26 N26R N26C 1.330e-03
C26 N26C ground 1.308e-13
L26 N26C N26O 1.437e-09
R27WB N27I N27W 4.810e-02
L27WB N27W N27R 1.174e-09
R27 N27R N27C 1.170e-03
C27 N27C ground 1.235e-13
L27 N27C N27O 1.321e-09
R28WB N28I N28W 4.561e-02
L28WB N28W N28R 1.126e-09
R28 N28R N28C 1.100e-03
C28 N28C ground 1.207e-13
L28 N28C N28O 1.259e-09
R29WB N29I N29W 4.561e-02
L29WB N29W N29R 1.126e-09
R29 N29R N29C 1.100e-03
C29 N29C ground 1.207e-13
L29 N29C N29O 1.259e-09
R30WB N30I N30W 4.810e-02
L30WB N30W N30R 1.174e-09
R30 N30R N30C 1.170e-03
C30 N30C ground 1.235e-13
L30 N30C N30O 1.321e-09
R31WB N31I N31W 4.976e-02
L31WB N31W N31R 1.206e-09
R31 N31R N31C 1.330e-03
C31 N31C ground 1.308e-13
L31 N31C N31O 1.437e-09
R32WB N32I N32W 5.432e-02
L32WB N32W N32R 1.295e-09
R32 N32R N32C 1.560e-03
C32 N32C ground 2.813e-13
L32 N32C N32O 1.584e-09
K0102 L01 L02 0.3413
K0102WB L01WB L02WB 0.2544
C0102 N01C N02C 1.426e-13
K0103 L01 L03 0.1426
K0103WB L01WB L03WB 0.1061
K0104 L01 L04 0.0720
K0104WB L01WB L04WB 0.0674
K0130 L01 L30 0.0607
K0131 L01 L31 0.1053
K0131WB L01WB L31WB 0.0799
K0132 L01 L32 0.1899
K0132WB L01WB L32WB 0.1729
K0203 L02 L03 0.3211
```

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K0203WB L02WB L03WB 0.2628
C0203 N02C N03C 1.205e-13
K0204 L02 L04 0.1333
K0204WB L02WB L04WB 0.1162
K0205 L02 L05 0.0701
K0205WB L02WB L05WB 0.0697
K0231 L02 L31 0.0706
K0232 L02 L32 0.1053
K0232WB L02WB L32WB 0.0799
K0304 L03 L04 0.3070
K0304WB L03WB L04WB 0.2809
C0304 N03C N04C 1.038e-13
K0305 L03 L05 0.1301
K0305WB L03WB L05WB 0.1200
K0306 L03 L06 0.0683
K0306WB L03WB L06WB 0.0719
K0332 L03 L32 0.0607
K0405 L04 L05 0.3070
K0405WB L04WB L05WB 0.2717
C0405 N04C N05C 1.041e-13
K0406 L04 L06 0.1301
K0406WB L04WB L06WB 0.1200
K0407 L04 L07 0.0701
K0407WB L04WB L07WB 0.0697
K0506 L05 L06 0.3070
K0506WB L05WB L06WB 0.2809
C0506 N05C N06C 1.038e-13
K0507 L05 L07 0.1333
K0507WB L05WB L07WB 0.1162
K0508 L05 L08 0.0720
K0508WB L05WB L08WB 0.0674
K0607 L06 L07 0.3211
K0607WB L06WB L07WB 0.2628
C0607 N06C N07C 1.205e-13
K0608 L06 L08 0.1426
K0608WB L06WB L08WB 0.1061
K0609 L06 L09 0.0607
K0708 L07 L08 0.3413
K0708WB L07WB L08WB 0.2544
C0708 N07C N08C 1.426e-13
K0709 L07 L09 0.1053
K0709WB L07WB L09WB 0.0799
K0710 L07 L10 0.0706
K0809 L08 L09 0.1899
K0809WB L08WB L09WB 0.1729
K0810 L08 L10 0.1053
K0810WB L08WB L10WB 0.0799
K0811 L08 L11 0.0607
K0910 L09 L10 0.3413
K0910WB L09WB L10WB 0.2544
C0910 N09C N10C 1.426e-13
K0911 L09 L11 0.1426
K0911WB L09WB L11WB 0.1061
K0912 L09 L12 0.0720
K0912WB L09WB L12WB 0.0674
K1011 L10 L11 0.3211
K1011WB L10WB L11WB 0.2628
C1011 N10C N11C 1.205e-13
K1012 L10 L12 0.1333
K1012WB L10WB L12WB 0.1162
K1013 L10 L13 0.0701
K1013WB L10WB L13WB 0.0697
```

```
K1112 L11 L12 0.3070
K1112WB L11WB L12WB 0.2809
C1112 N11C N12C 1.038e-13
K1113 L11 L13 0.1301
K1113WB L11WB L13WB 0.1200
K1114 L11 L14 0.0683
K1114WB L11WB L14WB 0.0719
K1213 L12 L13 0.3070
K1213WB L12WB L13WB 0.2717
C1213 N12C N13C 1.041e-13
K1214 L12 L14 0.1301
K1214WB L12WB L14WB 0.1200
K1215 L12 L15 0.0701
K1215WB L12WB L15WB 0.0697
K1314 L13 L14 0.3070
K1314WB L13WB L14WB 0.2809
C1314 N13C N14C 1.038e-13
K1315 L13 L15 0.1333
K1315WB L13WB L15WB 0.1162
K1316 L13 L16 0.0720
K1316WB L13WB L16WB 0.0674
K1415 L14 L15 0.3211
K1415WB L14WB L15WB 0.2628
C1415 N14C N15C 1.205e-13
K1416 L14 L16 0.1426
K1416WB L14WB L16WB 0.1061
K1417 L14 L17 0.0607
K1516 L15 L16 0.3413
K1516WB L15WB L16WB 0.2544
C1516 N15C N16C 1.426e-13
K1517 L15 L17 0.1053
K1517WB L15WB L17WB 0.0799
K1518 L15 L18 0.0706
K1617 L16 L17 0.1899
K1617WB L16WB L17WB 0.1729
K1618 L16 L18 0.1053
K1618WB L16WB L18WB 0.0799
K1619 L16 L19 0.0607
K1718 L17 L18 0.3413
K1718WB L17WB L18WB 0.2544
C1718 N17C N18C 1.426e-13
K1719 L17 L19 0.1426
K1719WB L17WB L19WB 0.1061
K1720 L17 L20 0.0720
K1720WB L17WB L20WB 0.0674
K1819 L18 L19 0.3211
K1819WB L18WB L19WB 0.2628
C1819 N18C N19C 1.205e-13
K1820 L18 L20 0.1333
K1820WB L18WB L20WB 0.1162
K1821 L18 L21 0.0701
K1821WB L18WB L21WB 0.0697
K1920 L19 L20 0.3070
K1920WB L19WB L20WB 0.2809
C1920 N19C N20C 1.038e-13
K1921 L19 L21 0.1301
K1921WB L19WB L21WB 0.1200
K1922 L19 L22 0.0683
K1922WB L19WB L22WB 0.0719
K2021 L20 L21 0.3070
K2021WB L20WB L21WB 0.2717
C2021 N20C N21C 1.041e-13
```

```
K2022 L20 L22 0.1301
K2022WB L20WB L22WB 0.1200
K2023 L20 L23 0.0701
K2023WB L20WB L23WB 0.0697
K2122 L21 L22 0.3070
K2122WB L21WB L22WB 0.2809
C2122 N21C N22C 1.038e-13
K2123 L21 L23 0.1333
K2123WB L21WB L23WB 0.1162
K2124 L21 L24 0.0720
K2124WB L21WB L24WB 0.0674
K2223 L22 L23 0.3211
K2223WB L22WB L23WB 0.2628
C2223 N22C N23C 1.205e-13
K2224 L22 L24 0.1426
K2224WB L22WB L24WB 0.1061
K2225 L22 L25 0.0607
K2324 L23 L24 0.3413
K2324WB L23WB L24WB 0.2544
C2324 N23C N24C 1.426e-13
K2325 L23 L25 0.1053
K2325WB L23WB L25WB 0.0799
K2326 L23 L26 0.0706
K2425 L24 L25 0.1899
K2425WB L24WB L25WB 0.1729
K2426 L24 L26 0.1053
K2426WB L24WB L26WB 0.0799
K2427 L24 L27 0.0607
K2526 L25 L26 0.3413
K2526WB L25WB L26WB 0.2544
C2526 N25C N26C 1.426e-13
K2527 L25 L27 0.1426
K2527WB L25WB L27WB 0.1061
K2528 L25 L28 0.0720
K2528WB L25WB L28WB 0.0674
K2627 L26 L27 0.3211
K2627WB L26WB L27WB 0.2628
C2627 N26C N27C 1.205e-13
K2628 L26 L28 0.1333
K2628WB L26WB L28WB 0.1162
K2629 L26 L29 0.0701
K2629WB L26WB L29WB 0.0697
K2728 L27 L28 0.3070
K2728WB L27WB L28WB 0.2809
C2728 N27C N28C 1.038e-13
K2729 L27 L29 0.1301
K2729WB L27WB L29WB 0.1200
K2730 L27 L30 0.0683
K2730WB L27WB L30WB 0.0719
K2829 L28 L29 0.3070
K2829WB L28WB L29WB 0.2717
C2829 N28C N29C 1.041e-13
K2830 L28 L30 0.1301
K2830WB L28WB L30WB 0.1200
K2831 L28 L31 0.0701
K2831WB L28WB L31WB 0.0697
K2930 L29 L30 0.3070
K2930WB L29WB L30WB 0.2809
C2930 N29C N30C 1.038e-13
K2931 L29 L31 0.1333
K2931WB L29WB L31WB 0.1162
K2932 L29 L32 0.0720
```

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K2932WB L29WB L32WB 0.0674
K3031 L30 L31 0.3211
K3031WB L30WB L31WB 0.2628
C3031 N30C N31C 1.205e-13
K3032 L30 L32 0.1426
K3032WB L30WB L32WB 0.1061
K3132 L31 L32 0.3413
K3132WB L31WB L32WB 0.2544
C3132 N31C N32C 1.426e-13
.ENDS PACKAGE
--------------------------------------------------------------------
```

```
*******************************************************
**********           Package Models          ***********
*                                                     *
*                                                     *
* Package Model (28-lead PLCC)                        *
* EXT = (External Input to Pin)                       *
* INT = (Internal Output of the Pin) GND = (0V         *
*******************************************************
.SUBCKT PKG28 EXT INT GND
CPKG 82 GND 1.5PF
RPKG1 EXT 82 750
RPKG2 82 83 750
RPKG3 83 INT .2
LPKG1 EXT 82 3.5NH
LPKG2 82 83 3.5NH
.ENDS PKG2
*************************************************************************
* Package Model (52-lead TQFP)                        *
EXT = (External Input to Pin) INT = (Internal Output of the Pin) GND = (0V)
*************************************************************************
.SUBCKT PKG52 EXT INT GND
CPKG 82 GND 2.0PF
RPKG1 EXT 82 750
RPKG2 82 83 750
RPKG3 83 INT 0.2
LPKG1 EXT 82 1.0NH
LPKG2 82 83 1.0NH
.ENDS PKG52
```

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