High-Current Complementary Silicon Power Transistors

2N5684 (PNP), 2N5686 (NPN)

These packages are designed for use in high−power amplifier and switching circuit applications.

Features

- High Current Capability − I_C Continuous = 50 Amperes
- DC Current Gain − h_{FE} = 15−60 @ I_C = 25 Adc
- Low Collector−Emitter Saturation Voltage − $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 25 Adc
- Pb−Free Packages are Available*

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	80	Vdc
Collector−Base Voltage	V_{CB}	80	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current − Continuous	I_C	50	Adc
Base Current	I_B	15	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.715	mW mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	θ_{JC}	0.584	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Indicates JEDEC Registered Data.

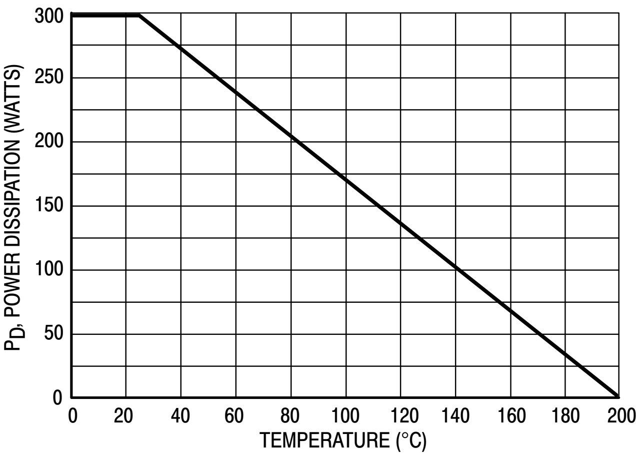
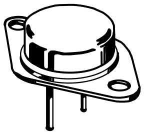


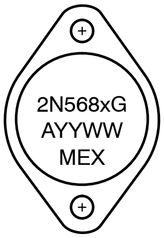
Figure 1. Power Derating

Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

50 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60−80 VOLTS, 300 WATTS

MARKING DIAGRAM





TO−204 (TO−3)
CASE 197A
STYLE 1

2N568x = Device Code
x = 4 or 6
G = Pb−Free Package
A = Location Code
YY = Year
WW = Work Week
MEX = Country of Orgin

ORDERING INFORMATION

Device	Package	Shipping
2N5684G	TO−3 (Pb−Free)	100 Units/Tray
2N5686	TO−3	100 Units/Tray
2N5686G	TO−3 (Pb−Free)	100 Units/Tray

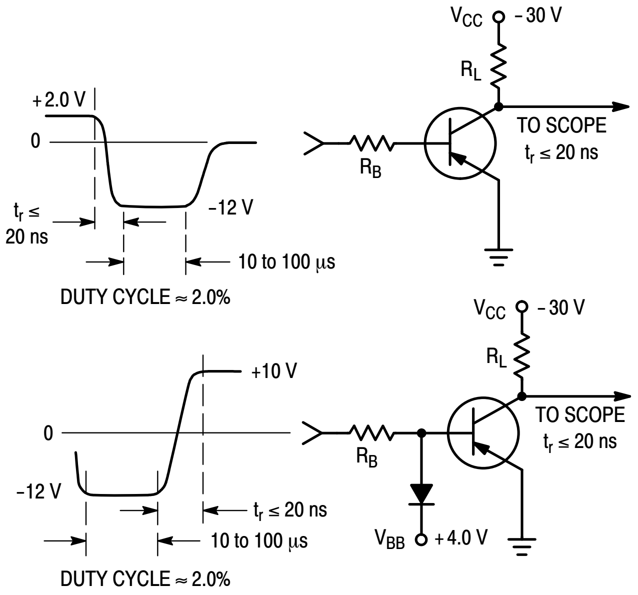
*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (Note 2)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 3) (I_C = 0.2 Adc, I_B = 0)	$V_{CEO(sus)}$	80	–	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0)	I_{CEO}	–	1.0	mAdc
Collector Cutoff Current (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 – –	 2.0 10	mAdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	–	2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (Note 3) (I_C = 25 Adc, V_{CE} = 2.0 Vdc) (I_C = 50 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	 15 5.0	 60 –	–
Collector−Emitter Saturation Voltage (Note 3) (I_C = 25 Adc, I_B = 2.5 Adc) (I_C = 50 Adc, I_B = 10 Adc)	$V_{CE(sat)}$	 – –	 1.0 5.0	Vdc
Base−Emitter Saturation Voltage (Note 2) (I_C = 25 Adc, I_B = 2.5 Adc)	$V_{BE(sat)}$	–	2.0	Vdc
Base−Emitter On Voltage (Note 2) (I_C = 25 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain − Bandwidth Product (I_C = 5.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.0	–	MHz
Output Capacitance 2N5684 (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) 2N5686	C_{ob}	– –	2000 1200	pF
Small−Signal Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	h_{fe}	15	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Indicates JEDEC Registered Data.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

Figure 2. Switching Time Test Circuit

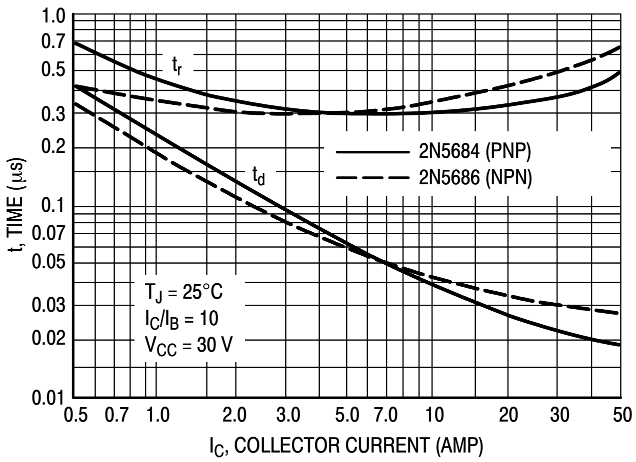


Figure 3. Turn−On Time

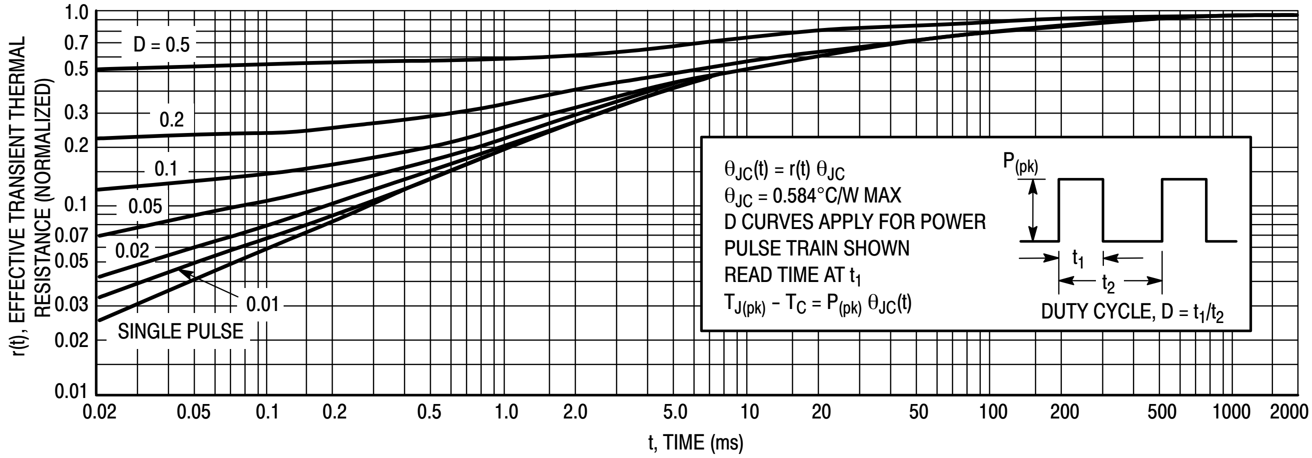


Figure 4. Thermal Response

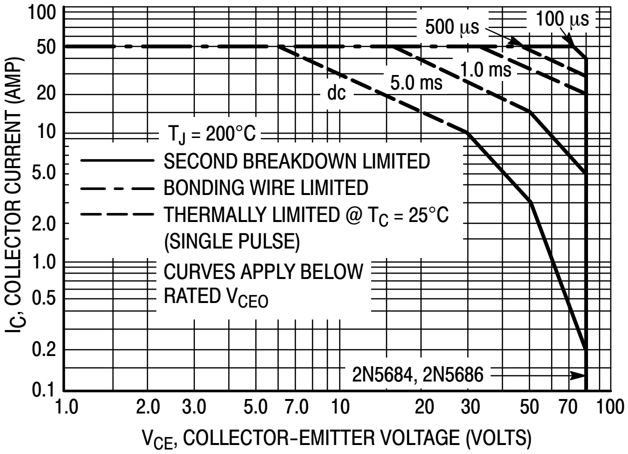


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

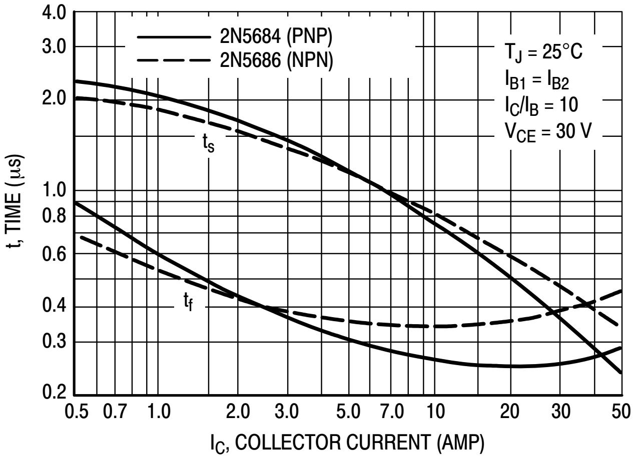


Figure 6. Turn−Off Time

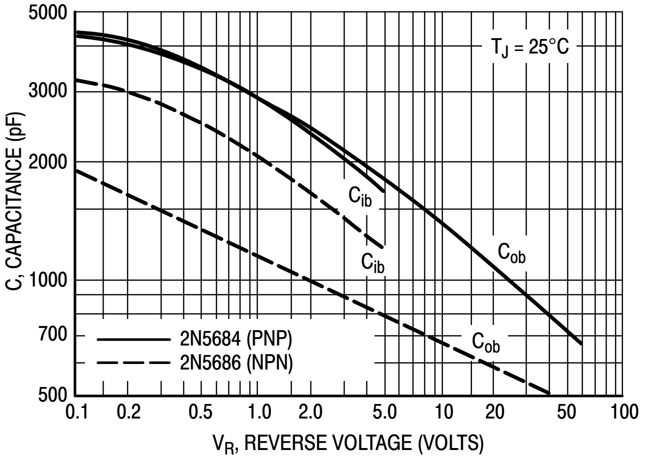
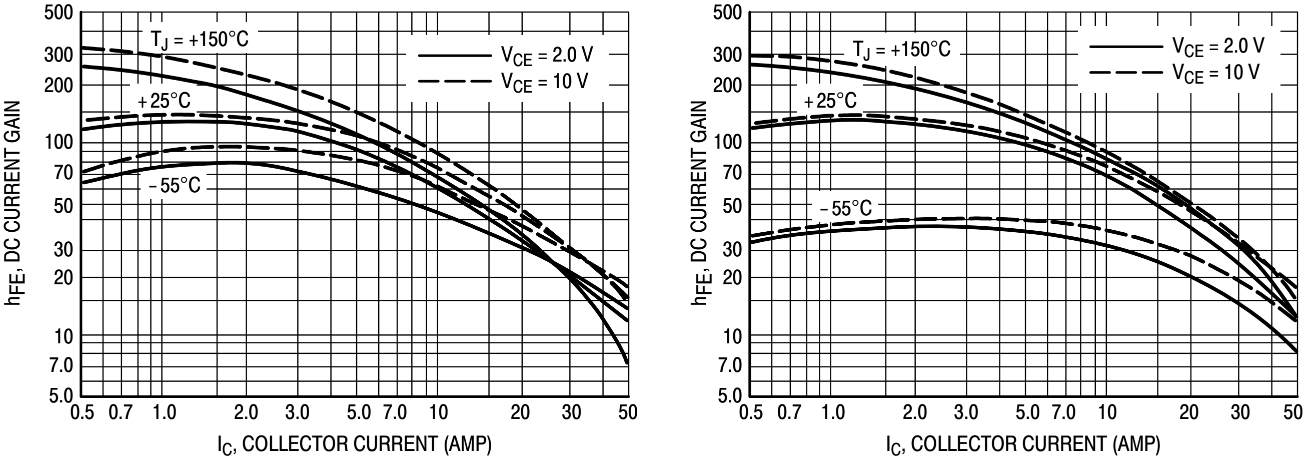


Figure 7. Capacitance


PNP
2N5684

NPN
2N5686

Figure 8. DC Current Gain

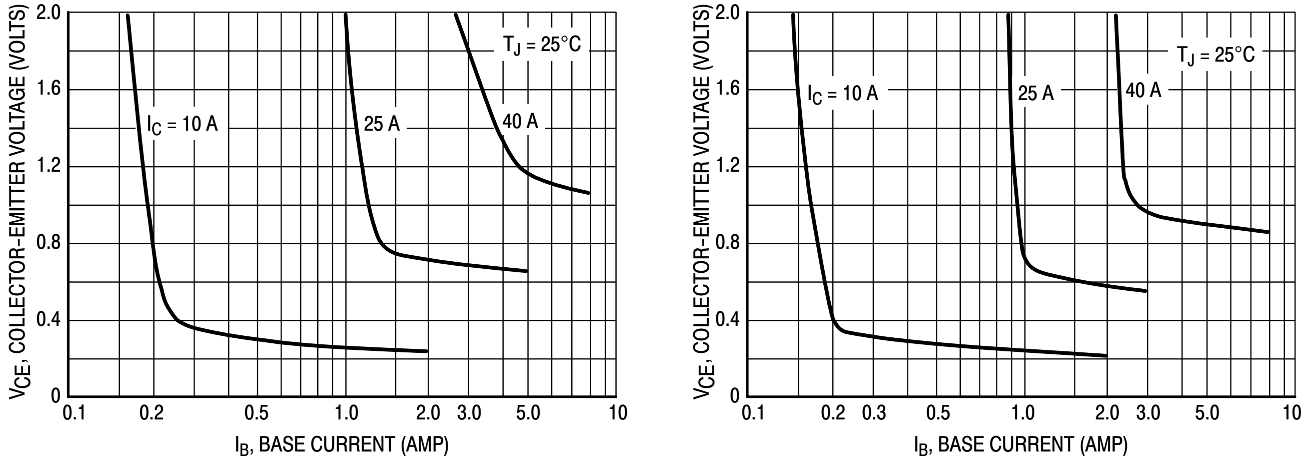


Figure 9. Collector Saturation Region

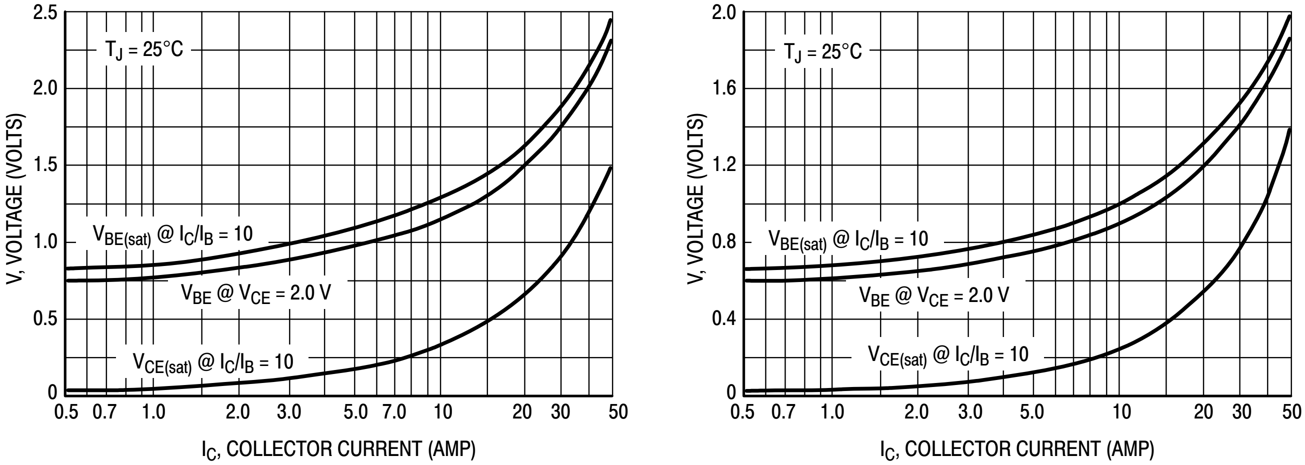
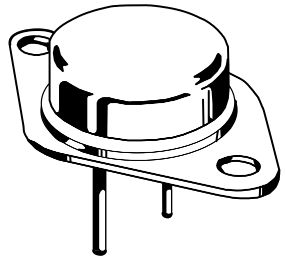


Figure 10. “On” Voltages

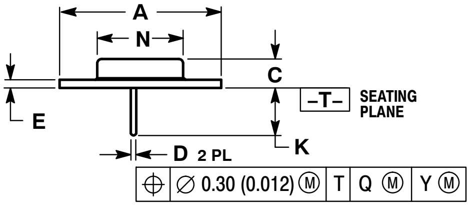
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

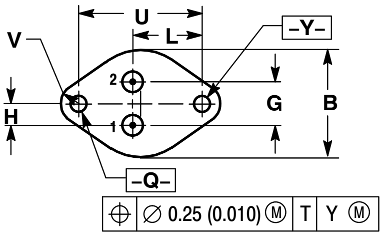


SCALE 1:1

TO-204 (TO-3)
CASE 197A-05
ISSUE K

DATE 21 FEB 2000





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

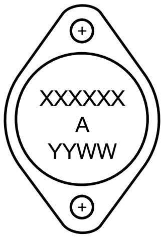
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. EMITTER
2. BASE
CASE: COLLECTOR

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE: DRAIN

STYLE 4:
PIN 1. ANODE = 1
2. ANODE = 2
CASE: CATHODES

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Locationa
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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