

# Medium-Power Plastic PNP Silicon Transistors

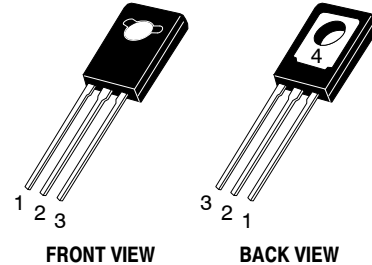
3.0 A, 40–80 V, 30 W  
GENERAL PURPOSE  
POWER TRANSISTORS

## 2N4918 - 2N4920 Series

These medium-power, high-performance plastic devices are designed for driver circuits, switching, and amplifier applications.

### Features

- Low Saturation Voltage –  $V_{CE(sat)} = 0.6 \text{ Vdc (Max) @ } I_C = 1.0 \text{ A}$
- Excellent Power Dissipation,  $P_D = 30 \text{ W @ } T_C = 25^\circ\text{C}$
- Excellent Safe Operating Area
- Gain Specified to  $I_C = 1.0 \text{ A}$
- Complement to NPN 2N4921, 2N4922, 2N4923
- Pb-Free Package is Available\*



TO-225  
CASE 077  
STYLE 1

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector – Emitter Voltage	$V_{CEO}$	40	Vdc
		60	
		80	
Collector – Base Voltage	$V_{CBO}$	40	Vdc
		60	
		80	
Emitter – Base Voltage	$V_{EBO}$	5.0	Vdc
Collector Current – Continuous (Note 1)	$I_C$ (Note 2)	1.0	Adc
		3.0	
Base Current	$I_B$	1.0	Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	30	W
		0.24	
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The 1.0 A max  $I_C$  value is based upon JEDEC current gain requirements. The 3.0 A max value is based upon actual current-handling capability of the device (See Figure 5).
2. Indicates JEDEC Registered Data for 2N4918 Series.

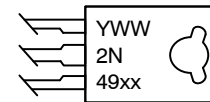
### THERMAL CHARACTERISTICS (Note 3)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$\theta_{JC}$	4.16	$^\circ\text{C/W}$

3. Recommend use of thermal compound for lowest thermal resistance.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### MARKING DIAGRAM



xx = 18, 19, 20  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 2.

## 2N4918 – 2N4920 Series

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (Note 4) ( $I_C = 0.1\text{ A dc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	40 60 80	– – –	Vdc
Collector Cutoff Current ( $V_{CE} = 20\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 30\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 40\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	– – –	0.5 0.5 0.5	mAdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 125^\circ\text{C}$ )	$I_{CEX}$	– –	0.1 0.5	mAdc
Collector Cutoff Current ( $V_{CB} = \text{Rated } V_{CB}$ , $I_E = 0$ )	$I_{CBO}$	–	0.1	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	1.0	mAdc

### ON CHARACTERISTICS

DC Current Gain (Note 4) ( $I_C = 50\text{ mAdc}$ , $V_{CE} = 1.0\text{ Vdc}$ ) ( $I_C = 500\text{ mAdc}$ , $V_{CE} = 1.0\text{ Vdc}$ ) ( $I_C = 1.0\text{ A dc}$ , $V_{CE} = 1.0\text{ Vdc}$ )	$h_{FE}$	40 30 10	– 150 –	–
Collector–Emitter Saturation Voltage (Note 4) ( $I_C = 1.0\text{ A dc}$ , $I_B = 0.1\text{ A dc}$ )	$V_{CE(sat)}$	–	0.6	Vdc
Base–Emitter Saturation Voltage (Note 4) ( $I_C = 1.0\text{ A dc}$ , $I_B = 0.1\text{ A dc}$ )	$V_{BE(sat)}$	–	1.3	Vdc
Base–Emitter On Voltage (Note 4) ( $I_C = 1.0\text{ A dc}$ , $V_{CE} = 1.0\text{ Vdc}$ )	$V_{BE(on)}$	–	1.3	Vdc

### SMALL-SIGNAL CHARACTERISTICS

Current–Gain – Bandwidth Product ( $I_C = 250\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$f_T$	3.0	–	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 100\text{ kHz}$ )	$C_{ob}$	–	100	pF
Small–Signal Current Gain ( $I_C = 250\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	25	–	–

4. Pulse Test:  $PW \approx 300\ \mu\text{s}$ , Duty Cycle  $\approx 2.0\%$

### ORDERING INFORMATION

Device	Package	Shipping†
2N4920G	TO–225 (Pb–Free)	500 Unit / Bulk

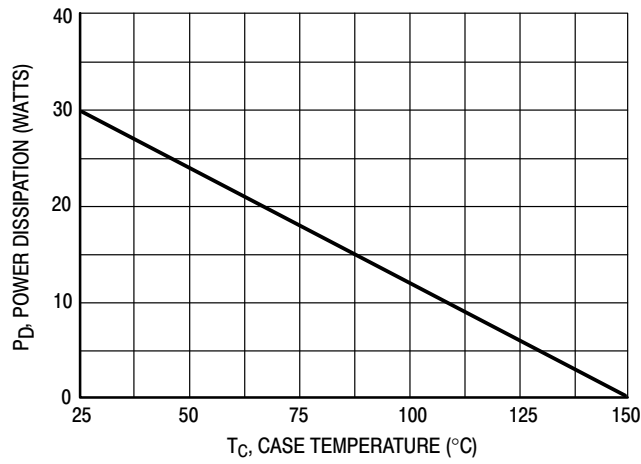
### DISCONTINUED (Note 5)

2N4918	TO–225	500 Unit / Bulk
2N4919	TO–225	500 Unit / Bulk
2N4920	TO–225	500 Unit / Bulk

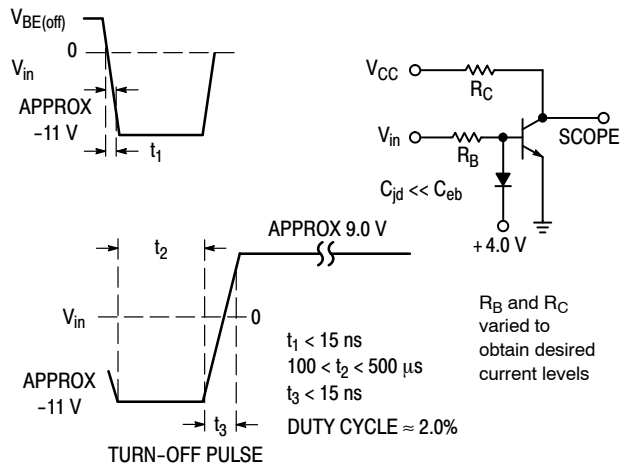
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

5. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on [www.onsemi.com](http://www.onsemi.com).

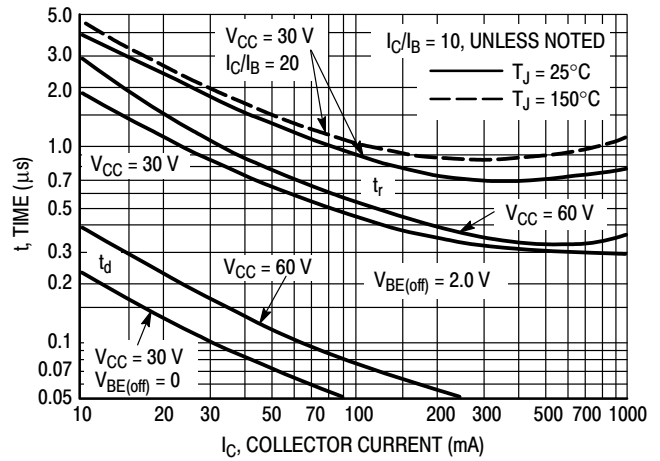
## 2N4918 – 2N4920 Series



**Figure 1. Power Derating**

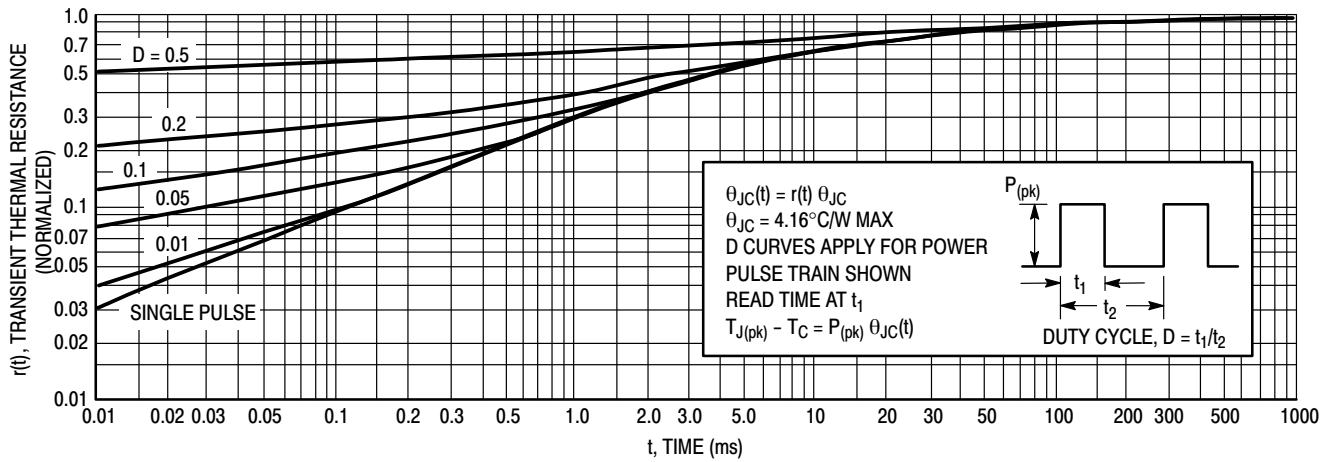


**Figure 2. Switching Time Equivalent Test Circuit**

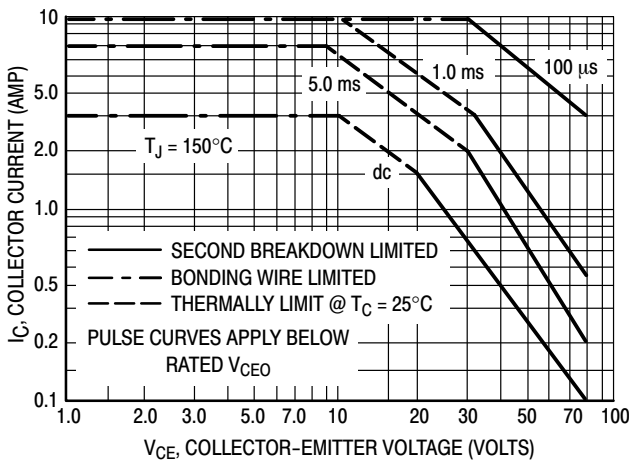


**Figure 3. Turn-On Time**

## 2N4918 - 2N4920 Series



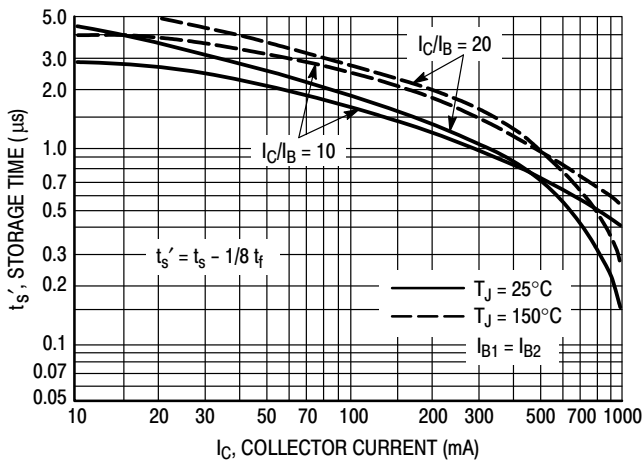
**Figure 4. Thermal Response**



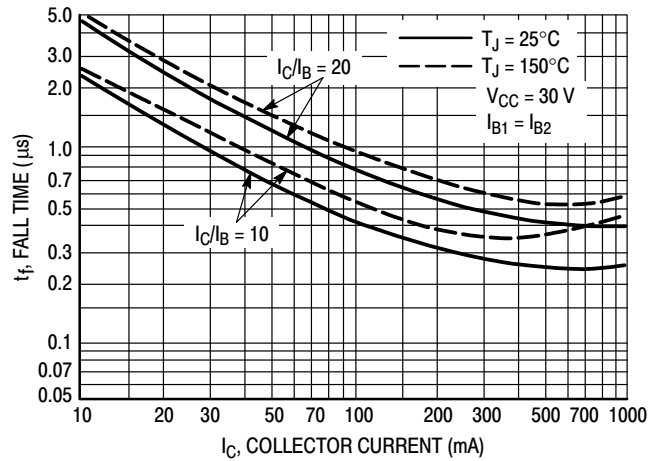
**Figure 5. Active-Region Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^{\circ}\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^{\circ}\text{C}$ . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



**Figure 6. Storage Time**



**Figure 7. Fall Time**

# 2N4918 – 2N4920 Series

## TYPICAL DC CHARACTERISTICS

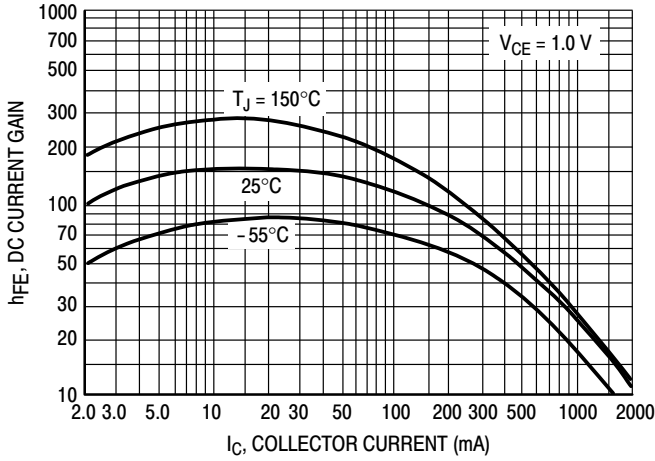


Figure 8. Current Gain

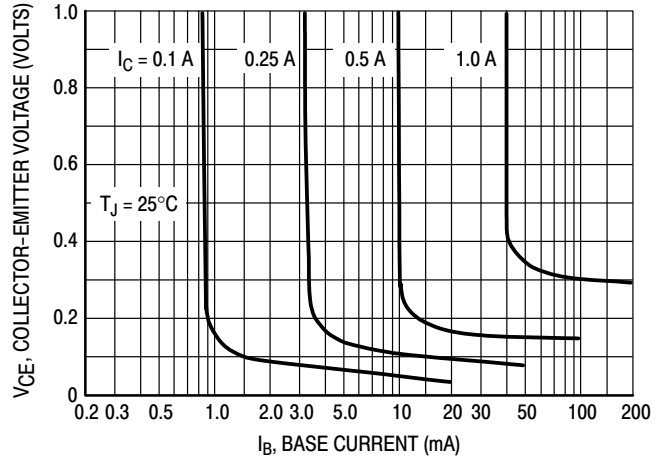


Figure 9. Collector Saturation Region

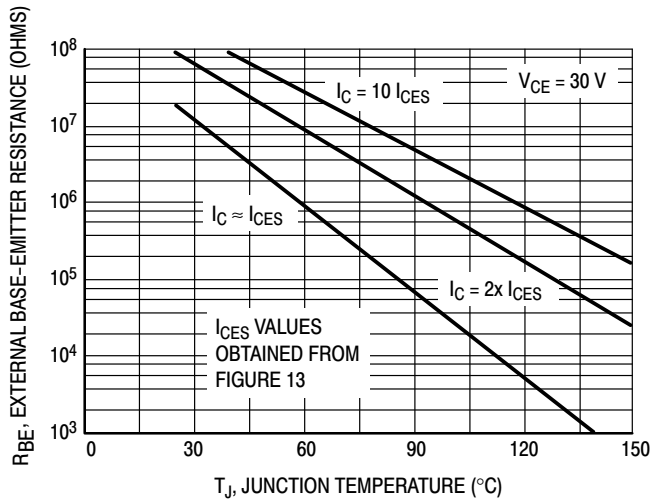


Figure 10. Effects of Base-Emitter Resistance

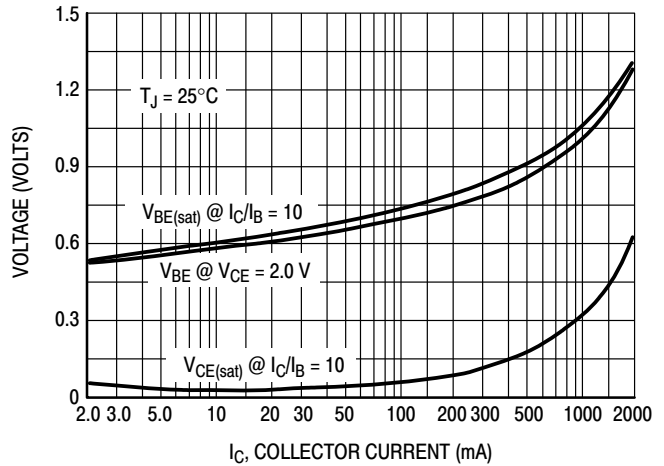


Figure 11. "On" Voltage

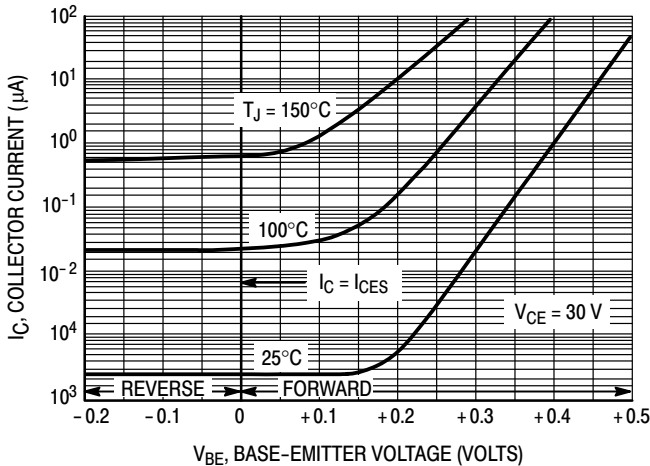


Figure 12. Collector Cut-Off Region

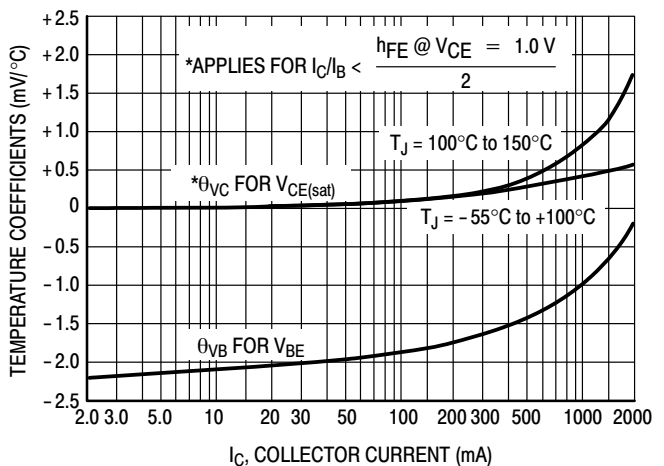
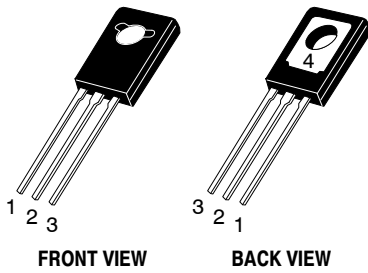


Figure 13. Temperature Coefficients

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



**TO-225**  
CASE 77-09  
ISSUE AD

DATE 25 MAR 2015

SCALE 1:1



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. NUMBER AND SHAPE OF LUGS OPTIONAL.

DIM	MILLIMETERS	
	MIN	MAX
A	2.40	3.00
A1	1.00	1.50
b	0.60	0.90
b2	0.51	0.88
c	0.39	0.63
D	10.60	11.10
E	7.40	7.80
e	2.04	2.54
L	14.50	16.63
L1	1.27	2.54
P	2.90	3.30
Q	3.80	4.20

**GENERIC MARKING DIAGRAM\***



- Y = Year
- WW = Work Week
- XXXXX = Device Code
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "µ", may or may not be present.

- |   |   |   |   |   |
|---|---|---|---|---|
| <p>STYLE 1:<br/>PIN 1. EMITTER<br/>2., 4. COLLECTOR<br/>3. BASE</p> | <p>STYLE 2:<br/>PIN 1. CATHODE<br/>2., 4. ANODE<br/>3. GATE</p> | <p>STYLE 3:<br/>PIN 1. BASE<br/>2., 4. COLLECTOR<br/>3. EMITTER</p> | <p>STYLE 4:<br/>PIN 1. ANODE 1<br/>2., 4. ANODE 2<br/>3. GATE</p> | <p>STYLE 5:<br/>PIN 1. MT 1<br/>2., 4. MT 2<br/>3. GATE</p>     |
| <p>STYLE 6:<br/>PIN 1. CATHODE<br/>2., 4. GATE<br/>3. ANODE</p>     | <p>STYLE 7:<br/>PIN 1. MT 1<br/>2., 4. GATE<br/>3. MT 2</p>     | <p>STYLE 8:<br/>PIN 1. SOURCE<br/>2., 4. GATE<br/>3. DRAIN</p>      | <p>STYLE 9:<br/>PIN 1. GATE<br/>2., 4. DRAIN<br/>3. SOURCE</p>    | <p>STYLE 10:<br/>PIN 1. SOURCE<br/>2., 4. DRAIN<br/>3. GATE</p> |

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