JFET Primer

Construction and Operation of the SiC JFET

AND90329/D

Scope

This document provides explains the construction and operation of **onsemi** SiC JFETs to facilitate their use mainly in a variety of applications. Following the JFET construction is a description of key parameters, unique features, and datasheet graphs.

Introduction

The SiC JFET has some significant advantages over competing technologies, particularly low on-resistance for a given chip area, known as $R_{DS}{\cdot}A$, and no parameter drift even after repeated high energy transients. These are critically important for semiconductor circuit breakers and relays, which require extremely low conduction loss, completely reliable switching both normally and during an emergency, and a service life of 20+ years.

This application note provides qualitative explanations of construction, operation, and unique features of the **onsemi** SiC JFET. There is very little math involved since this is a basic introduction to JFETs. For information about the application of SiC JFET in circuits, please refer to the SiC JFET User Guide.

JFET Construction

Figure 1 shows a “cartoon” cross-section drawing of a **onsemi** SiC JFET, which is a vertical JFET, in this case without voltages applied. The three JFET terminals are labelled: source, gate, and drain. The PN junction of the gate and drift region forms the drain-gate diode. The other diode in the JFET is between gate and source. It is helpful to think of driving the JFET gate as biasing the gate-source diode. Each of these diodes has a corresponding capacitance. Doping type and concentration are qualitatively shown. Each channel and gate region forms a “cell”, and there are thousands of parallel cells in a single JFET.

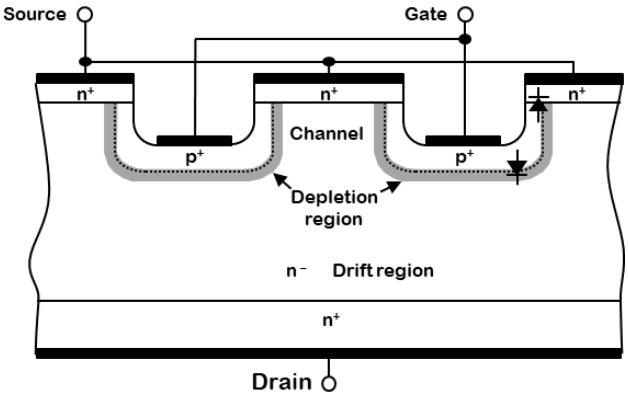

Figure 1. Vertical JFET Cross Section

There is a depletion region around the drain-gate PN junction. This depletion region is highly resistive due to a lack of mobile carriers. In this unbiased state, the depletion region is so small that electrons can freely flow between the source and drain terminals through the open channel. This gives the **onsemi** SiC JFET its normally on characteristic.

Figure 2 shows a single JFET cell with drain-to-source current flowing and with positive V_{DS}. This positive V_{DS} reverse biases the drain-gate PN junction and causes its depletion region to expand. If V_{DS} continues to increase until the depletion regions fill the channel, then the channel is “pinched” and current can no longer increase much, a condition commonly called saturation. A positive gate-source voltage forward-biases the drain-gate (and gate-source) PN junction, causing the drain-gate depletion region to shrink and thus countering its expansion due to positive V_{DS} as indicated Figure 2(a) and (b) with $V_{GS} = 0$ and $V_{GS} > 0$, respectively. Applying positive V_{GS} is an easy way to reduce the on-resistance by about 15%, depending on operating conditions. This significant reduction is one of the benefits of the SiC JFET in applications where minimizing conduction loss is top priority, such as semiconductor circuit breakers and relays.

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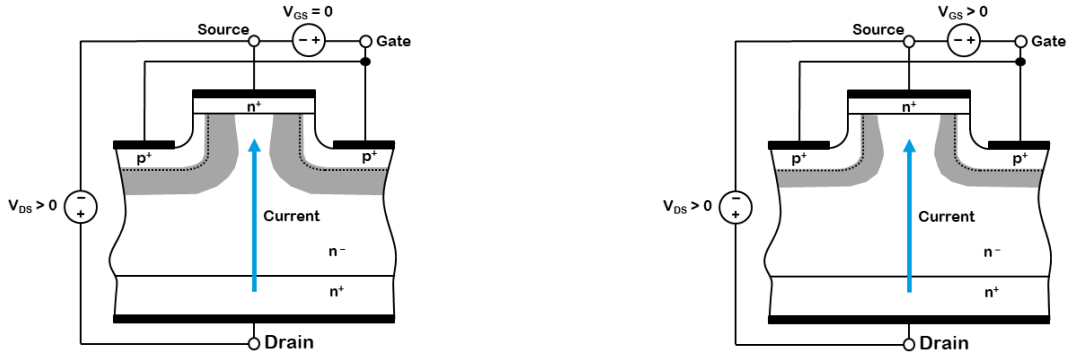

Figure 2. onsemi SiC JFET Cell with Drain-source Current Flow Causing Positive V_{DS} and (a) V_{GS} = 0, and (b) V_{GS} > 0

The reduction in on-resistance mentioned here is due to a widening of the channel with V_{GS} in the range of 1.8 to 2.5 V. On-resistance can be even further reduced by injecting enough gate current to result in bipolar current flow (electrons and holes), but any benefit from this would be countered by the high gate drive power required. There is no risk of damaging the JFET chip unless the gate current continuously exceeds several Amps. A quick side note: even with sufficient current into the gate to cause significant conductivity modulation, the SiC JFET can still switch fast. Minority carriers (holes) in the drift region are either quickly recombined due to short lifetime in SiC or quickly swept out because there is no PN junction in the current path to trap minority carriers.

Applying negative V_{GS} expands each depletion region. With sufficiently negative V_{GS}, the expanded depletion regions “pinch off” the channel, as indicated in Figure 3(a), with V_{DS} = 5 V, which is typically used when measuring the threshold voltage $V_{G(th)}$.

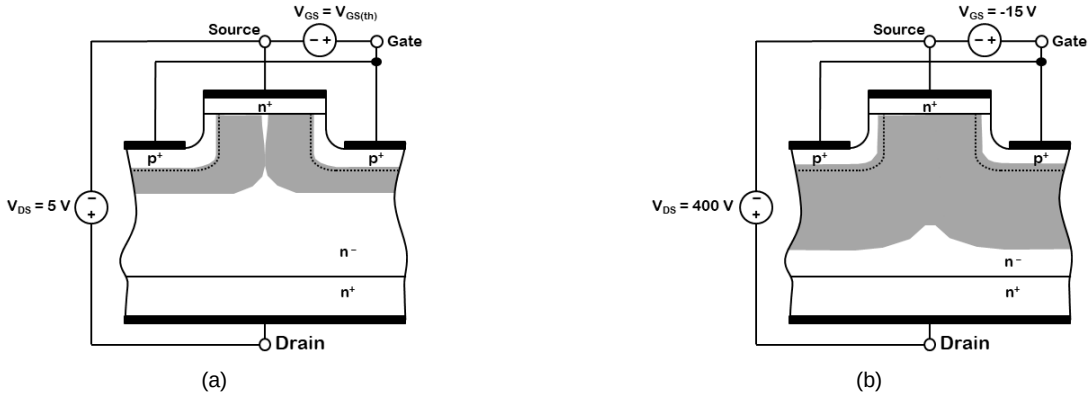

Figure 3. onsemi SiC JFET Cell (a) Biased at V_{GS} = $V_{G(th)}$ and V_{DS} = 5 V, and (b) V_{GS} = −15 V and V_{DS} = 400 V

In Figure 3(b), the JFET is fully off with V_{GS} = −15 V and a V_{DS} of 400 V expanding the depletion region well into the drift region where high voltage is blocked by the drain-gate diode. If V_{DS} is increased until the depletion region expands to the edge of the drift region, then the JFET avalanches and current increases sharply with further increasing V_{DS}. Power dissipation in avalanche is very high due to the high V_{DS}, with energy in the chip dependent upon time spent in avalanche and the avalanche current. **onsemi** SiC JFETs can survive repetitive avalanche, and all JFETs avalanche tested during production. Of course, the avalanche energy must remain within the energy absorption capability of the chip, which depends on design and chip size.

This background information makes the curves in the JFET datasheet more meaningful. Shown in Figure 4 are output characteristics with various gate-source voltages at room temperature (a) and maximum operating temperature (b) of a 750 V, 4.3 mΩ SiC JFET in a TOLL (MO-229) package, part number UJ4N075004L8S. The typical part has a gate threshold voltage $V_{G(th)}$ = −6 V, at which 180 mA flows from drain to source with V_{DS} = 5 V. A good way to think of the threshold voltage is as an indicator of when a part begins to switch on rather than off. A gate-source voltage at least 2 V less than the minimum threshold voltage is needed to keep the JFET fully off. The UJ4N075004L8S has a minimum $V_{G(th)}$ of −8.3 V, so a maximum keep-off voltage would be −10.3 V, whereas −12 V or less is recommended.

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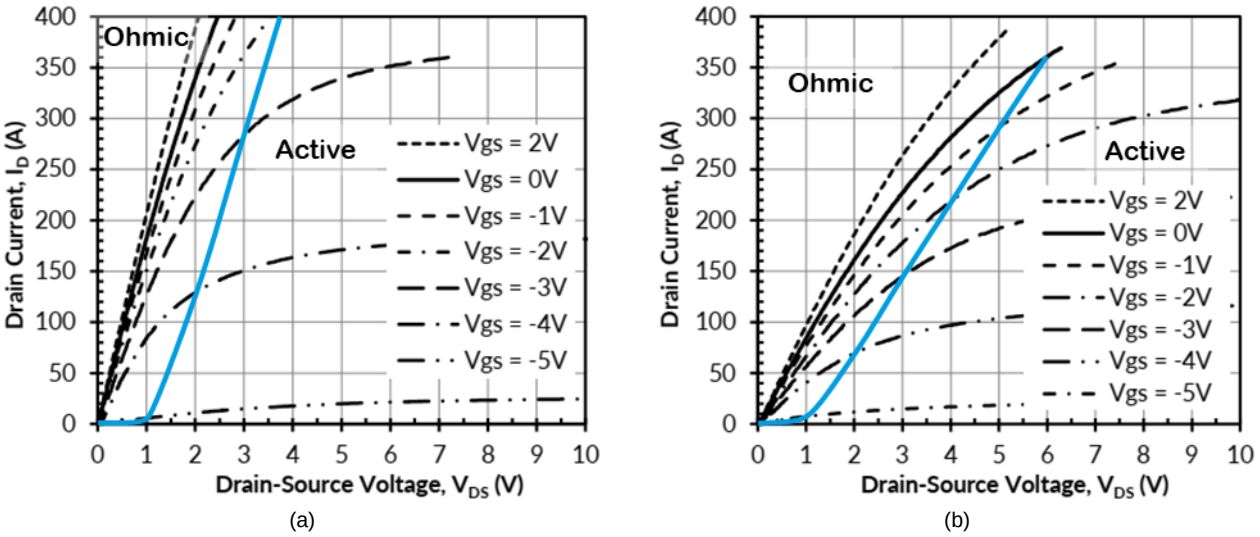

Figure 4. UJ4N075004L8S SiC JFET Output Characteristics at (a) 25 °C, and (b) 175 °C

In Figure 4, with V_{GS} = −5 V, the channel width is highly constricted by the depletion regions, so current flow is limited. Current increases slightly with V_{DS}, and the JFET is in "saturation". At V_{GS} = −4 V, the depletion regions are narrower, making the channel wider and thus increasing the conductivity (reducing the on-resistance). This curve clearly shows the effect of increasing V_{DS} widening the depletion regions, "bending" the output characteristic curve until there is little increase in current versus V_{DS}. Saturation is also called active mode because drain-source current responds strongly to changes in V_{GS}, and very little to V_{DS}; the current is gate-controlled. The boundary between Ohmic and Active modes is defined as $V_{GS} - V_{G(th)} > V_{DS} > 0$ and is indicated in each graph in Figure 4 by the blue curves.

Increasing V_{GS} decreases the width of the depletion regions, thus widening the channel and reducing on-resistance. Figure 4 shows curves corresponding to certain V_{GS} values, all the way to +2 V, which is the last V_{GS} test voltage. Note that $R_{DS(on)}$ is on-resistance measured at either V_{GS} = 0 V or V_{GS} = +2 V. Figure 3(a) shows output characteristics at 25 °C, and Figure 3(b) at 175 °C. The $R_{DS(on)}$ at 125 °C measured with V_{GS} = 0 V is 1.63 times higher than at 25 °C, and 2.18 times higher at 175 °C. This temperature coefficient (TC for short) of $R_{DS(on)}$ is mostly due to the bulk SiC material in the JFET. The $R_{DS(on)}$ TC must be considered when selecting a SiC JFET part number and deciding how many to parallel.

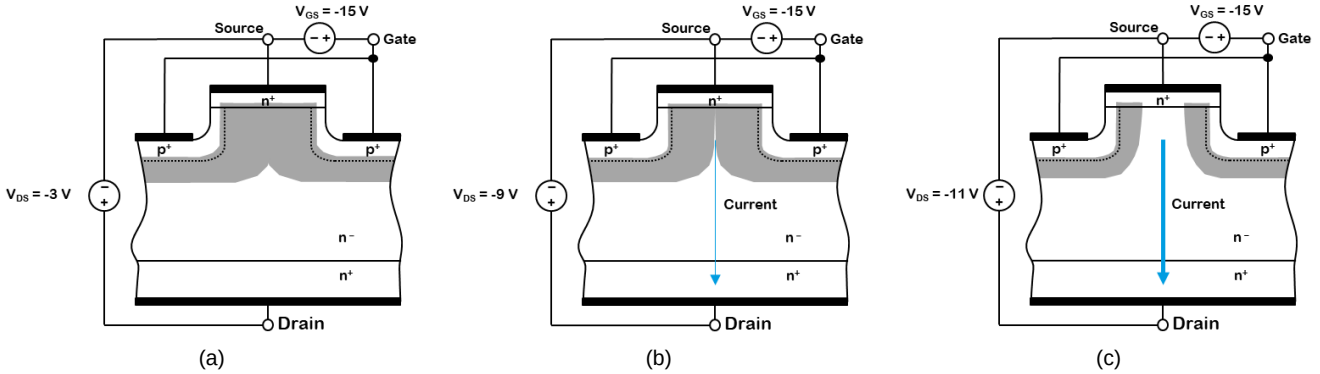

Figure 5. onsemi Gen3 and Gen4 SiC JFET with Reverse Biases

With the absence of a body diode, the **onsemi** Gen3 and Gen4 SiC JFETs have unique reverse conduction characteristics. Figure 5 shows a Gen3 or Gen4 SiC JFET cell with V_{GS} = −15 V and various drain-source biases. In Figure 5(a), V_{DS} = −3 V. Remember that negative V_{GS} expands the depletion regions, whereas negative V_{DS} contracts them. The difference between V_{DS} and V_{GS} is several Volts below the threshold voltage, so the channel is fully blocked, and no drain-source current can flow (except sub-microamp leakage current, which we ignore for now). In Figure 5(b), V_{DS} has decreased to −9 V, and $V_{GS} - V_{DS}$ = −6 V, which is $V_{G(th)}$ of this JFET, and a small current flows from source to drain. In Figure 5(c), $V_{GS} - V_{DS}$ = −4 V, which is 2 V above the threshold voltage and source-drain current flows much more freely.

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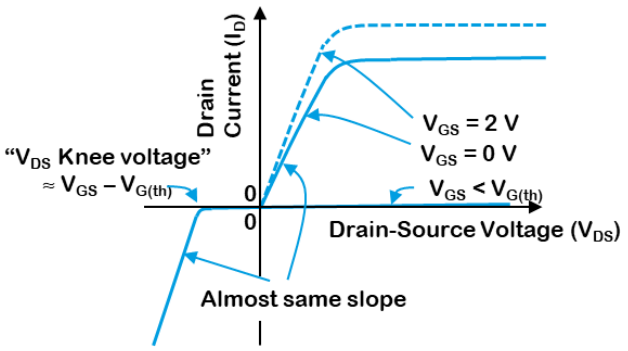

Figure 6. Extended Output Characteristics

The forward and reverse characteristics are summarized in Figure 6 where negative drain-source current and voltage are included. The **onsemi** SiC JFET can block hundreds of Volts in the first quadrant (positive V_{DS} and I_D), but as we have seen, it can block very limited voltage in the third quadrant. This blocking voltage depends on the drain-gate and gate-source diode biasing, and very little on temperature due to the weak temperature coefficient of the threshold voltage (TVTC). Negative V_{DS} tends to open the JFET channel and overcomes the tendency of negative V_{GS} to close it when, approximately, $V_{DS} \le V_{GS} - V_{G(th)}$. This is approximate because $V_{G(th)}$ is measured with V_{DS} = +5 V, but we are now dealing with negative V_{DS} and hence a slightly wider channel. An easy way to remember this is the V_{DS} "knee voltage" is approximately the amount that V_{GS} is driven more negative than $V_{G(th)}$. Another way to think of when reverse current can flow is by rearranging and combining, $V_{DS} \le V_{GS} - V_{G(th)}$, which becomes $V_{GS} \ge V_{G(th)}$, as if the gate and source terminals swapped functions.

The expansion of the channel with more negative current and hence more negative V_{DS} results in slightly lower on-resistance with reverse versus forward current, and negative current versus V_{DS} curves do not bend and go into saturation as they do with forward current. What happens if the source-drain current has extremely large magnitude? A second loop includes the gate drive and the drain-gate diode, as shown in Figure 7 where V_{DS} is negative enough to forward bias the drain-gate diode inside the JFET, designated as DG Figure 7. This requires a very high current relative to the JFET's normal operating current, almost a short-circuit condition.

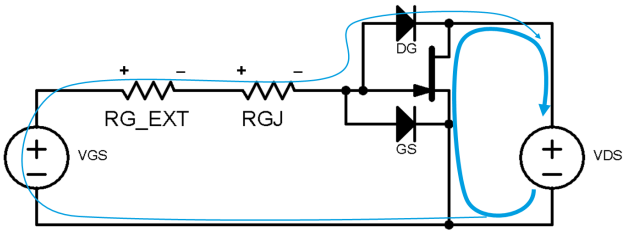

Figure 7. Extremely High Reverse Current Causing Drain-gate Diode Current

Such current through the internal and external gate resistors (RGJ and RG_EXT) causes a reduction in gate-source voltage at the JFET terminals and consequently an increase in the on-resistance. This tends to limit the peak reverse current. This is more likely to happen when the JFET chip is hot, with correspondingly higher on-resistance and lower forward voltage of the drain-gate diode. Power dissipation is very high in this situation, so the duration must be short, a few microseconds at most.

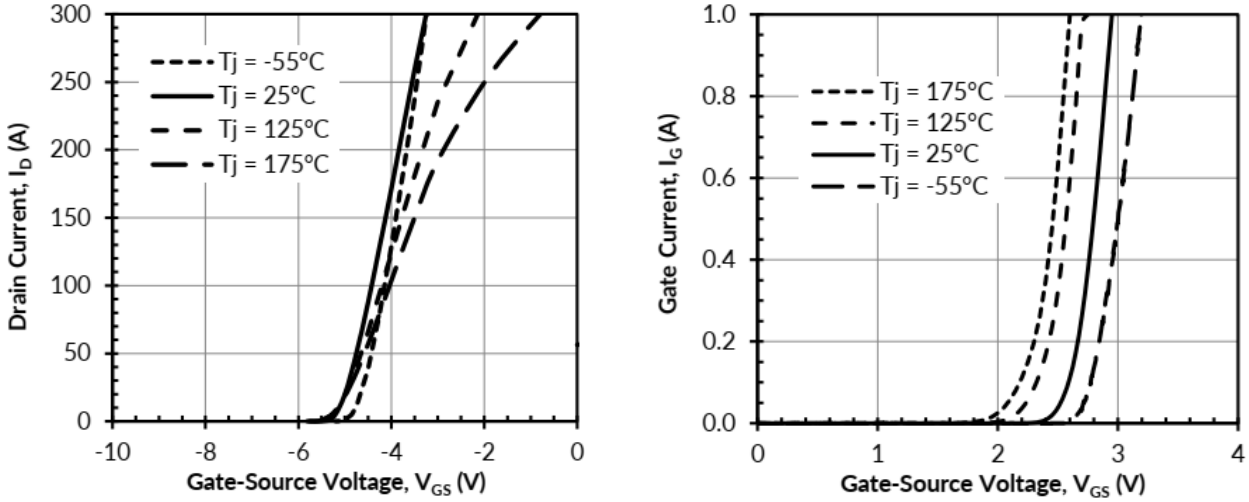

Figure 8. UJ4N075004L8S (a) Transfer Characteristics and (b) Gate Current versus Voltage

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Figure 8(a) shows the UJ4N075004L8S transfer characteristics. From the slopes of the straight-line portions of the curves, the transconductance at 25, 125, and 175 °C is 164, 113, and 90 A/V respectively. There is very little crossover of the 25, 125, and 175 °C transfer characteristic curves, which is due to the quite flat threshold voltage temperature coefficient (TVTC) of only −1.8 mV/°C for this **onsemi** Gen4 SiC JFET. A flat TVTC greatly reduces a chance of a thermally unstable hot spot forming on the chip during active mode operation and high current switching. This is one of the reasons the **onsemi** SiC JFET is so reliable. Another is no degradation or parameter drift, thanks to the simple electrical structure of the JFET. Please refer to the JFET Active Mode Application Note for further details.

Figure 8(b) shows the UJ4N075004L8S gate current versus V_{GS}, where the SiC JFET gate-source diode is forward biased. The temperature-dependent diode “knee voltage” is plain to see, and the slope corresponds to the JFET gate resistance, which for this part is 0.4 Ω. Notice that V_{GS} is in a range of about 2 to 2.6 V with I_G in the milliamps range, with temperature spanning from −55 to 175 °C. Also gleaned from this graph is the JFET’s gate-source diode forward voltage temperature coefficient, which is −3.2 mV/°C. This parameter can be used to sense the JFET chip temperature.

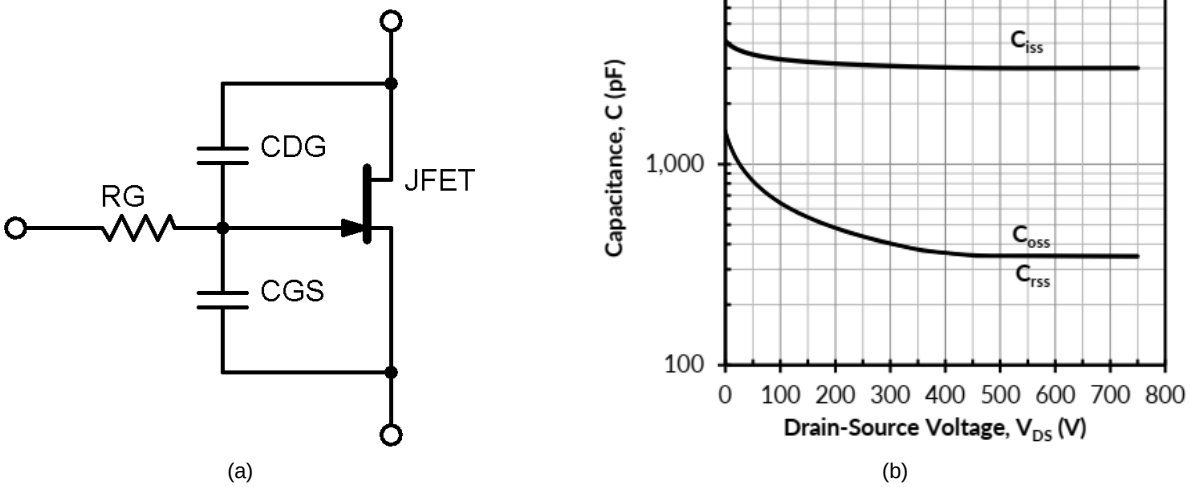

Figure 9. (a) onsemi SiC JFET Symbol with Intrinsic Capacitances and Gate Resistance (b) UJ4N075004L8S Capacitances versus V_{DS}

Figure 9(a) shows a JFET symbol with drain-gate capacitance (CDG), gate-source capacitance (CGS), and on-chip gate resistance (RG) explicitly shown. The input capacitance C_{iss} in the graph of Figure 9(b) is the parallel combination of the drain-gate (same as C_{rss}) and gate-source capacitances, and we see that most of the input capacitance is from the gate-source capacitance. A unique feature of **onsemi** Gen3 and Gen4 SiC JFETs is the lack of drain-source capacitance, resulting from no P−N junction in the drain-source current path and no body diode feature. Output capacitance C_{oss} is the parallel combination of drain-source and drain-gate capacitances, and it is directly related to chip size regardless of technology (JFET, MOSFET, IGBT, etc.). Because the drain-source capacitance is practically zero, all the output capacitance is from the drain-gate capacitance, designated as C_{rss}. This is why C_{oss} and C_{rss} are equal in the capacitance graph in Figure 9(b).

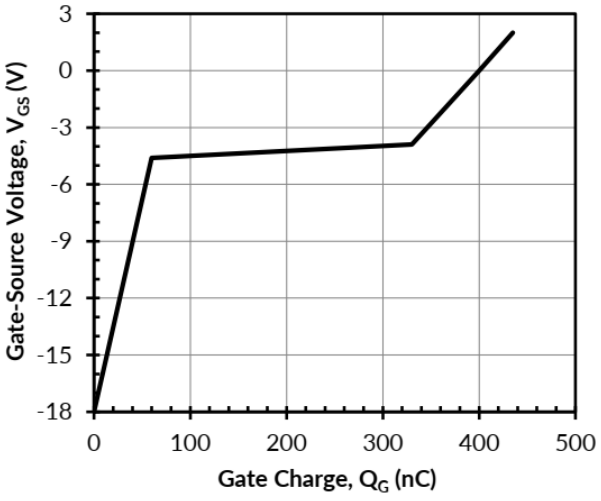

Figure 10. UJ4N075004L8S V_{GS} versus Gate Charge

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Two final points: First, the **onsemi** Gen3 and Gen4 SiC JFET gate charge is relatively large because $C_{rss} = C_{oss}$. During V_{DS} voltage transition, the entire output capacitance is charged/discharged by the gate driver. This is especially desirable for low switching frequency applications that need easy control of the switching speed, such as semiconductor circuit protection and relays. One simply adjusts the gate resistor value and/or the gate drive voltage. On the other hand, the high gate charge makes switch-mode applications more challenging with these JFETs. Finally, gate drive loop design and layout are critical. Please follow the best practices mentioned in the JFET User Guide.

Summary

- **onsemi** manufactures vertical SiC JFETs. Their design and operation were qualitatively presented.
- **onsemi** SiC JFETs feature industry leading R_{DS}·A, high peak current capability, and outstanding reliability.
- The JFET's unique characteristics were explained, including third quadrant operation and capacitances.
- The JFET User Guide contains valuable information to use **onsemi** SiC JFETs to their full advantage.

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