TND6396/D
Rev. 2, March – 2024

# Silicon Carbide (SiC) – From Challenging Material to Robust Reliability



March, 2024 – Rev. 2
Publication Order Number:
TND6396/D

# Silicon Carbide (SiC) – From Challenging Material to Robust Reliability

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## Abstract

Silicon Carbide (SiC) is one of the most promising semiconductor materials for manufacturing high−power electronic devices. Thanks to its excellent physical properties (high saturation electron drift velocity, high thermal conductivity, high breakdown electric field), SiC−based systems can achieve very low losses and faster−switching speed with smaller geometries than Silicon (Si) MOSFET transistors. While **onsemi** made great use of knowledge and methodologies acquired for many years on Si technologies, the specific challenges introduced by SiC materials have been and still are extensively assessed to tailor an appropriate qualification methodology to demonstrate robust reliability.

This white paper will introduce the reader to the **onsemi** Quality and Reliability methodology deployed from first design to mass production. This comprehensive approach is founded on the interaction between different fields, such as a rigorous design methodology, strict production monitoring, manufacturing control, adequate screening, and robust qualification plans.

This methodology, applied to the Automotive market for many decades, has shown its efficiency on Silicon products and has been tailored to address the specific needs of Silicon Carbide products. You will be guided through this evolution to SiC and, more specifically, its successful deployment addressing the integrity of the Gate Oxide of SiC MOSFET transistors.

Finally, the paper will briefly present recent publications on cryogenic bias temperature instability, body diode degradation, and dynamic stress requirements.

## Introduction

The quality and reliability of a given product are governed by all activities, from ideation to delivery to the end users' product line. The **onsemi** Quality Statement/Policy fully embeds this approach (Figure 1).

It remains subject to several potential process−related reliability hazards even within the highest possible degree of reliability designed into the product.

To eliminate these, one must understand the limiting failure modes and mechanisms and trace them back through failure analysis and feedback loops to process weaknesses and implement

permanent corrective actions. This is achieved through elaborate wafer & product qualification, rigorous design methodology, production monitoring, manufacturing control & adequate screening. The use of these programs is described in the general reliability specifications of **onsemi** and illustrated by the **onsemi** Quality – Road to Zero Defects (Figure 2).


**Figure 1. onsemi Quality Statement/Policy**

Consequently, **onsemi** has implemented three different qualification programs: the wafer fab qualification, the product qualification, and the assembly route qualification. Each of these qualification programs focuses explicitly on other areas of the product manufacturing cycle and aims to ensure maximum reliability of the targeted area.


**Figure 2. onsemi Quality – Road to Zero Defects**

The wafer fab route qualification (also called intrinsic qualification) primarily focuses on the wafer fab processing—designed to ensure a constant inherently high−reliability level for all wafers processed according to the qualified flow. At that stage, physics−based degradation models are extracted.

The product and assembly route qualifications (also called extrinsic qualifications) validate the reliability of the packaged dies based on the Mission Profile of the final products, the ultimate goal being to assure high−reliability performance of the end product.

## Silicon Carbide Challenges

Silicon Carbide (SiC) material combines excellent physical properties and attractive design features, resulting in a very appealing solution for manufacturing high−power electronic devices.

Multiple crucial elements must be combined when safely releasing a product to the market, as illustrated in Figure 3.

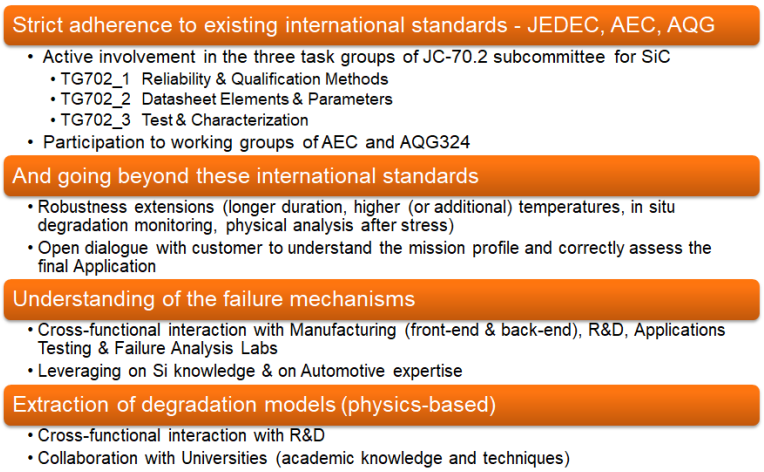


**Figure 3. Definition of Robust Intrinsic and Extrinsic Reliability**

The first challenge is linked to the readiness of international standards. While these guidelines are well established for Silicon−based technologies, multiple sub−teams within JEDEC, AEC, and AQG committees are actively working to develop the proper foundation for future SiC standards. This will ensure that suppliers are guided through a well−documented global methodology and will avoid long debate on the validity of collected data.

The next challenge resides in the physics−based understanding of the failure mechanisms to properly quantify the product robustness versus the required Mission Profile of the customer.

Electric Vehicles typically have extended mission profiles when compared to combustion vehicles. This, combined with the enhanced performance of SiC technology compared to

conventional Si technology or IGBTs, requires the reliability stressing to match the final customer Application more closely.

At this stage, the involvement of a cross−functional team (Manufacturing front−end, Research & Development, Manufacturing back−end, Applications Testing, and Failure Analysis engineering) is key to success. A clear relation between Intrinsic Reliability (lifetime models) and Applications is established.

Close collaboration with Universities and Research Centers is crucial to go deeper into the theoretical aspects or to offer dedicated techniques & complementary skill sets not always available in the semiconductor industry. Figure 4 illustrates the characterization and Reliability assessment of the SiC/$SiO_2$ interface.

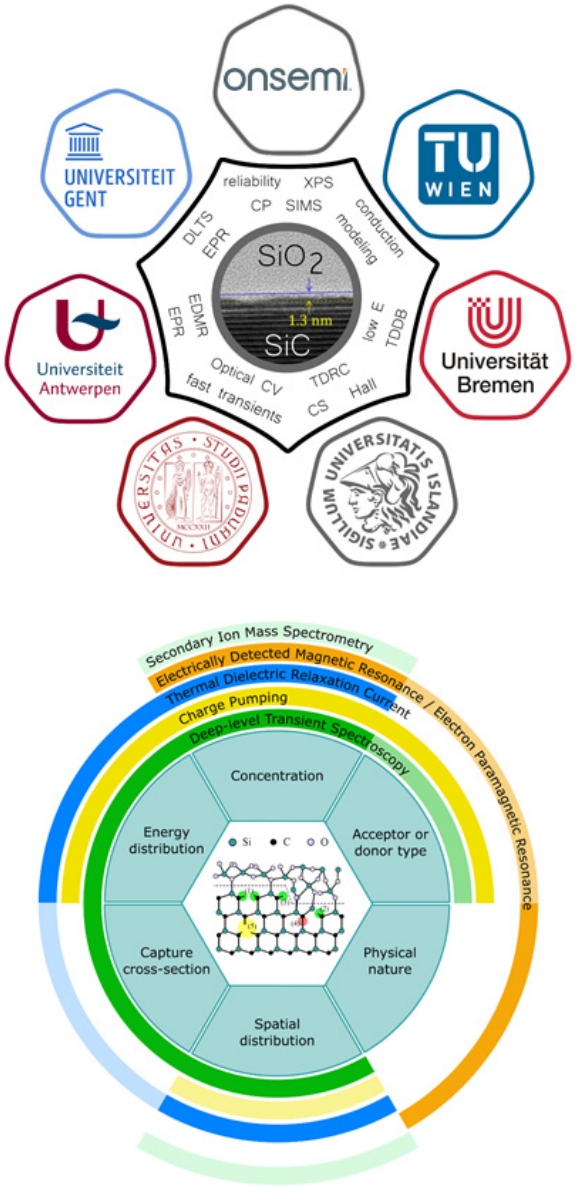


**Figure 4. Collaboration with Universities and Research Centers − SiC/$SiO_2$ Interface**

The following SiC−specific challenges typically need to be addressed:

- Substrate and Epitaxy defectivity level
- Gate Oxide: intrinsic lifetime modeling ($SiC/SiO_2$ interface characterization) and extrinsic population (screening)
- Body Diode degradation
- Reliability during high−voltage blocking (HTRB)
- Application−related performance (Avalanche robustness, Edge termination, Short Circuit, Ruggedness against Cosmic Rays, Design for High dv/dt ruggedness, Surge currents).

## The onsemi Methodology

For each degradation mechanism, the **onsemi** approach is rigorous and cross−functional. Steps are Control – Improve – Test & Screen – Characterize – Qualify & extract models.

When applied to Gate Oxide Integrity (GOI), these steps articulate as follows:

### Control

Methodology and tools are in place for manufacturing SiC technologies (Control Plan, Statistical Process Control, Process FMEA). Data is being collected and used as a foundation for potential process improvements.

### Improve

Since substrate or epitaxial defects, metallic contaminants, and particles can heavily impact the gate oxide quality, continuous improvements and their controlled introduction to production are crucial to reduce defects' occurrence further.

### Test & Screen

**onsemi** has developed a full suite of visual and electrical screening tools to eliminate defective dies.

The wafer fab process flow starts with a substrate scan, identifying all defects with coordinates tracking and auto−classification. Multiple inspections identify additional potential process defects at critical process steps. All flagged defects found in the inspections above are excluded from the population (Figure 5).

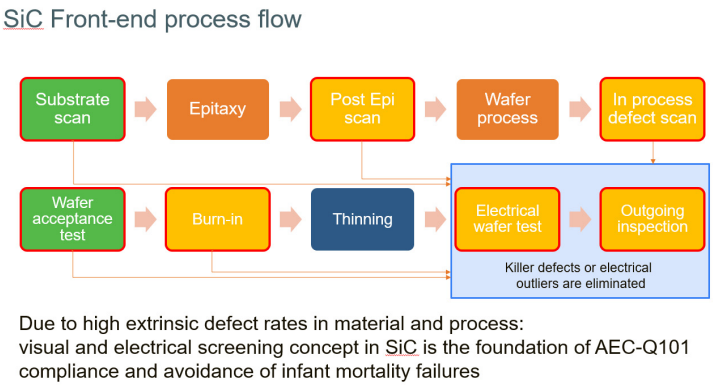


**Figure 5. Scanning and Inspections During the Front−End Process**

Electrical screening is implemented at multiple levels:

- Wafer level performance and acceptance (parametric testing and gate oxide integrity acceptance criteria)
- Wafer level Burn−in
- Wafer level die Sort
- Dynamic Part Average Testing is in place to remove electrical outliers.

Finally, all wafers are screened with 100% automated outgoing inspection, including for visual defects.

### Characterize

**onsemi** is using the Charge to Failure ($Q_{BD}$) as a simple method to compare gate oxide quality independent of the gate oxide thickness. This technique is more refined than GOI/Vramp and will detect finer details in the intrinsic distribution.

As illustrated in Figure 6, planar SiC and Si gate oxides have comparable intrinsic capabilities in breakdown and lifetime. A side−by−side comparison of intrinsic $Q_{BD}$ performance (independent of gate oxide thickness) shows **onsemi** planar SiC being 50 times better intrinsically than Si for the same nominal thickness.

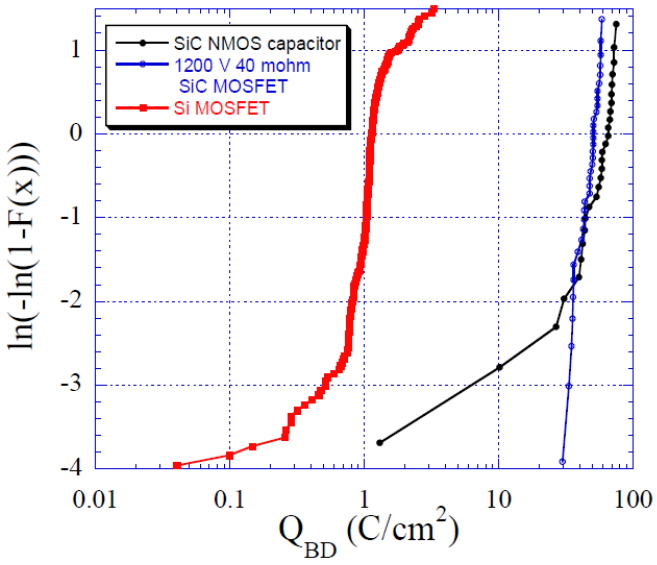


**Figure 6. $Q_{BD}$ Measured for SiC NMOS Capacitors, 1200 V 40 mΩ SiC MOSFETs, and a Si MOSFET Product when forcing 5 mA/cm$^2$ with a Forward Biased Gate at Room Temperature**

In production, the gate oxide quality of each lot is evaluated by sampling charge to failure ($Q_{BD}$) for SiC MOSFET product dies and compared with large area (2.7 mm x 2.7 mm) NMOS capacitors.

An acceptance criterion is in place to accept or reject at the wafer level.

### Qualify & Extract Models

Determining the true current conduction mechanism(s) of the gate oxide is crucial when defining the stressing conditions [1]. Thermally Assisted Tunneling competes with Fowler Nordheim as a function of stressing electric fields and stressing temperature (Figure 7).

Therefore, understanding the conduction mechanisms prevents stress in another conduction mode than the one representative of actual use conditions in the field.

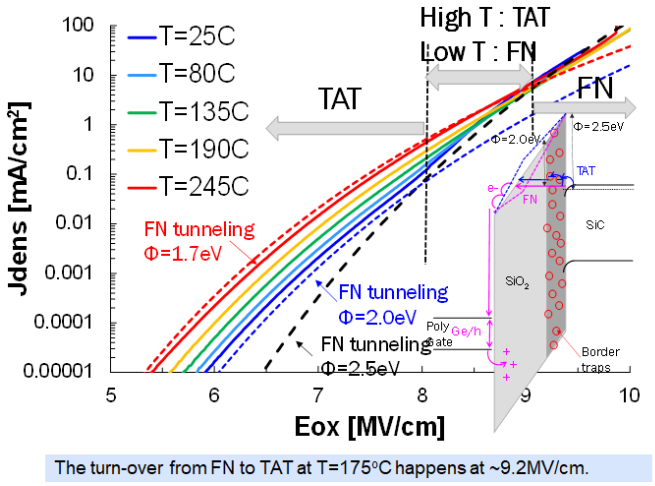


**Figure 7. Competing Current Conduction Mechanisms as Function of Temperature and Electric Fields**

The intrinsic performance of the gate oxide is assessed via Time Dependent Dielectric Breakdown (TDDB) stressing. Gate bias and temperature are combined to stress the SiC MOSFETs, and times−to−failures are recorded. Weibull statistical distributions are then used to extract the lifetimes.

A very conventional approach has been used so far: Arrhenius temperature acceleration and E model for the gate voltage. Additional studies are ongoing to refine the model; the E model is considered too conservative. Stresses at lower oxide fields and long duration (with $t_{63\%}$ of several months to more than a year) are being conducted, and they should experimentally confirm which model best suits the data.

Figure 8 shows TDDB data of SiC production MOSFETs stressed at a temperature of 175°C and at oxide fields where electron trapping occurs (hence below 9 MV/cm, see also Figure 7), for which the same failure mode occurs as expected under real−life conditions. For the lowest stress voltage, times−to−fail over half a year are recorded. Experiments at even lower fields, with an estimated $t_{63\%}$ of 1 to 2 years, are being conducted at a university partner. A 20−year lifetime is reached for $V_{gs}$ = 21 V, well above the specified operating voltage, using the conservative E−model, at 5 ppm.

Figure 9 shows the $I_G(t)$ curves (gate current as a function of stress time) of the individual MOSFET transistors during TDDB stress. The gate current $I_G$ remains constant until reaching a specific envelope curve, after which $I_G$ drops due to the trapped electrons. This envelope curve reflects the trapped charge that the dielectric can sustain before the transistor parameters are affected. This charge is about one decade lower than the charge−to−breakdown ($Q_{BD}$) of the dielectric (i.e., the charge for which the dielectric breaks) and is at par with the $Q_{BD}$ obtained on Si/$SiO_2$ transistors.

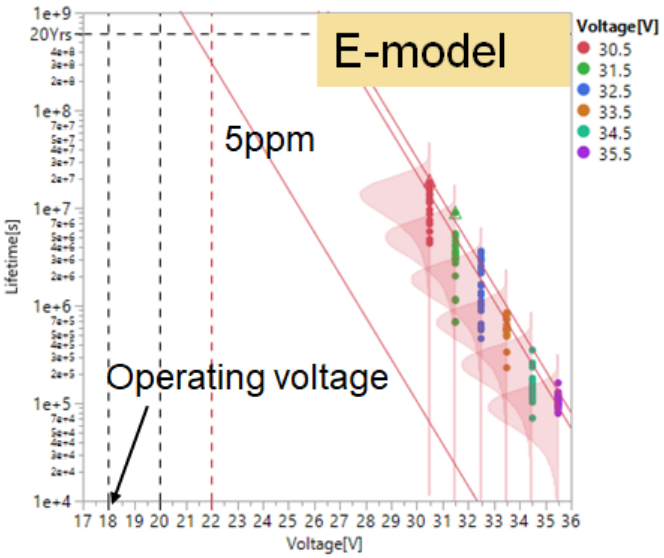


**Figure 8. TDDB Data of SiC Production MOSFETs (Stress at 175°C and Below 9 MV/cm So Under Electron Trapping, See Also Figure 7)**

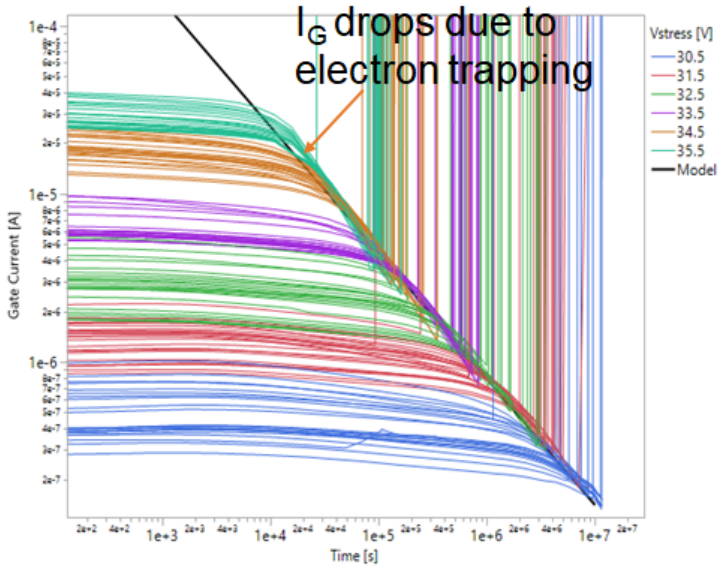


**Figure 9. $I_G(t)$ Curves of the TDDB Data Depicted in Figure 8 (SiC Production MOSFETs Stressed at T=175°C)**

## Published Material

The purpose of this section is to describe recent studies performed at **onsemi** briefly. The related publications are listed in the References section and will provide all details a reader would love to obtain to get deeper into these technical topics.

## Bias Temperature Instability (BTI)

BTI is a well−known degradation mode in the Si world, with threshold voltage drift of the MOSFET due to generation or charging of traps at or near the semiconductor/oxide interface, ultimately leading to a detrimental increase of the on resistance. SiC MOSFETs are also affected, and the fact that one is dealing with a wide bandgap material makes the study more complex. The behavior of the material has to be well understood not only in DC but also in switching mode.

The characterization of the $SiC/SiO_2$ interface and the assessment of its intrinsic reliability has been a focal point at **onsemi** for many years, with the creation of a Research Network to study and improve interface states and mobility, using selected research partners and experimental techniques (see Figure 4).

Static BTI evaluation for ON and OFF states occurs at package level via High Temperature (positive and negative) Gate Bias stressing, including a drift analysis of electrical parameters after stress. Dynamic BTI requires a more comprehensive approach. **onsemi** allocated resources to deeply investigate Ultra−Fast Bias Temperature Instability (UF−BTI), with the measurement and modeling of threshold voltage ($V_{th}$) shifts when applying positive (PBTI) and negative (NBTI) gate stress (or both) as illustrated in Figure 10.

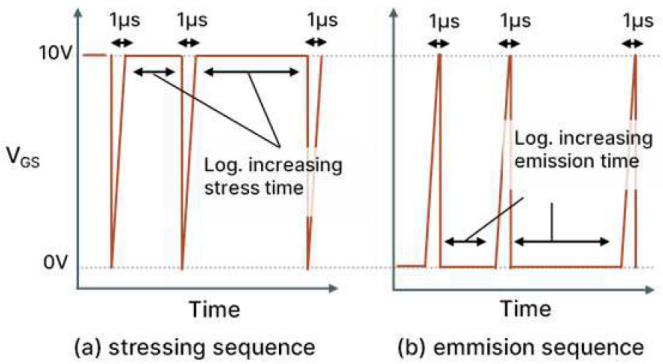


**Figure 10. Schematic Representation of the Stress / Measure / Emission Sequence Used to Investigate Ultra Fast BTI on SiC MOSFETs**

During PBTI, the “apparent” $V_{th}$ will shift to higher voltages (due to capture of electrons), while during NBTI, the “apparent” $V_{th}$ will shift to lower voltages (due to emission of electrons or capture of holes). PBTI has a permanent and recoverable component, and NBTI seems only to have a recoverable part.

A conventional $I_dV_g$ characterization is not able to capture the fast components. But during a typical switching application (100 kHz, so ~ 5 to 10 µs), the fast BTI component will dominate and can become a potential application problem.

**onsemi** collected data down to the µs range and over an extensive range of temperatures, including cryogenic.

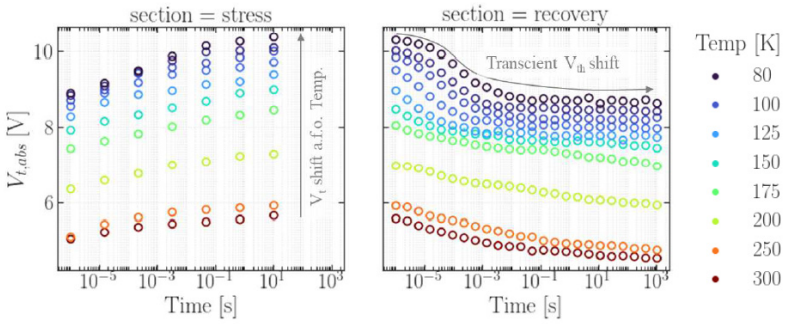


**Figure 11. $V_{th}$ Shift as a Function of Time and Temperature during PBTI at $V_g$ = +10 V and Subsequent Recovery**

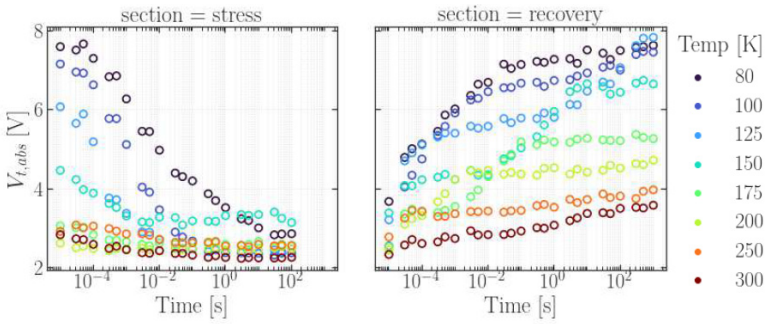


**Figure 12. $V_{th}$ Shift as a Function of Time and Temperature during NBTI at $V_g$ = −10 V and Subsequent Recovery**

The followings steps were:

- The extraction of the Capture & Emission Time (CET) maps ($V_{th}$ shifts result from trapped charges, distributed in energy and space). Figure 11 displays $V_{th}$ shifts during stress and in the subsequent recovery as a 10 V PBTI stress, and in Figure 12 as a −10 V NBTI stress
- The AC and DC modeling of the $V_{th}$ drifts (fast BTI component for the applications and slow BTI component for the long−term intrinsic reliability)
- Extract a physical model (defect type, energy, depth) as shown in Figure 13
- Predict lifetime under real−life application requirements.

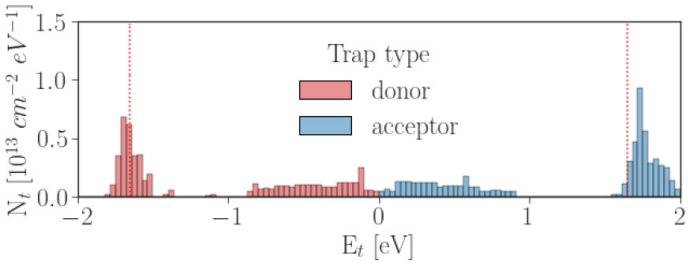


**Figure 13. Fitting of the Absolute $V_{th}$ Shifts after NBTI and PBTI (with the Comphy Model) allows Extracting a Trap Distribution**

The cryogenic UF−BTI study has been presented at ISPSD2022 [4].

### Body Diode Degradation

Bipolar degradation by Body Diode stress in SiC MOSFET can result in an on−state resistance increase triggered by the current flowing through the body diode when it is forward biased. This degradation is sometimes also reported as a drift in forward voltage or increased off−state leakage. The test procedure is described in Figure 14, while Figure 15 shows the forward voltage drop $V_F$ and current $I_D$ during pulsed measurements.

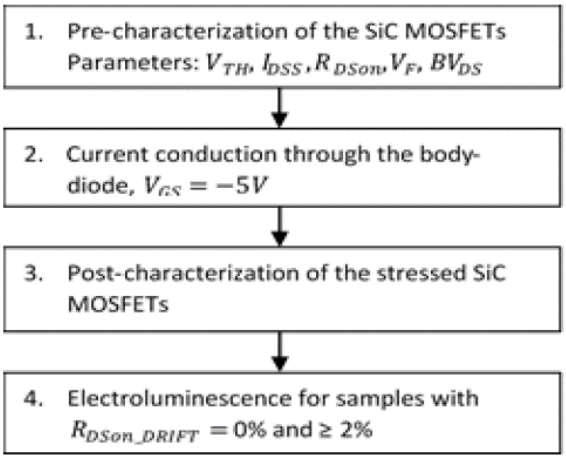


**Figure 14. Test Procedure for Bipolar Degradation**

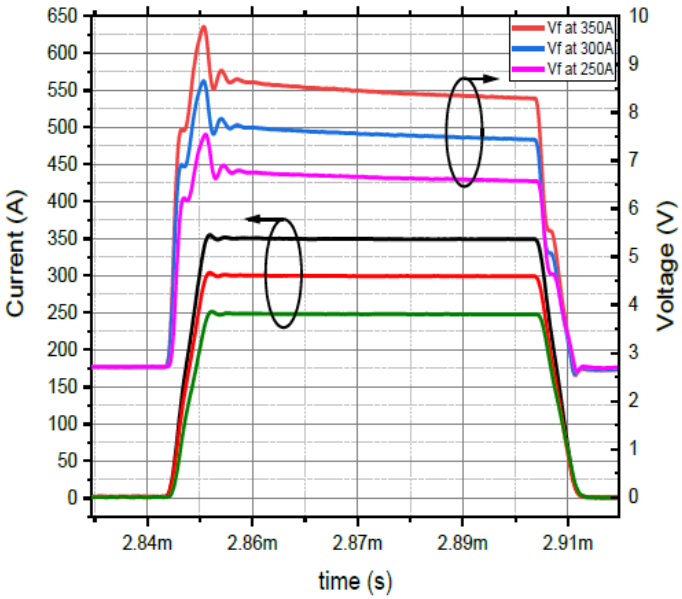


**Figure 15. Transient Measured Body Diode Forward Voltage Drop $V_F$ and Current $I_D$ during Pulsed Current Measurements with 250, 300 & 350 A, and $V_{GS}$ = −5 V**

**onsemi** has extensively assessed this degradation mechanism—most recently publishing a study at ECSCRM2021 [2], performing individual mapping of BPDs in SiC MOSFET dies to establish a correlation between $R_{DSon}$ drift after body diode stress and the number of BPDs in the devices. $R_{DSon}$ and $V_F$ drifts were clearly increasing with the number of BPDs in a device. However, extremely high current densities (J > 1600 A/cm$^2$) had to be used to observe a significant degradation in MOSFETs with no BPD (Figure 16).

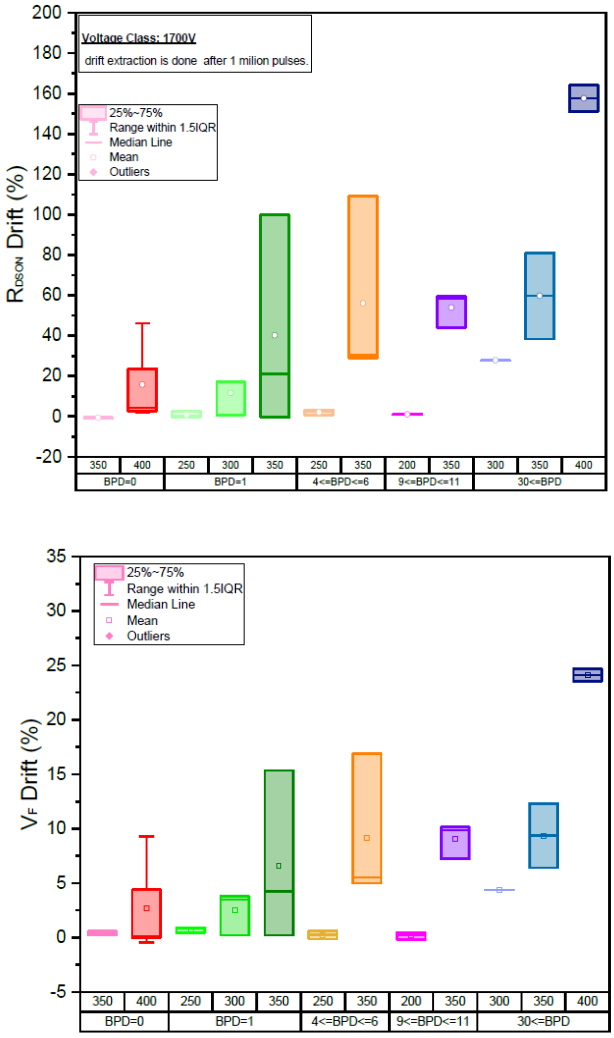


**Figure 16. Drift in $R_{DSon}$ and $V_F$ versus BPD Count on 1700 V 25 mΩ SiC MOSFETs and versus Current. Body Diode Stress of 1 million 50 μs Long Pulses**

**onsemi** implements the following elements for all SiC technology nodes:

- Visual screening is in place, with each production wafer thoroughly scanned for Basal Plane Dislocations (BPDs)
- The epitaxial buffer layer is highly doped, and the development of stacking faults from BPD is limited

- Finally, design rules for maximum current densities have been defined to remain within a safe operating area for each MOSFET.

Thanks to the combination of these three elements, **onsemi** SiC MOSFET technologies up to 1200 V can be considered as not impacted by Body Diode degradation.

### Dynamic Stressing

Degradation under dynamic conditions is one of the concerns related to wide bandgap material. Dynamic stressing studies have been performed at **onsemi** on benches internally developed (limited sample size). We present an example of Room Temperature Dynamic Gate Stress below.

Regarding dynamic stressing events on larger sample sizes (such as three lots of 80 units each), test solutions are presently in development (both internally and with an equipment supplier).

Room Temperature Dynamic Gate Stress: a transient and overshoot−free $V_{GS}$ stress was performed at T = 25°C with $V_{DS}$ = 0 V using a gate driver switching between −8 V and 20 V with a 50% duty cycle [3].

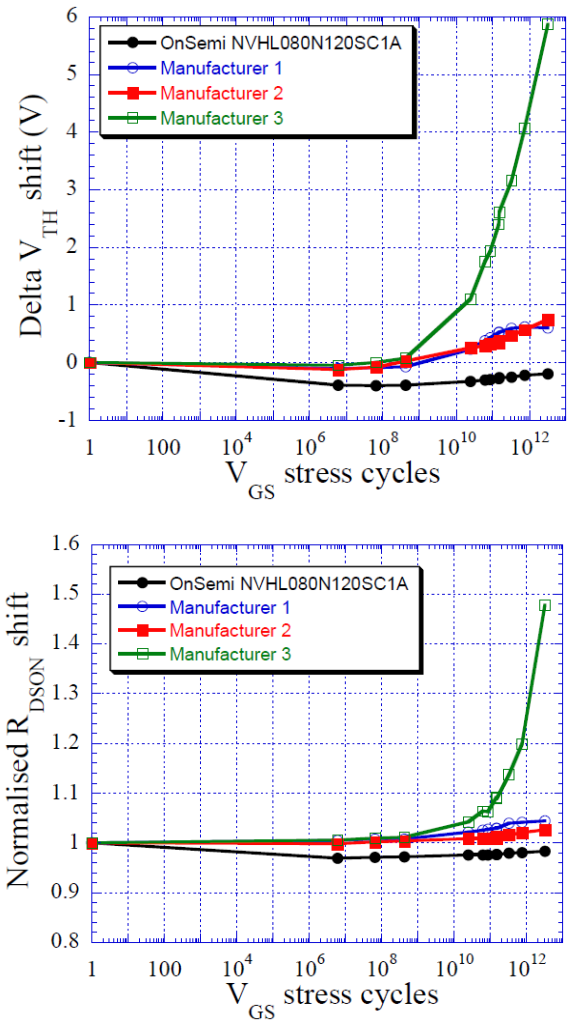


**Figure 17. Shifts of $V_{th}$ and Normalized $R_{DSon}$ for onsemi's Commercially Available 1200 V 80 mΩ SiC MOSFET and 1200 V SiC MOSFET Products from three other Manufacturers**

The stress measurements were interrupted after different time intervals to run a test program consisting of $V_{th}$ and $R_{DSon}$. The shifts of $V_{th}$ and normalized $R_{DSon}$ shifts are shown in Figure 17 for **onsemi**'s commercially available 1200 V 80 mΩ SiC MOSFET together with 1200 V SiC MOSFET products from three other manufacturers ($V_{GS}$ = −8 V being outside the datasheet rating for two of them).

## Conclusion

As illustrated in this white paper, **onsemi** has developed a comprehensive and cross−functional methodology to assess and safely release SiC products to the market.

The combination of a rigorous design methodology, strict production monitoring, manufacturing control, adequate screening, and robust qualification plans is the foundation of robust and reliable SiC products.

The paper briefly addressed some specific SiC challenges as an introduction to how they have been characterized and modeled at **onsemi**.

Our published material provides more details about the physics−based studies performed at **onsemi** (see References for the most recent ones).

## References


[1] A Charge−to−Breakdown (QBD) Approach to SiC Gate Oxide Lifetime Extraction and Modeling − P. Moens[1], J. Franchi[1], J. Lettens[1], L. De Schepper[1], M. Domeij[1], F. Allerstam[1] − [1]**onsemi** − ISPSD 2020

[2] Pulsed forward bias body diode stress of 1700 V SiC MOSFETs with individual mapping of basal plane dislocations − S. Kochoska[1], M. Domeij[1], S. Sunkari[1], J. Justice[1], H. Das[1], H. Lee[1], X.Q. Hu[1], T. Neyer[1] − [1]**onsemi** − ECSCRM 2021

[3] Gate oxide reliability and $V_{th}$ stability of planar SiC MOS technology − M. Domeij[1], J.Franchi[1], S. Masloughkas[1], P. Moens[1], J. Lettens[1], J. Choi[1], F. Allerstam[1] − [1]**onsemi** − ECSCRM 2021

[4] Cryogenic Ultra−Fast Bias Temperature Instability Trap Profiling of SiC MOSFETs − F. Geenen[1], F. Masin[2], A. Stockman[1], C. De Santi[2], J. Lettens[1], D. Waldhoer[3], M. Meneghini[2], T. Grasser[3], P. Moens[1] − [1]**onsemi**, Belgium; [2]Università degli Studi di Padova, Italy; [3]Technischen Universität Wien, Austria − ISPSD 2022





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