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TECHNICAL NOTE

INTRODUCTION

This technical note has been written to clarify some of the terminology used to describe the operation and performance of solid state image sensors. It is intended for use by anyone considering using these sensors in a systems design, and particularly for first time users. This note provides only brief explanations of the common terms encountered in image sensor specifications. A listing of suggested readings on solid state image sensors and applications is located at the end of this document.

CONTENTS

Accumulation Mode

Accumulation mode, also referred to as MPP mode (Multi−Pinned Phase) is the state in a semiconductor where the majority carrier concentration at the oxide−semiconductor interface is greater than the substrate or bulk carrier concentration. When applied to solid state image sensors, the accumulation mode of operation can result in greatly reduced dark current and dark pattern noise.

Accumulation is achieved by applying the appropriate voltage levels to the CCD and transfer gates. For an n−type buried channel CCD, the majority carriers are holes. To attract holes to the SiO_2−Si interface, a voltage sufficiently less than the substrate potential must be applied.

Image sensors which gain the most benefit from running in accumulation mode are those which operate under long integration times. Not all image sensors can support the accumulation mode of operation. Many image sensors have ESD protection circuitry at the inputs to protect the sensor, and these circuits often limit the negative swing of the applied voltages to greater than −1.0 Volts.

Active Area

The surface area of an image sensor which is light sensitive is called the active area. In the case of interline and linear sensors, this area is usually made up of only the photodiode active area, since all other regions on the imager are typically covered with a metal layer which prevents incident light from being absorbed within the silicon substrate. The area of the light sensitive CCD or photodiode (Lp x Wp) may be greater than the active area (La x Wa), in which case the metal light shield is used to define the smaller active area. In full−frame sensors, the active area is defined by this light shield.

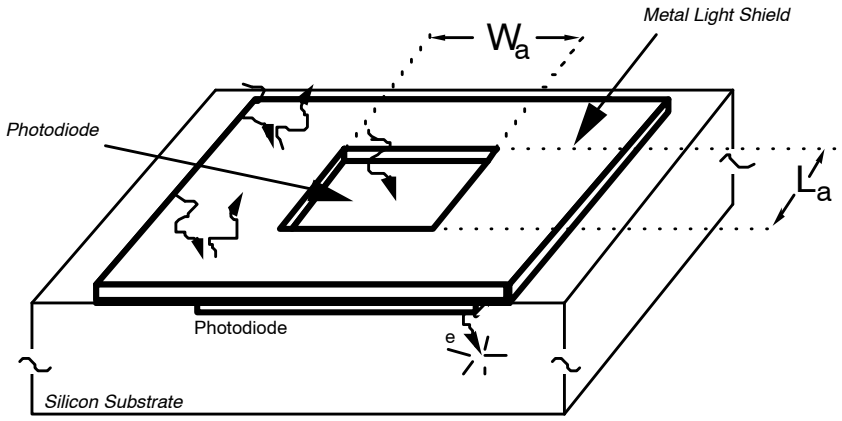

Figure 1. Photodiode with Aperture Light Shield

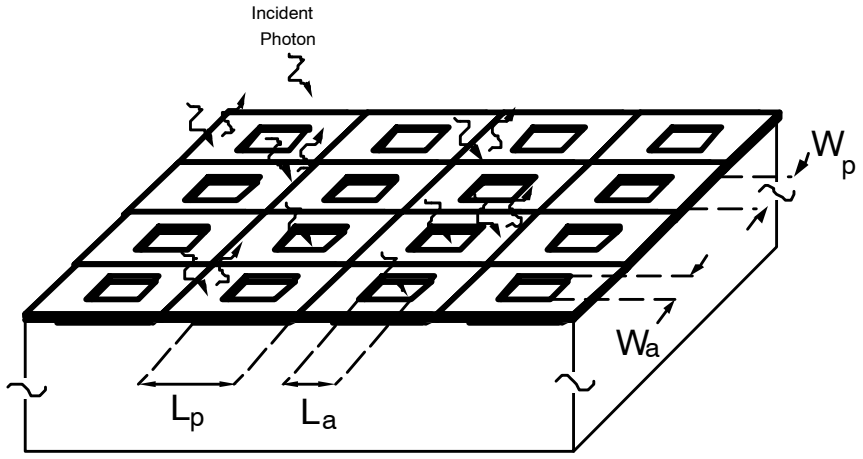

Figure 2. Array of Photodiodes

Blooming

When the maximum charge capacity of the CCD or photo−diode is exceeded, the excess charge will overflow into adjacent CCD cells or photosites. This overflow of photogenerated charge is termed Blooming. The result of blooming is a corrupted image near the blooming site. The extent of the image degradation is dependent on the level of excess charge and on the architecture of the imager being used. The effects of blooming can be minimized by incorporating an antiblooming structure near the charge

collection site. Antiblooming structures are constructed so as to provide a safe path for the excess photogenerated charge (i.e. blooming charge). Vertical antiblooming structures reside below the charge collection site and allow excess charge to overflow directly into the substrate; whereas, lateral antiblooming structures reside adjacent to the charge collection site and allow excess charge to overflow into a reversed biased diode. Clocking schemes may be used to reduce blooming; however, these are less effective at higher frame rates.

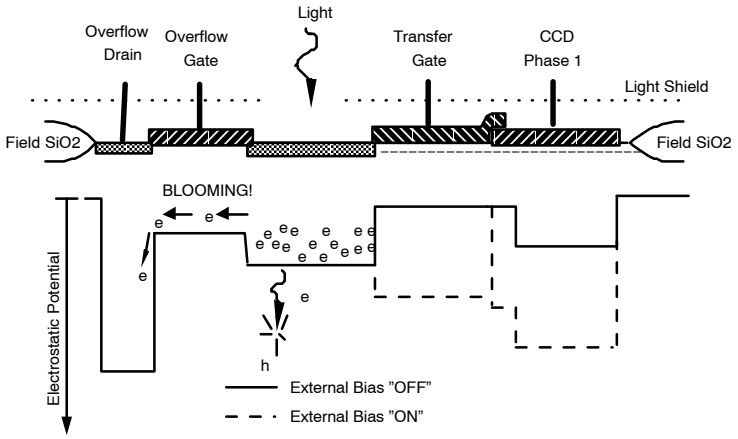

Figure 3. Lateral Overflow Structure

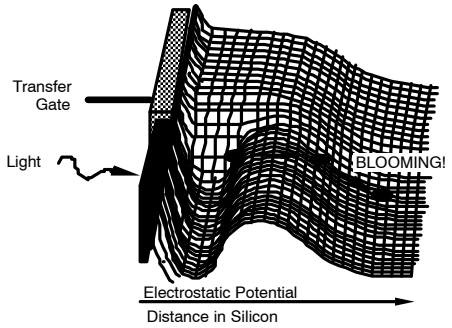

Figure 4. Vertical Overflow Structure

Buried Channel CCD

The Charge Coupled Device (CCD) structure can be used in image sensors to transport and collect photogenerated charge.

The physical location of charge contained within a CCD stage measured with respect to the surface of the silicon substrate is called the channel.

A buried channel CCD is one in which the channel is located some distance below the surface of the silicon. That is, below the silicon – silicon dioxide interface (Si–SiO_2 interface), which is known to contain a higher density of electron traps and a higher dark current. Transferring charge at or near the Si–SiO_2 surface can degrade the charge transfer efficiency (especially at higher CCD clocking speeds) and cause an increase in dark noise.

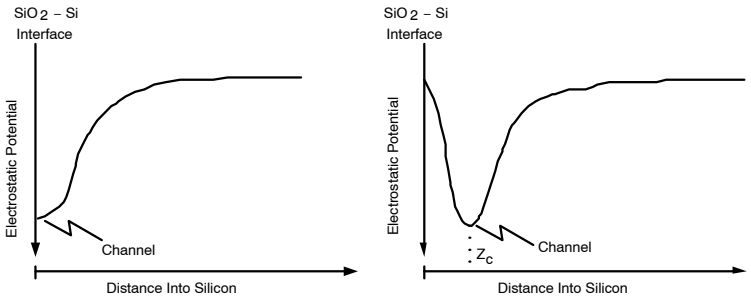

Figure 5. Surface Channel / Buried Channel

CCD Clock

Charge Coupled Devices (CCDs) use input timing signals to setup the electrostatic potentials necessary to transport charge. A two phase CCD will require two input signals, a three phase will require three signals, and a four phase CCD will require four input signals. The amplitude of the CCD input signals, combined with the built in channel potential of each phase, will determine the magnitude of the electrostatic potential under each phase, and the phase relationships between the input clocks will permit the transportation of charge.

For a two phase CCD, two input timing signals are required for operation. For charge to move from phase 1 (Φ1) to phase 2 (Φ2), it is necessary that the phase 1 signal turn "OFF" (external bias = 0.0 V) and phase 2 signal turn "ON" (external bias ≥ VCCD V). Similarly, the phase 2 signal should be "OFF" and the phase 1 signal "ON" to transport charge from phase 2 to phase 1. This results in two input timing signals which are complements of each other, as shown below. The "ON" / "OFF" duty cycle of each clock is typically 50%, but may vary as long as the "ON" / "OFF" times meet the specification requirements and the signals remain complements of each other.

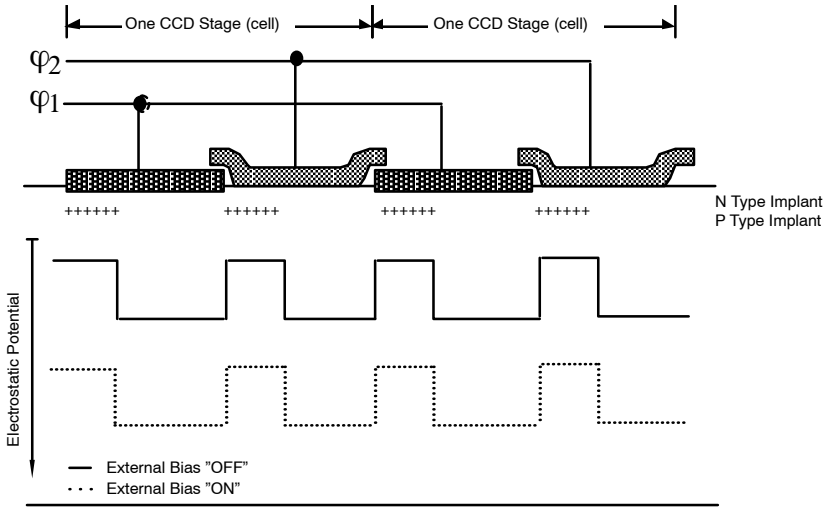

Figure 6. Cross Sectional View of True Two Phase CCD

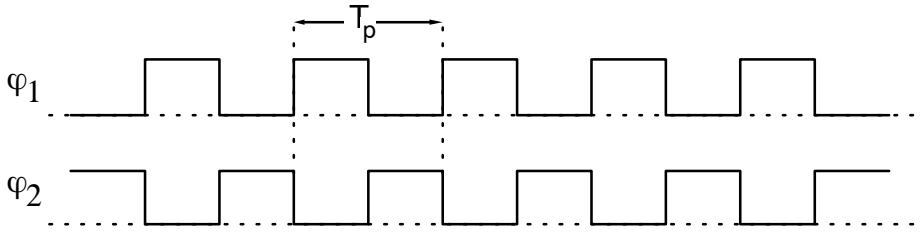

Figure 7. Input Timing for Two Phase CCD

The point at which the complementary clock signals cross (e.g. 50% of amplitude) is very important for optimum operation. The phase 1 and phase 2 signals are controlled differently during the photodiode to CCD charge transfer. Once the charge transfer is complete, the CCD signals again resume the complementary pattern.

Charge Capacity

The maximum amount of charge that an imager can collect and transfer while maintaining all performance specifications is termed the saturation charge level and defines charge capacity. Charge capacity may be limited by either the photosite or CCD capacity. If the charge capacity is exceeded, the excess charge will overflow into adjacent structures and produce artifacts known as blooming and smear. If an anti−blooming structure is adjacent to the charge collection site, the excess charge will be prevented from overflowing into adjacent charge collection and transport structures; thus, prevent blooming from occurring.

Multiplying the charge capacity (N_{sat}) by the charge−to−voltage conversion factor yields that maximum output voltage, or saturation voltage.

$$V_{sat} = N_{sat} \times \frac{dV}{dN} \text{ [Volts]} \qquad \text{(eq. 1)}$$

Charged Coupled Device

A Charge Coupled Device (CCD) is an integrated circuit which allows individual charge packets to be transferred over a physical distance while maintaining the original

charge packet integrity. Charge coupled devices are ideally suited for use in solid state imagers as a means of transferring integrated photogenerated charge. The CCD may be used to collect the photogenerated charge, or it may be placed adjacent to a array of photodiodes or photocapacitors. A CCD used to directly collect photogenerated charge will have reduced photoresponse at shorter optical wavelengths due to the presence of polysilicon electrodes. Several of the more common CCD structures are described in more detail in other sections of this reference document.

Charge Transfer Efficiency

Charge Transfer Efficiency (CTE) is the fraction of charge which is successfully transferred during one CCD transfer cycle (note that a phase CCD will have two transfer cycles per CCD stage). CTE is equal to one minus the Charge Transfer Inefficiency (CTI), or:

$$CTE = 1 - CTI \quad \text{(eq. 2)}$$

Some manufacturers define CTE as the charge transferred per CCD stage, so care should be taken when comparing different manufacturer's specifications for CTI and CTE to ensure that both use the same definition. The total charge remaining in a CCD stage after being clocked through the entire CCD is termed the CTE per line for linear imagers or CTE per frame for area array image sensors, and is equal to:

$$CTE_{Line} = (CTE)^{CCD\_Transfers} \quad \text{(eq. 3)}$$

(for Linear Image Sensors)

$$CTE_{Frame} = (CTE_X)^{X\_CCD\_Transfers} \times (CTE_Y)^{Y\_CCD\_Transfers} \quad \text{(eq. 4)}$$

(for Area Array Image Sensors)

Charge Transfer Inefficiency

Charge Transfer Inefficiency (CTI) is the fraction of charge left behind during a CCD transfer.

Care should be taken when comparing different manufacturer's specifications for CTI or CTE to ensure that both use the same definition.

Charge Transfer Inefficiency is measured by injecting a sequence of charge packets of known size into a CCD and then monitoring the resultant imager output waveform. Note that a two phase CCD will have two transfers per CCD stage. The injected signal amplitude and the signal lost from the injected signal are then used to calculate CTI as follows:

$$CTI = \frac{N_{lost}}{N_{infected} \times CCD\_Transfers} = \frac{V_{lost}}{V_{infected} \times CCD\_Transfers} \quad \text{(eq. 5)}$$

Color Filter Array (CFA)

For color imaging applications, it is necessary to separate the optical spectrum of the incident image into three color bands. In most applications, it is desirable to perform the color separation on the imager. Color separation is typically accomplished by depositing organic dyes on the imager surface. The color dyes, or color filters, can be configured to work in an additive (RGB) or subtractive (YMC) process. That is, the deposited layers may act as transmission filters or as absorbing filters. The deposition of three color filters yields three bandpass filters, which can be designed to occur in any pattern across an imager.

On tricolor linear imagers, a blue bandpass filter is deposited on one whole channel, a green bandpass filter is deposited one another channel, and a red bandpass filter is deposited on the remaining channel. Thus, a single pass scan of an object obtains all color information. Color filter patterns on area arrays can also occur in varying arrangements.

Correlated Double Sampling (CDS)

A schematic diagram of a typical image sensor output stage and the corresponding image sensor timing are shown below. The output stage functions as follows. The reset gate signal (ΦR) is turned "ON" to reset the floating diffusion node. Then reset is turned "OFF" and the output signal is allowed to settle. Next the phase 2 CCD clock (Φ2) is turned "OFF" and the phase 1 CCD clock (Φ1) turned "ON". As the phase 2 CCD clock turns "OFF", the charge in the last phase 2 stage is dumped onto the floating diffusion node and the output signal is allowed to settle at its new value. Finally, the reset gate signal is again turned "ON" and the cycle repeats.

The voltage level of the output signal after the reset gate has turned "OFF" and before phase 2 is turned "OFF" is called the reset level. This level is typical in the range of 7 to 9 volts. The reset level will have a noise component due to variations in the effective "ON" resistance of the reset transistor (Q1). This noise is very small, but detectable in very high dynamic range systems.

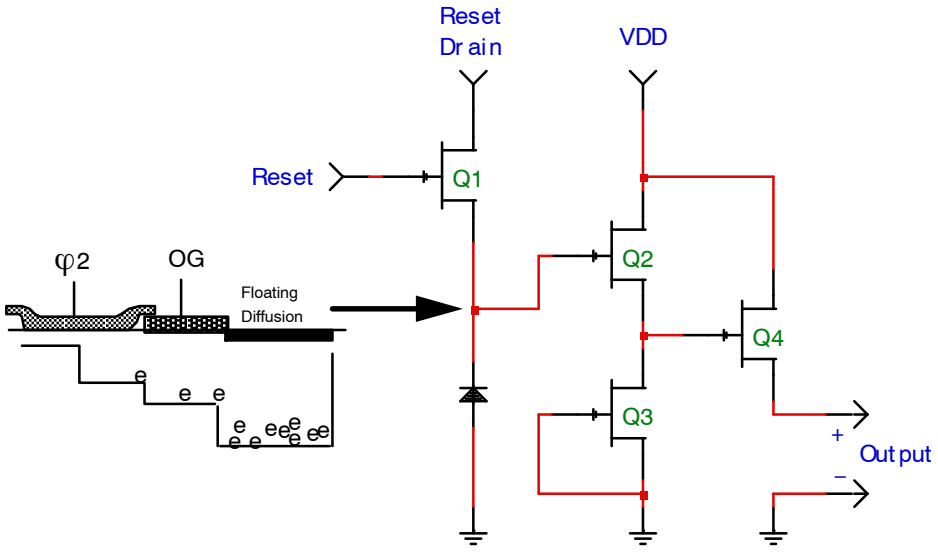

Figure 8. Output Circuitry

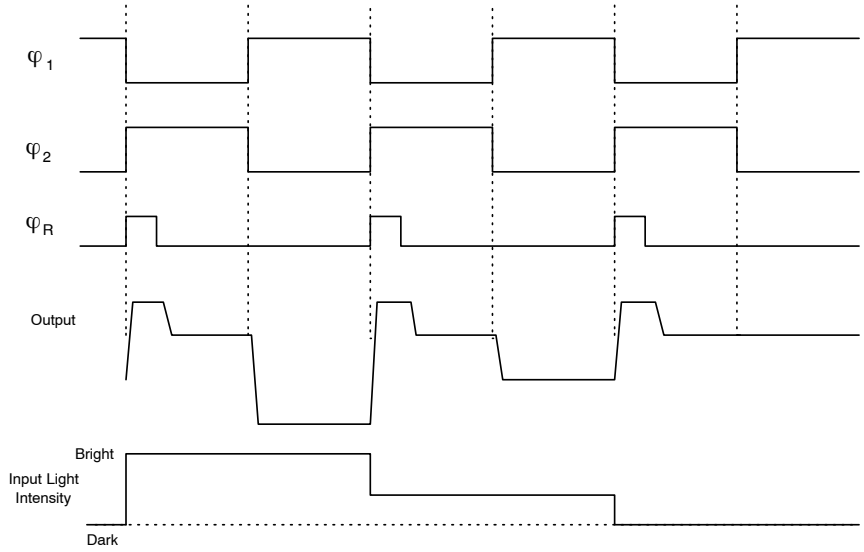

Figure 9. Signal Timing

Typical saturation voltages are in the range of 1 to 3 volts. This makes the lowest level of the output signal about 4 volts (7 − 3). Most analog−to−digital converters will not accept inputs signals in this range, so some signal processing must be performed on the output signal.

The goals of processing the output signal are to (1) remove the reset level noise, and (2) translate the output signal to a level acceptable by analog to digital converters. Goal number 1 is met by performing a differential measurement on each photosite (also known as Correlated Double Sampling, or CDS), and goal number 2 is achieved by converting the output signal to a ground referenced, positive going signal.

The timing required to perform the CDS signal processing is shown below. There are several common circuits used to perform the CDS function; however, all make a differential measurement.

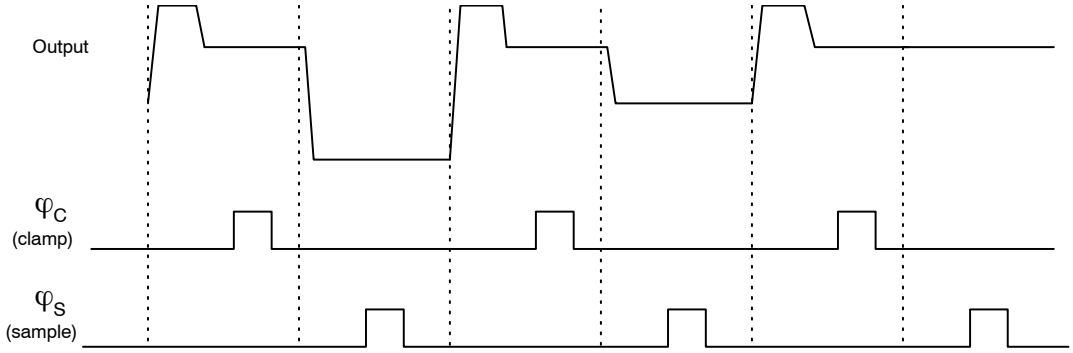

Figure 10. CDS Timing Signals

One method is to AC couple the output signal and then clamp it to ground during the flat reset portion of the signal. Variations in the output which occur after the clamp is complete will be with respect to ground. Then the ground referenced signal is passed through an inverting amplifier, resulting in a positive going ground referenced signal. Only one additional sample pulse is required to complete the processing by sampling the signal during the active portion of the signal (i.e. during the time when the phase 2 CCD input is "OFF").

The clamped and sampled signal is then ready for direct input into an analog−to−digital converter.

Another method uses two sample pulses to charge one capacitor to the reset level and another to the active portion of the output. The two signals are then fed into an inverting differential amplifier where a difference measurement is performed and the signal is converted to a positive going, ground referenced signal.

Dark Current

Dark signal is a termed used to refer to the background signal present in the image sensor readout when no light is incident upon the image sensor. This background signal is a result of thermally emitted charge being collected in the photosites transfer gates, and CCDs. The magnitude of the dark signal is dependent on the image sensor architecture, mode of operation (see "Accumulation Mode"), and on the image sensor operating temperature. Due to the present of localized defects in the silicon substrate, the dark signal collected in each pixel will vary from pixel to pixel. This variation in dark signal is called the dark signal noise. The average current associated with the readout of a complete dark image is referred to as the dark current. The dark current will double for approximately every 9°C increase in image sensor temperature.

Dark Reference Pixels

Dark reference pixels are groups of photo−sensitive pixels covered by a metal light shield. These pixels are used as a black level reference for the image sensor output. Since the incident light is blocked from entering these pixels, the signal contained in these pixels is due only to dark current. It is assumed that each photo−sensitive pixel (active and dark reference) will have approximately the same dark signal; thus, subtracting the average dark reference signal from each active pixel signal will remove the background dark signal level. Dark reference pixels are typically located at one or both ends of the arrays, as shown below for a linear image sensor.

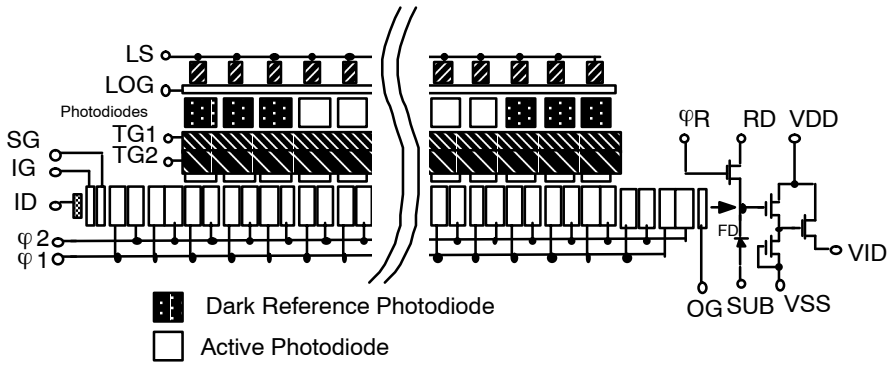

Figure 11. Single Channel of Linear Image Sensor

Data Rate

The data rate is the total number of pixels being clocked off an imager over a period of time. If the imager has only one output, then the data rate is typically equal to the horizontal CCD clocking rate. An imager with two outputs will have a data rate equal to two times the horizontal CCD clocking rate, assuming both outputs are clocked out in parallel.

Defective Pixel

A defective pixel is one whose response to illumination variations differs significantly from the mean response of all other pixels. The maximum deviation from the mean response permitted is imager as well as application dependent. The number and type of defects acceptable is also application dependent, and can range from zero to as many as 1000 defects in some cases. It is sometimes possible to remove the effect of the defective pixel by applying one of several signal processing defect correction algorithms. One of the simplest such algorithms is to replace the defective pixel with the average response of the two nearest neighboring pixels, i.e.

$$P_d = \frac{1}{2}(P_{d-1} + P_{d+1})$$

Dynamic Range

Dynamic Range (DR) is the ratio of the maximum output signal, or saturation level, of an image sensor to the dark noise level of the imager. The dark noise level, or noise floor of an imager, is typically expressed as the root mean square (rms) variation in dark signal voltage. The dark signal includes components from dark current within the photosite and CCD regions, reset transistor and output amplifier noise, and input clocking noise. An input referred noise signal in the charge domain can be calculated by dividing the dark noise voltage by the imager charge−to−voltage conversion factor. The dynamic range is typically expressed in units of decibels as:

$$DR = 20 \log\frac{V_{sat}}{V_{Dark,rms}} = 20 \log\frac{N_{sat}}{N_{Dark,rms}} \quad [dB] \qquad \text{(eq. 6)}$$

Electronic Shutter

An electronic shutter is used to vary the effective integration time (T_{eff}) of a group of pixels. The circuitry used to perform the shuttering drains all charge out of the photosensitive pixel for a fraction of the total integration time (T_{int}). When used on tri−linear image sensor arrays, the electronic shutter can be used to balance the color response of the red, green and blue channels.

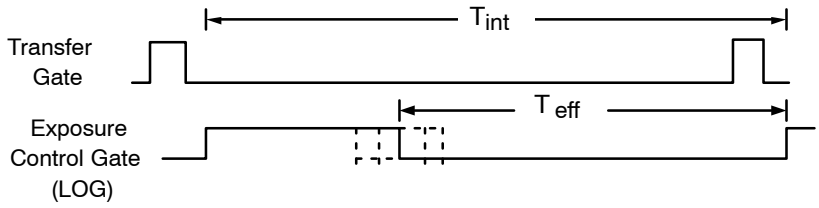

Figure 12. Typical Electronic Shutter Timing

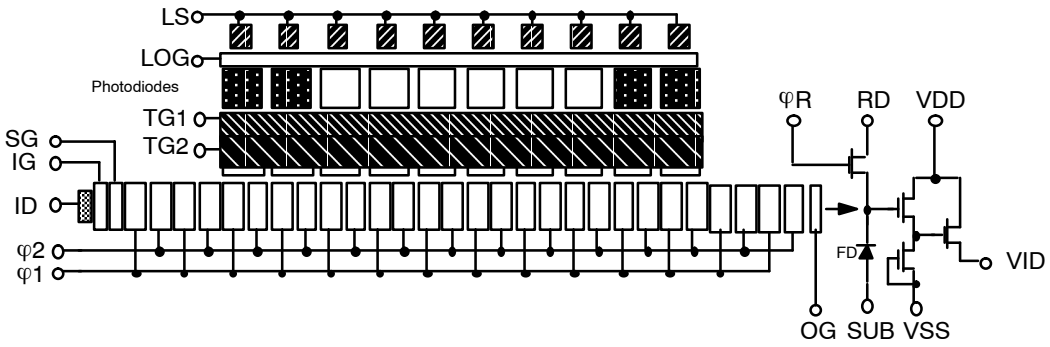

Figure 13. Single Channel of Linear Image Sensor

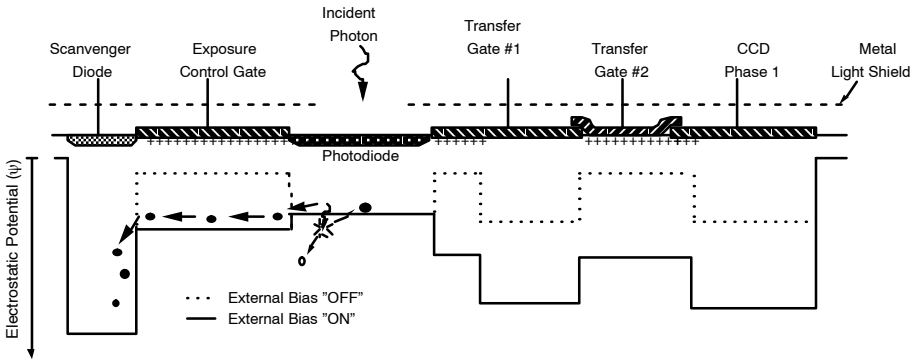

Figure 14. Cross Sectional View of Lateral Electronic Shutter

Fill Factor

The fill factor is the ratio of the light sensitive area to the total photosite area. Fill factor on some types of area arrays can be improved using lenlets (see “Lenticular Array (Microlenses/Lenslets)”).

Fixed Pattern Noise

If the output of an image sensor under no illumination is viewed at high gain a distinct non−uniform pattern, or fixed pattern noise, can be seen. This fixed pattern can be removed from the video by subtracting the dark value of each pixel from the pixel values read out in all subsequent frames. Dark fixed pattern noise is usually caused by variations in dark current across an imager, but can also be caused by input clocking signals abruptly starting or stopping or by having the CCD clocks not being close compliments of each other. Mismatched CCD clocks can result in high instantaneous substrate currents, which when combined with the fact that the silicon substrate has some non−zero resistance can result in the substrate potential bouncing. The pattern noise can also be seen when the imager is under uniform illumination. An imager which exhibits a fixed pattern noise under uniform illumination and shows no pattern in the dark is said to have Light pattern noise or Photosensitivity pattern noise. In addition to the reasons mentioned above, light pattern noise can be caused by the imager entering saturation, the non−uniform clipping effect of the antiblooming circuit, and by non−uniform, photosensitive pixel areas often caused by debris covering portions of some pixels.

Floating Diffusion

The floating diffusion is the charge sensing node used to convert the charge packets carried by the CCD into a voltage change which can be detected at the imager output. The term floating diffusion describes the charge sensing node structure, which is typically formed by implanting and diffusing a N−type dopant into a P−type substrate. During operation, the N side of the diode (the diffusion) is reset to a positive potential by the reset transistor (Q1) and then allowed to float. When charge is subsequently dumped onto the floating diffusion a proportional change in voltage occurs. The change in voltage due to a charge packet of size N on the charge sensing node will be V = q N / C, where C is the effective node capacitance and q is the elementary charge.

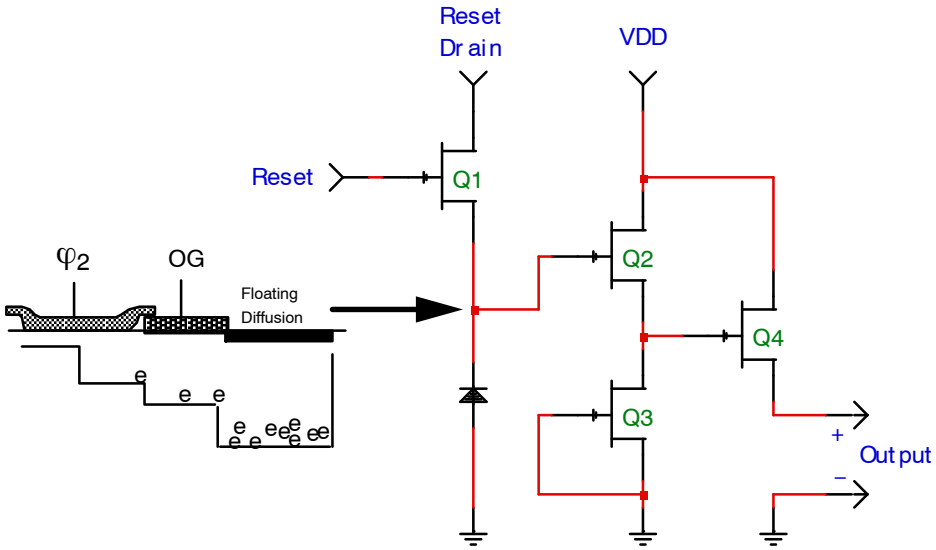

Figure 15. Typical Image Sensor Output Amplifier

Four Phase CCD

A four phase CCD is one which requires four polysilicon electrodes to make up one CCD cell. Four phase CCDs require four input clocks to properly transport charge.

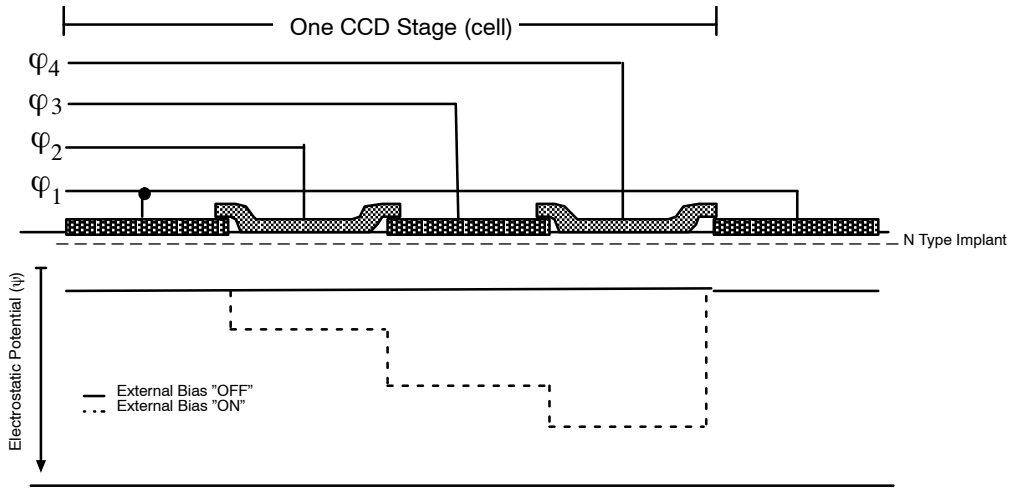

Figure 16. Four Phase CCD

Frame Rate

The frame period (T_p) of an imager is the time elapsed between successive image readouts, and the frame rate is the number of images which can be read out during one second ($F_p = 1/T_p$).

Frame Transfer Image Sensors

A frame transfer image sensor is similar to the full frame imager with the addition of an optically isolated frame storage region. These devices operate by first turning “OFF” the vertical CCDs and opening the external shutter. At the end of the integration time, the image in region A is quickly transferred into region B, which is not light sensitive. The vertical CCDs are again turned “OFF” and the external shutter opened to acquire the next image. At the same time the image in region B is clocked out of the imager one line at a time.

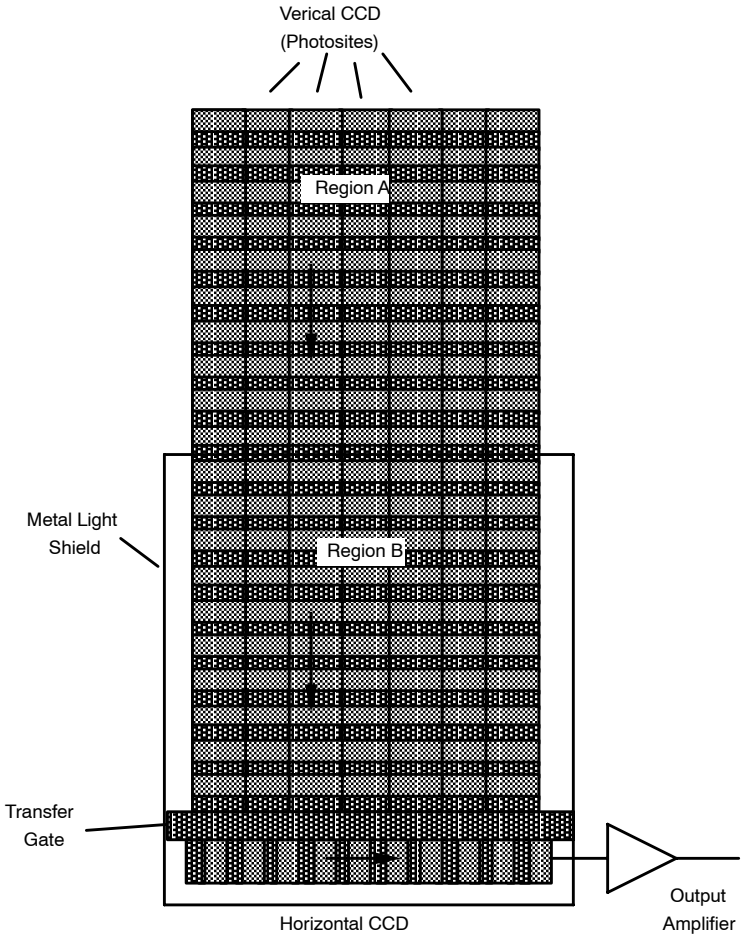

Figure 17. Full Frame Transfer Image Sensor

Full Frame Image Sensor

An area array which uses the CCDs to both collect photo−generated charge and transport the charge into a horizontal CCD is termed a Full−Frame Image Sensor. Since most portions of the image sensor are photo−sensitive, an external shutter is required to remove incident light before any charge transferring begins.

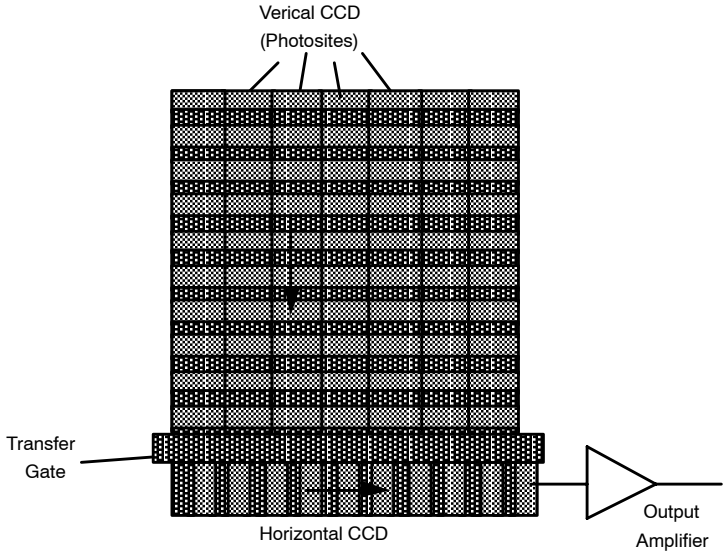

Figure 18. Full Frame Area Image Sensor

Horizontal CCD

Horizontal CCDs are used to transfer photosite charge packets to the output amplifier. In area image sensors, the charge packets are first transferred into the vertical CCDs and then into the horizontal CCD. In linear image sensors, the photosite charge packets are transferred directly into the adjacent horizontal CCD. Since linear image sensors use only one orientation of CCD, the horizontal prefix is dropped.

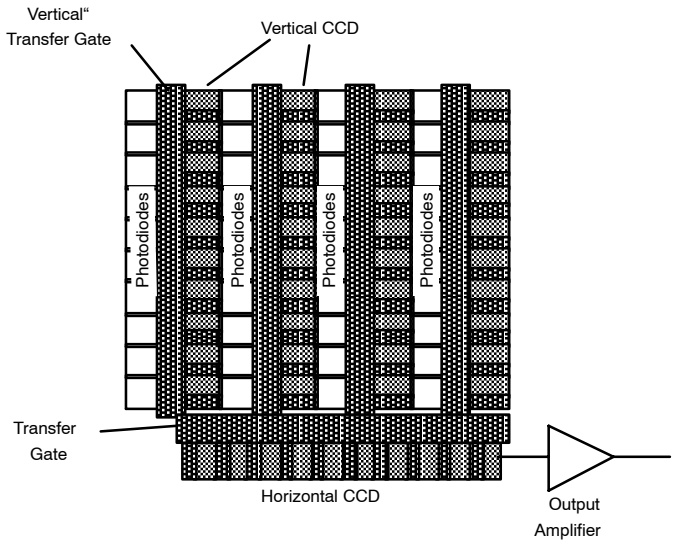

Figure 19. Orientation of CCDs on Area Image Sensor

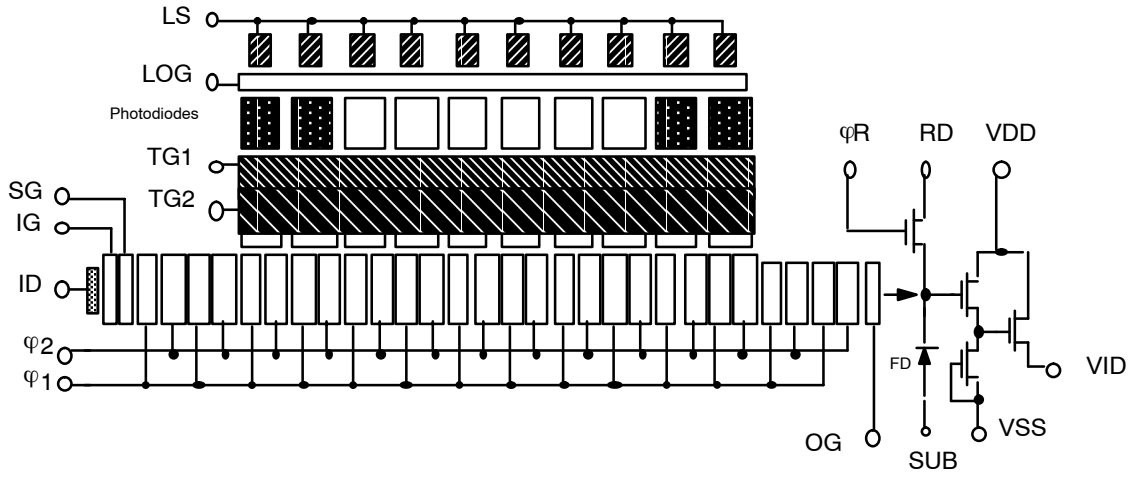

Figure 20. Orientation of CCD on Linear Image Sensor

Image Sensor

A device capable of converting an incident optical pattern (i.e. image) into an electronic signal which contains all spatial and intensity relationships of the original pattern. The term is usually used to refer to solid state semiconductor image sensors.

Integration Period

The integration period is the total time the image sensor collects photons from the incident light pattern. Image sensors with electronic shutters can have effective integration times less than the actual integration period.

Interlaced Image Sensor

An interlaced image sensor is one which transfers out a portion of the image being integrated during one frame and the remaining section of the image during the next frame. NTSC compatible interlaced imagers output the odd field of the image and then the even field of the image. An interlaced display, like the typical NTSC compatible television, writes every odd line of the image (e.g. lines 1, 3, 5, ... etc.) to the display, and then writes all even lines of the image to display. If the two images are written quickly enough (< 1/30 second), then the viewer will be unable to detect the individual fields.

Interline Image Sensor

An interline image sensor has a light shielded CCD adjacent to each photosite array. An area array interline image sensor and a linear interline image sensor are depicted below. Note that only the photosite arrays are not covered by the aluminum light shield, so while one image is being integrated the previous image can be safely transferred out of the image sensor. Interline imager sensors, unlike full−frame devices, do not require an external shutter.

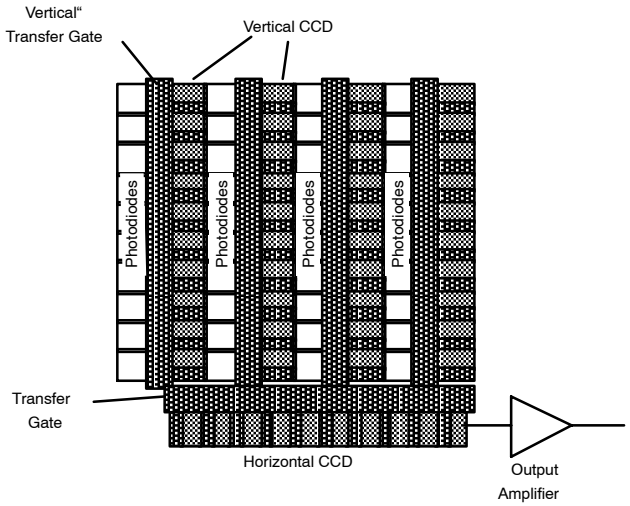

Figure 21. Interline Area Array Image Sensor

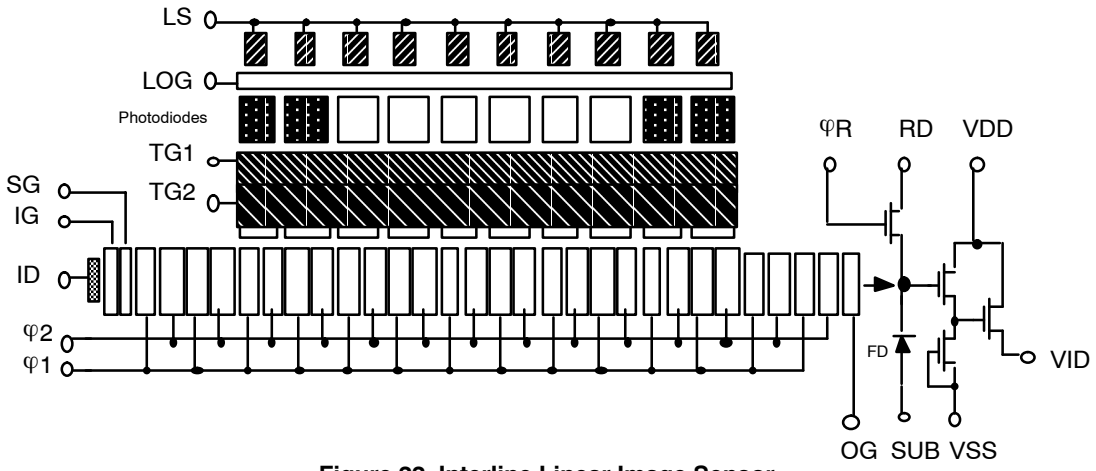

Figure 22. Interline Linear Image Sensor

Lateral Overflow Drain

See “Blooming” for a complete description.

Lenticular Array (Microlenses/Lenslets)

Interline array imager sensors and array imagers with lateral overflow drains suffer from reduced optical fill factor; that is, the active area of a pixel is significantly less than the total pixel area. One way to increase the effective active area on such devices is to manufacture a tiny optical lens, or lenslet on each photosite. Increases in effective area of 2 to 3 times can be achieved. This in turn increases the photosite responsivity by an equal factor.

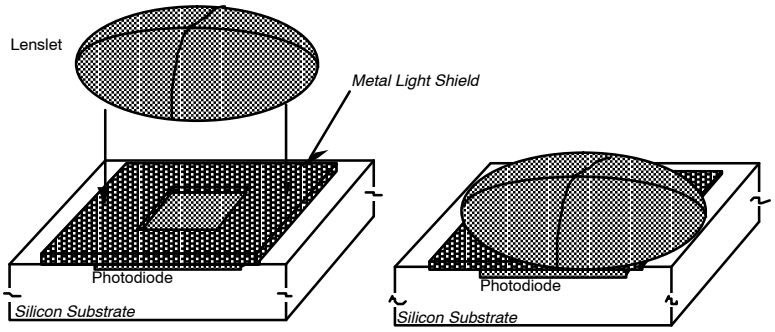

Figure 23. Lenslets are Fabricated over Photodiodes

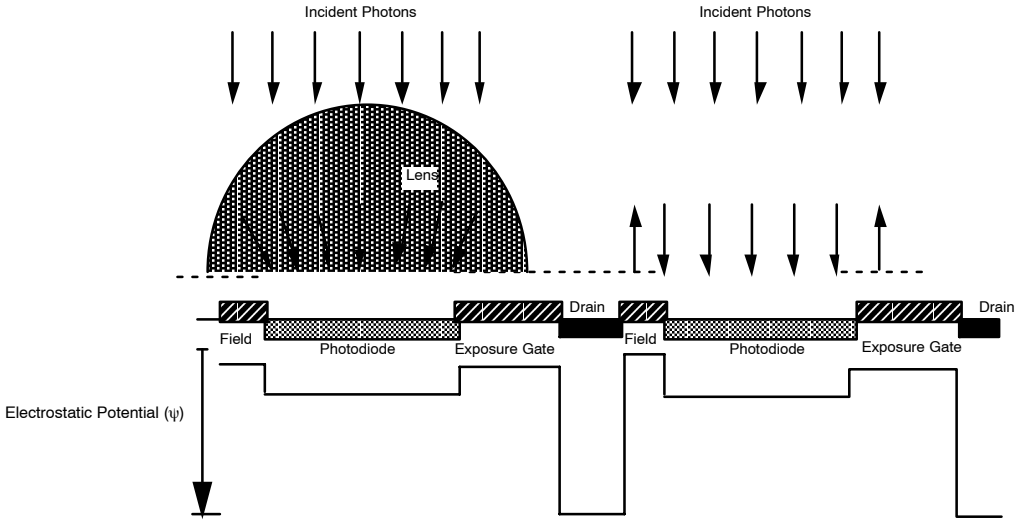

Figure 24. Effect of Lenslets is to Increase the Effective Active Area

Light Shield

A light shield is a layer of non−translucent material deposited on all areas of the image sensor except the photosensitive portion of the pixels. The light shield material is usually aluminum and will reflect a portion of the incident light and absorb the rest. The light shield is often electrically connected to scavenger diodes located about the imager perimeter and biased to a positive voltage.

Linear Image Sensor

A linear image sensor is one which contains one or more linear arrays of photosites. Associated with each photodiode array is at least one CCD and one charge sensing amplifier. Linear imager sensors are ideally suited for scanning applications such as paper copiers, fax machines, and film scanners.

A tri−linear image sensor is one which has three parallel linear photosites arrays, each with its own CCD and output amplifier. It is common practice to sequentially fabricate red, green, and blue bandpass filters such that each one of the arrays is uniquely covered by one of the primary colors to yield an image sensor which can obtain full color information with a single scan over the document.

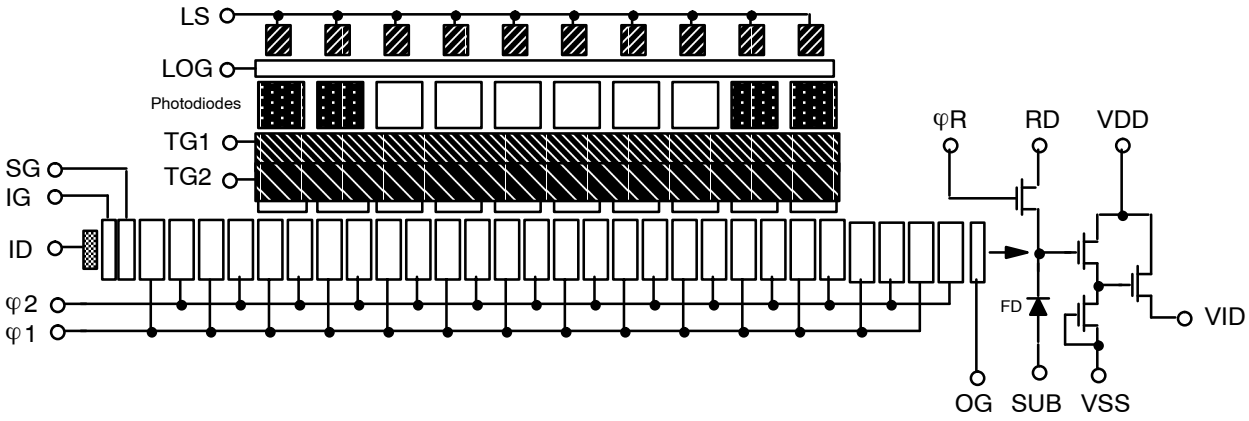

Figure 25. Single Channel of a Typical Linear Image Sensor

Modulation Transfer Function (MTF)

MTF is the magnitude of the spatial frequency response of a solid state imager. The three main components of imager MTF are termed the aperture MTF, diffusion MTF, and charge transfer efficiency MTF. The aperture MTF results from the discrete sampling nature of solid state imagers, with smaller pixel pitches yielding a higher MTF response. The diffusion of photogenerated charge degrades the imager response and is responsible for the second component. The third component is due to inefficient charge transfer in the shift register. The maximum frequency an imager can detect without aliasing occurring is defined as the Nyquist frequency and is equal to one over two times the pixel pitch. MTF is typically reported at the Nyquist frequency, 1/2 Nyquist, and 1/4 Nyquist. The aperture MTF limits the maximum response at Nyquist to 0.637 (Note that the maximum MTF response is 1.0). The diffusion component will further degrade this value, especially at longer optical wavelengths.

Multiple Outputs

An image sensor with multiple outputs is designed to divide up the photosite array(s) into sections. Each section can be readout using CCDs to a unique output amplifier. The advantage of an image sensor with multiple outputs is that the integrated image can be read out of the imager N times as faster, where N is the number of outputs. The outputs may be read out in parallel to increase the data rate, or may be output in a particular sequence to ease the task of image reconstruction.

Noise

Noise is any unwanted signal added to the imager output. Temporal noise sources present in a typical imager include the dark current, photon shot noise, reset transistor noise, CCD clocking noise, and the output amplifier noise. Dark current is dependent on the imager operating temperature and can be reduced by cooling the imager. The reset transistor noise can be removed using correlated double sampling signal processing. The photon shot noise cannot be eliminated; however, by acquiring and averaging several frames it, and all temporal noise sources, can be reduced.

The variation in dark current from pixel to pixel leads to a dark noise pattern across an imager. The effects of this dark pattern noise can be minimized by averaging several frames and then using the pixel−referenced, dark frame data as the zero reference level for each pixel.

Non−Interlaced

See “Progressive Scan”.

Output Amplifier

The photogenerated charge collected by the photosites is transferred to the output amplifier using a CCD. The output amplifier must then convert each charge packet into a corresponding voltage change at the device output pin. The circuit frequently used to accomplish this task is show below. This circuit consists of a two stage source follower amplifier with the biasing load for the last stage contained off chip. It is noted that the typical operating voltages for VDD and the reset drain are 10 to 15 volts.

The charge−to−voltage conversion begins by turning “ON” the reset transistor (Q1) at the same time the phase 2 CCD clock is turned “ON” (see region A in Figure 27). This action clears all charge off the floating diffusion node and resets the node voltage to the reset drain voltage. Due to the gate−to−source capacitance of Q1, the reset gate clock will feed through to the floating diffusion node, resulting in an output voltage slightly higher than the reset drain voltage. This feed through voltage disappears when the reset transistor is turned “OFF”, as depicted in region B. The last step is to simultaneously turn phase 1 “ON” and phase 2 “OFF.” This action causes the charge located in the phase 2 region of the last CCD stage to flow onto the floating diffusion, resulting in a decreased node voltage (see region C in Figure 27).

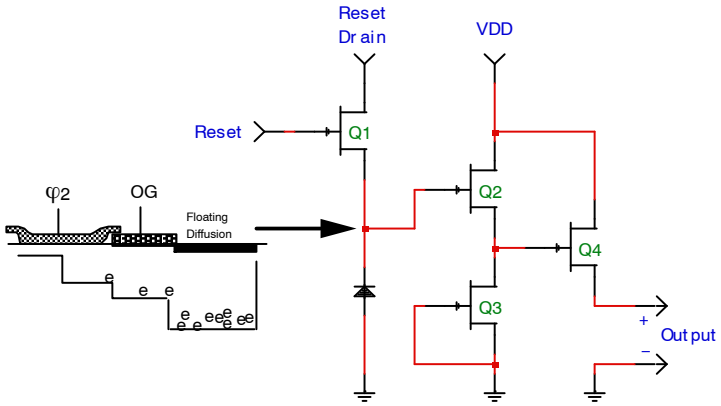

Figure 26. Typical Solid State Imager Output Amplifier

The magnitude of the voltage drop is determined by the capacitance of the floating diffusion node (i.e. Vout = Q / C_{fd}).

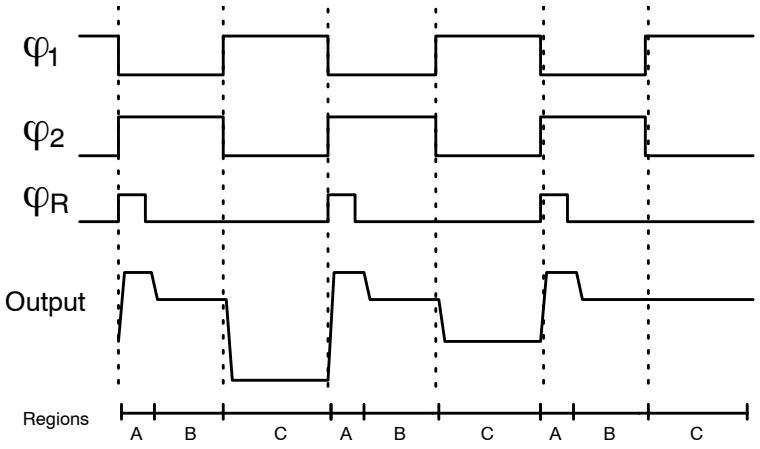

Figure 27. Corresponding Output Waveform

Transistor Q3 is a constant current bias for the first stage source following transistor Q2. The second stage source follower transistor (Q4) is designed to drive much higher loads than Q2, which implies higher drive currents. To minimize the power dissipation on the image sensor, the biasing load for Q4 is often located off the device (i.e. on the driver board). Depending on the expected application, some devices are designed with on chip bias loads for Q4. Since the dark current level (thermal noise level) doubles for every 9°C change in temperature, it is desirable to keep as much power dissipation off the device as possible. If the output amplifier dissipates significant power, the localized temperature around the amplifier will increase. This in turn will result in a temperature gradient across the device, which leads to a dark current gradient across the device.

Output Linearity

The non−linearity of an image sensor is typically defined as the percent deviation from the ideal linear response, which is defined by the line passing through Vsat and Vdark. The percent linearity is then 100 minus the non−linearity. The output linearity of a solid state image sensor is determined from the linearity of the photon collection process, the electron exposure structure nonlinearities (if it exists), the efficiency of charge transportation from the photosite to the output amplifier, and the output amplifier linearity.

The absorption of photons within the silicon substrate can be considered an ideal linear function of incident illumination level when averaged over a given period of time. The existence of an electronic exposure control circuit adjacent to the photosensitive sites can introduce a non−linearity into the overall response by allowing small quantities of charge to remain isolated in unwanted potential wells. Whether or not any potential wells exist depends on the design and manufacturing of the particular image sensor. The existence of such potential wells in the exposure circuitry, also called exposure defects, will degrade the linearity only at small signal levels and may be different from one photosite to the next. An image sensor with excessive exposure defects would be rejected during quality assurance testing.

The loss of charge during the transportation of charge packets from the photosite to the CCD, which is termed lag, tends to affect the linearity only at very small signal levels.

"Pinned" photodiodes, or buried photodiodes, have extremely small lag (< 0.5%), and can be considered to be lag free. The CCD charge transfer inefficiency (CTI) will reduce the amplitude of the charge packet as it is transported towards the output amplifier, with the greatest effect realized at very small signal levels. Modern CCD's have CTE in excess of 0.999999 per CCD transfer; thus, the overall effect on linearity is generally not a concern. If biased properly, the output amplifier will yield a nonlinearity of typically less than 2%.

Non linearity at signal levels beyond the saturation level is expected and can often vary significantly from pixel to pixel.

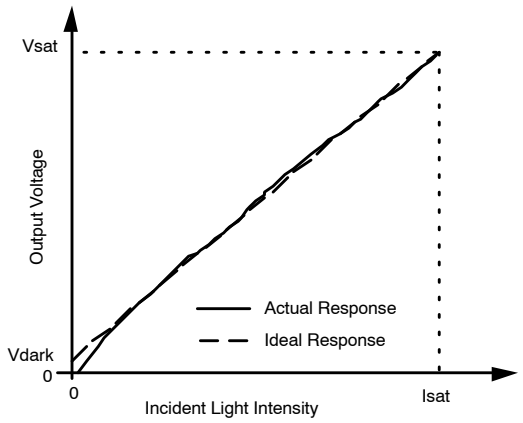

Figure 28. Definition of Non−Linearity

Output Sensitivity

The output sensitivity of an imager is defined as the ratio of the change in output voltage for a given quantity of charge transferred onto the charge detection node (i.e. floating diffusion). This is also referred to as the charge−to−voltage conversion factor (dV/dN). Noting that the voltage at a given node is equal to the charge on the node divided by the node capacitance (V = Q/C), the change in output voltage is seen to vary linearly with the change in charge, or:

$$\Delta V = \frac{\Delta Q}{C} \qquad \text{(eq. 7)}$$

To maximize the output sensitivity, the floating diffusion node capacitance (C) is made as small as possible. A typical value for the node capacitance is 20 to 50 fF ($20 - 50 \times 10^{15}$).

Photodiode Lag

Photodiode lag is defined as the percentage of total charge transferred from the photodiode to the adjacent CCD which remains in the photodiode after the transfer period is complete. Ideally, the lag should be zero (i.e. all charge is transferred). Certain types of photodiodes have much higher values of lag than others. For example, a standard PN photodiode will have the highest lag while a "pinned" photodiode will have the smallest. The origins of lag can be understood by picturing the reversed biased PN diode acting as a photon collection site. A reversed biased PN junction results in a space−charge region (also called depletion region) extending into both semiconductor types, with the majority on the lighter doped side. As photogenerated charge is collected, the space−charge region collapses. At the end of the integration period, an adjacent Transfer gate potential is increased by applying an external bias and the collected charge is allowed to flow into the adjacent CCD. As the charge flows out of the photodiode the space−charge region begins to extend back to the starting boundaries. At the tail end of this process, the photodiode potential approaches the value of the adjacent transfer gate potential, and the flow of charge is subject to sub−threshold effects. That is, the driving potential between the photodiode and the transfer gate becomes significantly small.

The result is that the last portion of charge will not be transferred as quickly as the first portion. The net effect is that not all charge is transferred out of the photodiode. The remaining charge will appear in the readout of the next lines or frames where the photosite is not illuminated. "Pinned" photodiodes have greatly improved lag performance due to the construction of the space−charge region. A "pinned" photodiode is created by making a P+NP type structure.

If the P+ implant is made sufficiently high, the N type region will be totally depleted and will have an associated electro−static potential independent of the adjacent transfer gate potential during the charge transfer process. The net effect is that a substantial potential difference can be maintained between the photodiode and the transfer gate during the whole transfer period, regardless of the amount of remaining charge in the photodiode.

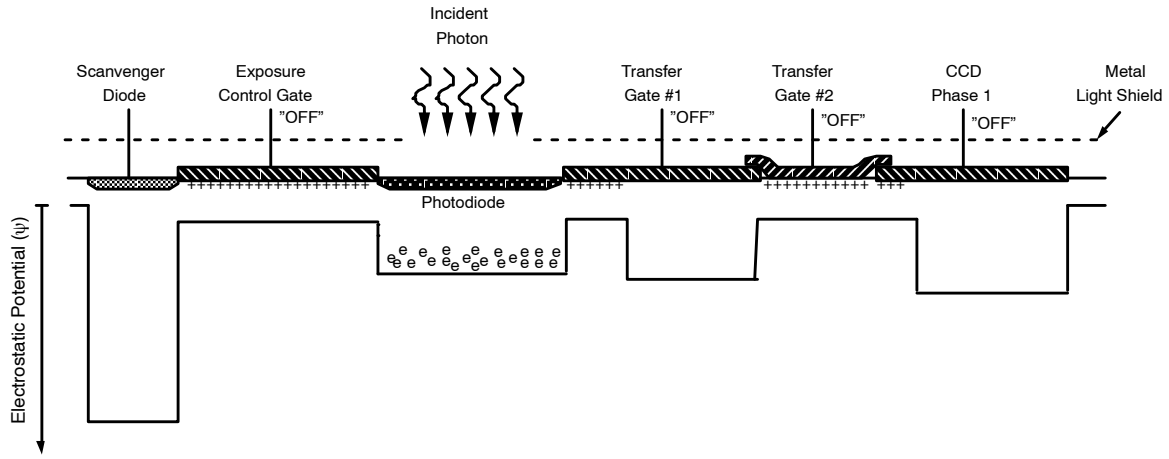

Figure 29. (1) Lag−Integrating Bright Line

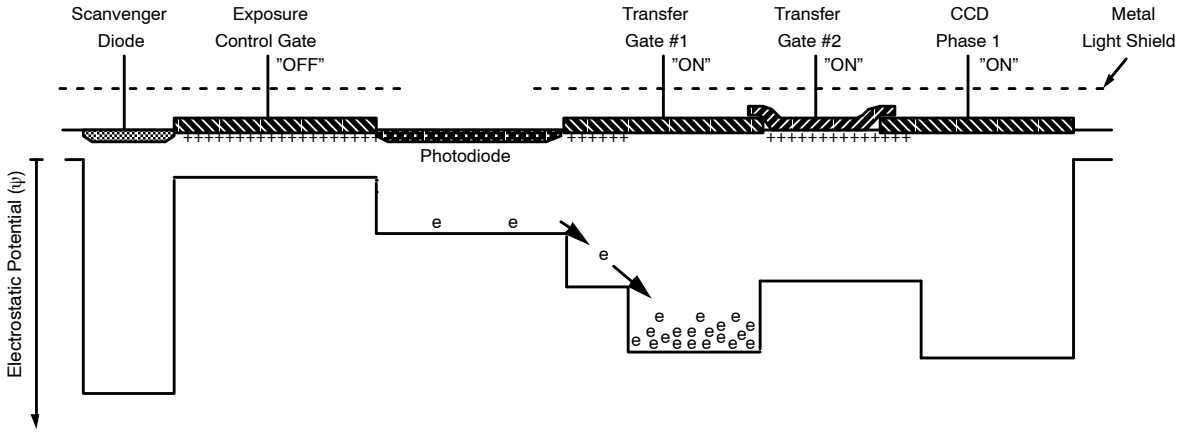

Figure 30. (2) Lag−Light Removed, Transfer Begins

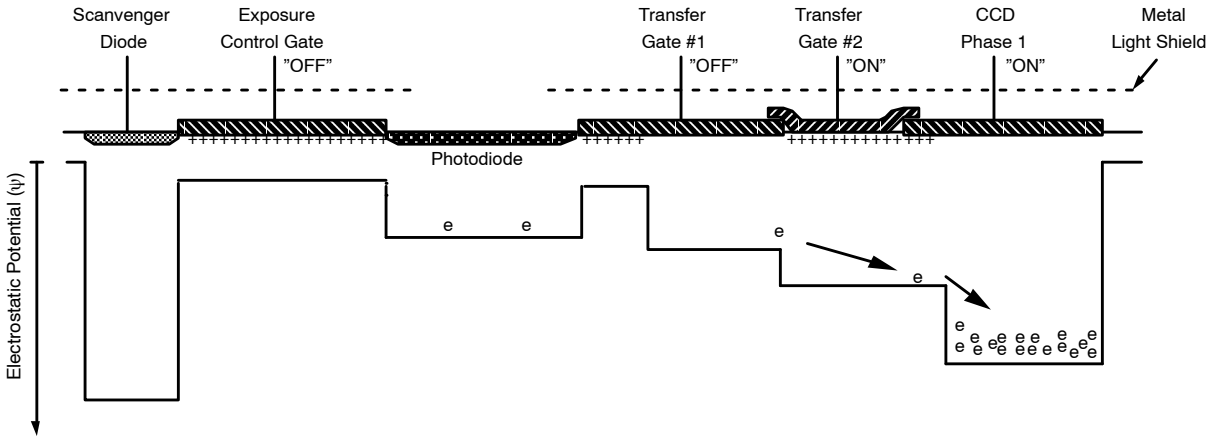

Figure 31. (3) Lag−Transfer Continues

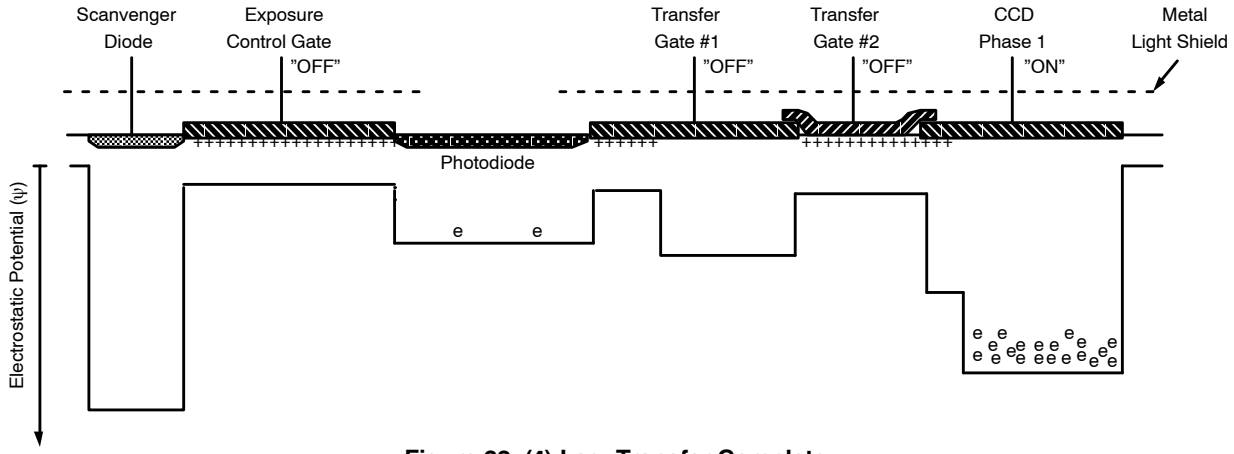

Figure 32. (4) Lag−Transfer Complete

Photoresponse Nonuniformity

The peak−to−peak variation in output signal under uniform illumination of the image sensor is called the Photoresponse Nonuniformity (PRNU). PRNU is very small for monochrome imagers (i.e. imagers with no color filters), since the only varying factors are the photosite quantum efficiency, the dark current, and the effective active area. These factors typically are very uniform across an imager. Color imagers have higher PRNU due to slight variations in the external color filters. Variations in color filter thickness will cause some photosites to have higher or lower photoresponse than others. These variations can be minimized using proper fabrication techniques and care during the design phase to minimize variation due to topology across the imager.

Pixel

A pixel is an individual photosite which has the ability to collect photogenerated charge and restrict the location of the charge to a discrete volume of space within the silicon substrate. Photodiodes and photocapacitors are two types of pixels, since both can collect and hold photogenerated charge. There is usually a one−to−one correspondence between the number and arrangement of pixels on an imager and the display device (e.g. CRT) used to view the captured image.

Pixel−to−Pixel Crosstalk

The absorption of a photon in silicon generates an electron−hole pair. The depth at which the absorption process occurs has a lot to do with whether or not the photogenerated electron will be collected within the potential well of the photosensitive pixel through which the photon originally entered. If absorption occurs within the photosensitive pixel space−charge region (1) (see Figure 34), the photogenerated electron will be collected by the built−in electric field. Since there are no electric fields below the space−charge region, electrons generated in this region (2) (see Figure 34) are free to randomly diffuse until they recombine in the substrate or are captured by a photosite or CCD register structure. Electrons generated below the space−charge region of a photodiode which are captured in a neighboring photosensitive pixel constitute pixel−to−pixel crosstalk. The effect of this type of crosstalk is to reduce the spatial resolving power (MTF) of the imaging array.

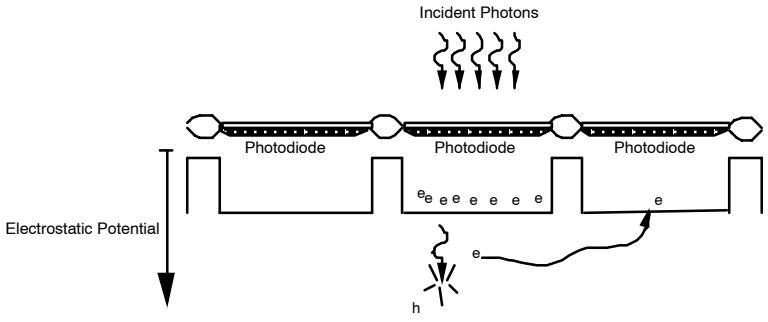

Figure 33. Absorption of Photons Below the Space−Charge Region

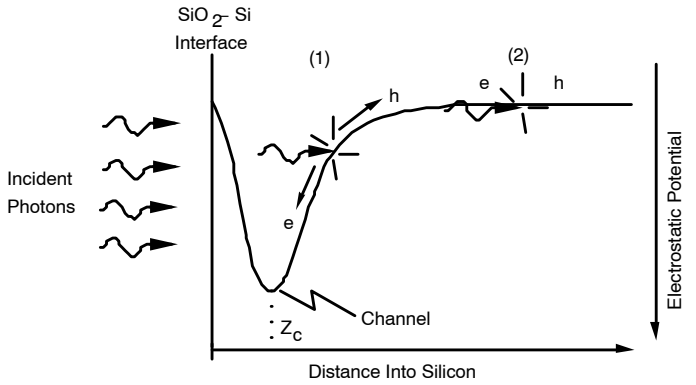

Figure 34. Space−Charge Regions 1 and 2

It is known that photons of longer wavelength, such as from red light, have a mean absorption depth greater than photons of shorter wavelength, such as from blue light. This phenomena means that red light will produce higher pixel−to−pixel crosstalk than green light, and green light will produce higher crosstalk than blue light. The percent of photons absorbed within the silicon substrate is shown below as a function of wavelength and absorption depth. A typical photosensitive pixel space−charge region depth is also indicated on Figure 35. As an example, it can be seen that 90% of all 520 nm photons will be absorbed within the space−charge region, but only 42% of all 670 nm photons will be absorbed.

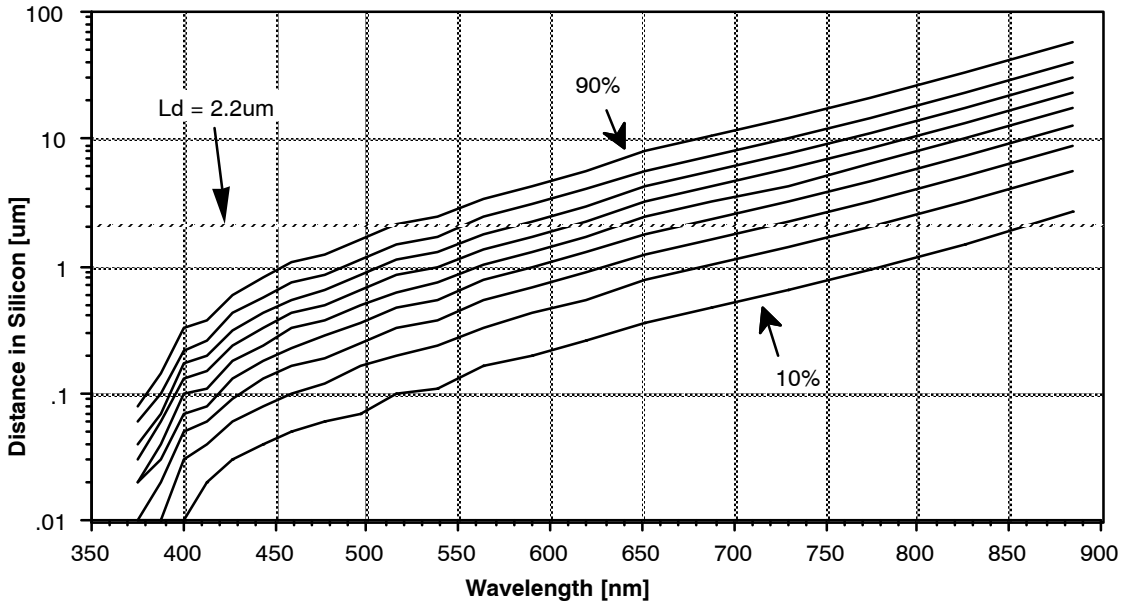

Figure 35. Percent of Photons Absorbed in Silicon versus Wavelength and Depth

Potential Well

A potential well is a localized region within a semiconductor substrate which has a higher electrostatic potential then the surrounding area. A region of increased electrostatic potential is equivalent to a region of reduced potential energy, since P.E. = −q x V, where q = magnitude of electronic charge and V is the electrostatic potential. Electrons introduced into an area of a potential well will be confined to that area until they recombine, are thermally emitted out of well, or are forced from the well by the application of an external force (e.g. external voltage). A potential well can be created by the application of an external bias to a MOS type structure (e.g. a CCD gate), creating a dynamic deep depletion region, or by setting up a variation if doping concentration, or both.

A CCD structure can be thought of as a MOS capacitor with two different potentials built in near the silicon surface. Dynamically applying an external voltage (potential) to the MOS capacitor will cause both potentials to increase or decrease, depending on the polarity of applied voltage.

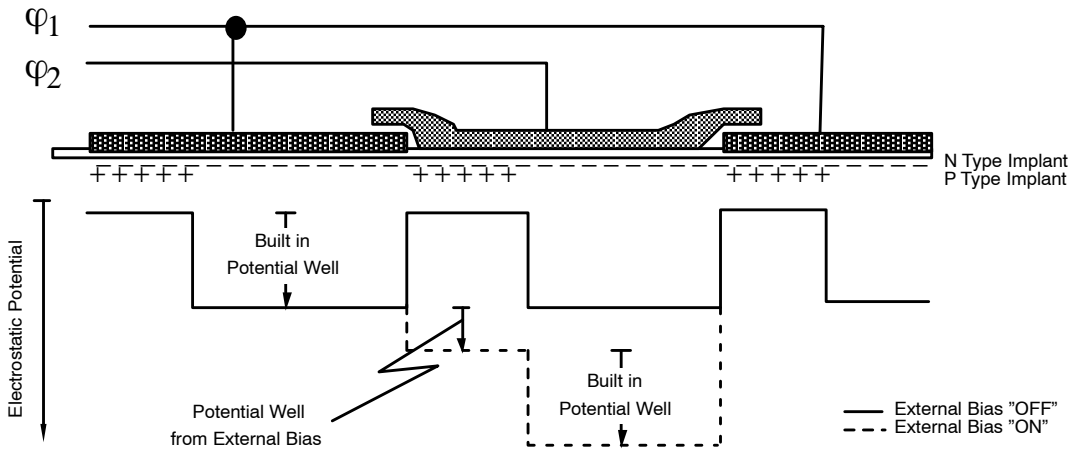

Figure 36. Potential Wells in True Two−Phase CC D

Progressive Scan

An area array image sensor which transfers out the entire image during one exposure cycle is called a Progressive Scan Imager, or non−interlaced image sensor. Similarly, a CRT display which displays the entire image during one frame is called a progressive or non−interlaced display. The other common type of readout encountered is called interlaced, which involves reading out a portion of the imager during one exposure cycle and the remainder in the next cycle. Interlaced displays are used in standard NTSC television, where the image on the screen is created by displaying two fields of the image (i.e. the odd and even fields).

Pseudo Two Phase CCD

A pseudo two phase CCD is similar to a true two phase CCD in that only two external clocks are required to operate the CCD. The difference is that the true two phase CCD requires only two polysilicon electrodes per CCD stage; whereas, the pseudo two phase CCD requires four electrodes, as shown in Figure 37. Generally the true two phase CCD architecture requires less area to implement.

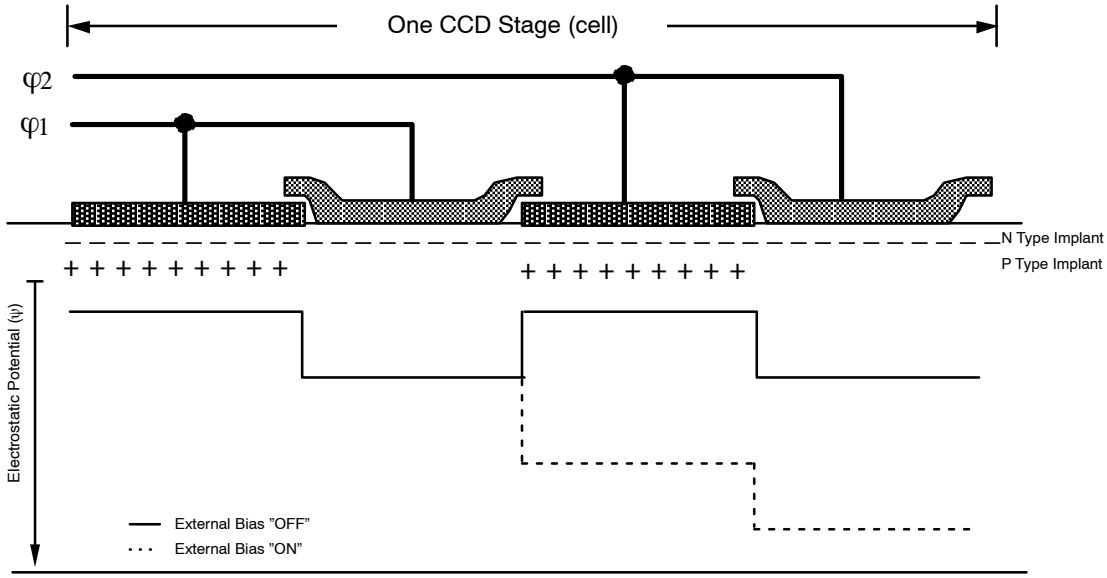

Figure 37. Pseudo Two Phase CC D

Quantum Efficiency

The ratio of the number of photogenerated electrons captured by a pixel to the number of photons incident upon the pixel during a period of time is termed the Quantum Efficiency (QE). Ideal photodiode quantum efficiency can be expressed as:

$$QE = \left(1 - \frac{e^{-\alpha(\lambda)\times L_d}}{1 + \alpha(\lambda) \times L_n}\right) \times \sqrt{\frac{\epsilon_{si}}{\epsilon_0}} \times \left(\frac{|E_{si}^{+}|^2}{|E_{in}^{+}|^2}\right) \quad \text{(eq. 8)}$$

Where ε is the permittivity, (λ) is the absorption coefficient, L_n is the depth from the silicon surface to the end of the photodiode space−charge region, L_d is the electron

diffusion length, and E^+ is the complex electric field strength. Quantum efficiency will vary as a function of optical wavelength due to the wavelength dependence of the absorption coefficient. In addition, interference effects caused by the thin films of silicon dioxide, silicon nitride and polysilicon on the surface will result in a wavelength dependence, which is described by the ratio of complex electric field amplitudes in the above equation.

Reset Clock

The reset clock is the signal used to clear all charge off of the charge sensing node (floating diffusion). The reset clock is generally applied to the gate of a FET, acting as a switch (Q1 in Figure 38). The drain of the FET is connected to a DC source of approximately 11 volts. When the reset FET is turned “ON”, or allowed to conduct, the charge on the sensing node is swept off to the drain and the node is reset to the drain voltage. The reset clock is turned “OFF” to allow the charge sensing node to stabilize and then the next charge packet is dumped onto the charge sensing node.

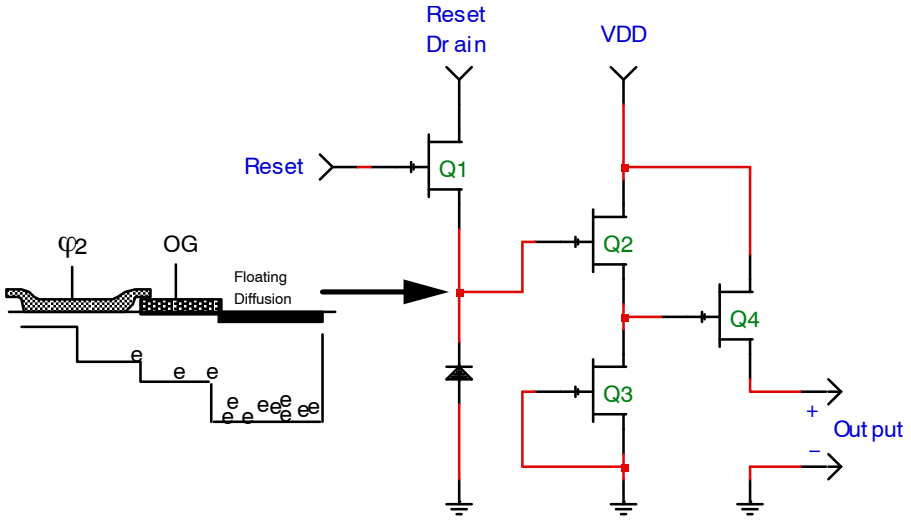

Figure 38. Typical Imager Output Amplifier

Resolution

The resolution of solid state image sensor is the spatial resolving power of that sensor. The spatial resolution of a sensor is described in the spatial frequency domain by plotting the modulation transfer function (MTF) versus spatial frequency. The discrete sampling nature of solid state image sensors gives rise to a sampling frequency which will determine the upper limit of the sensor’s frequency response.

Resolution is frequently described in terms of the number of dots or photosites per inch (DPI) in the imager or object planes. For example, a linear image sensor with a single array of 1000 photosites of pitch 10 μm would have a resolution of 2540 DPI (1000 / (1000 x 0.01 mm x 1”/25.4 mm)). If the sensor is used in an optical system to image an 8” wide document, then the resolution in the document plane would be 125 DPI (1000 pixels / 8”). This example is slightly misleading in that it does not consider the frequency response of the sensor or the optics. In reality, the sensor will have an MTF of between 0.2 and 0.7 at the Nyquist spatial frequency and the optics are likely to have an MTF of 0.6 to 0.9 at the Nyquist frequency. It is important to note that even though a sensor may have a high enough sampling frequency for a particular application, the overall frequency response of the sensor and optics may not be sufficient for the application!

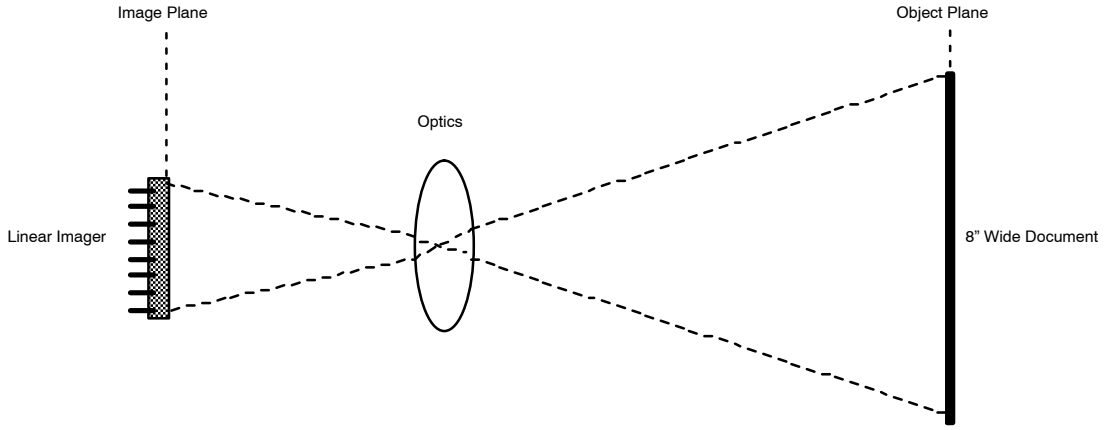

Figure 39. Linear Imager in a Simple Imager System

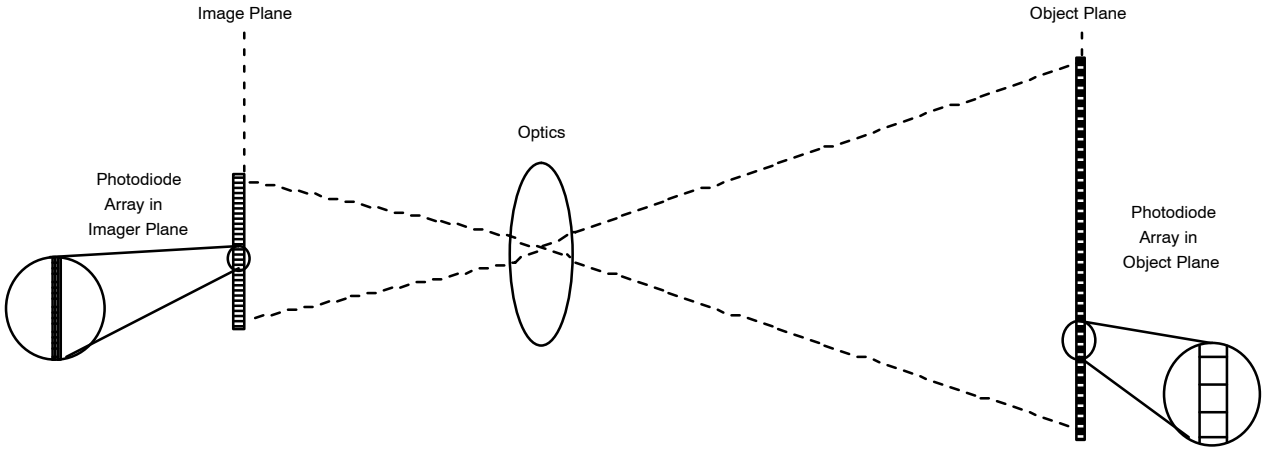

Figure 40. Object/Image Spatial Resolution Comparison

Responsivity

The imager output voltage per incident optical energy density is called the imager responsivity, and it is expressed in volts per micro−joule per centimeter squared, or $V/(\mu J/cm^2)$. Responsivity can be calculated from the photodiode quantum efficiency (QE), charge−to−voltage conversion factor (dV/dN), the energy per photon (E), and the pixel active area (A) as:

$$R(\lambda) = \frac{A \times \frac{dV}{dN} \times QE(\lambda)}{E(\lambda)} = A \times \frac{dV}{dN} \times QE(\lambda) \times \frac{\lambda}{hc} \quad \text{(eq. 9)}$$

As both the quantum efficiency and the photon energy are functions of the optical wavelength (λ), responsivity will be dependent on the wavelength. A curve of responsivity versus wavelength is required to calculate the imager output response to a given optical input. If the spectral irradiance (I(λ)) is known at the imager plane, then the imager output voltage can found from:

$$V_{out} = T_{int} \times \int_{\lambda_{min}}^{\lambda_{max}} R(\lambda) \times I(\lambda) d\lambda \quad \text{(eq. 10)}$$

where T_{int} is the integration time in seconds, and I(λ) is in unit of $W/(m^2-nm)$. The spectral irradiance can be measured using a commercial spectral radiometer, or it can be calculated from the optical system components.

NOTE: See reference 3.1 in the bibliography section for conversion methods from photometric to radiation units and vice−versa.

Saturation

See “Charge Capacity”.

Schottky Barrier Diodes

Schottky barrier diodes are used in platinum silicide infrared image sensors as the photosites. Infrared radiation with photon energy less than the bandgap of silicon is transmitted through the substrate and is absorbed by the PtSi layer. The absorbed photons excite valence electrons in the metal silicide to states above the fermi level, leaving behind holes. Holes which have sufficiency energy to pass over the Schottky barrier formed between the silicide and the silicon are called hot holes and are injected into the substrate.

Sensitivity

The sensitivity of an imager is determined by a combination of the pixel quantum efficiency and the charge−to−voltage conversion factor of the output amplifier and is specified as the imager responsivity.

Smear

Figure 41 depicts the situation where photogenerated charge originating below the space−charge region of a photosite diffuses into the adjacent CCD. This diffusion constitutes a photosite−to−CCD crosstalk signal, which is frequently referred to as smear. The result of smear is to add signal to each charge packet being transported by the CCD, which reduces the dynamic range of the image sensor. Smear is more likely to occur at longer optical wavelengths, since the mean absorption depth within silicon increases for longer wavelengths. Smear can be minimized by (1) increasing the photosite−to−CCD distance, (2) increasing the depth of the photosite space−charge region, or by (3) collecting the smear charge in first transfer gate (i.e. leave TG1 "ON" while integrating image signal). Smear from photogenerated electrons from outside the image sensor active area can also be minimized by the introduction of a scavenger diode around the photo−sensitive array.

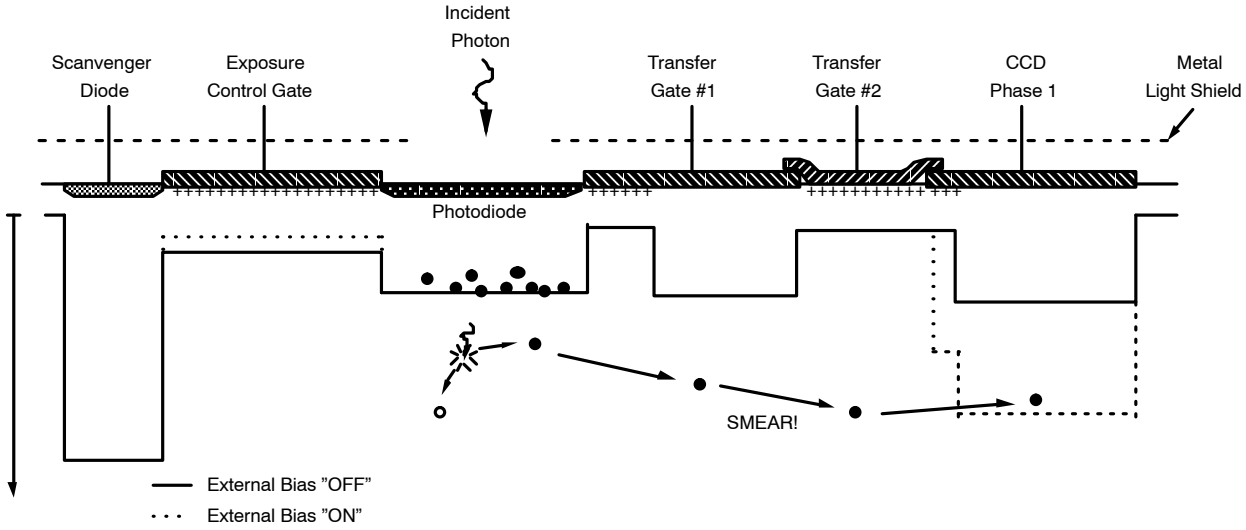

Figure 41. Photodiode−to−CCD Crosstalk (Smear)

Spectral Response

See the "Quantum Efficiency" and/or "Responsivity" for details.

Surface Channel

See "Buried Channel CCD".

Three Phase CCD

A three phase CCD is one which uses three polysilicon electrodes per CCD stage. This type of CCD will require three input clocks to properly transport charge packets.

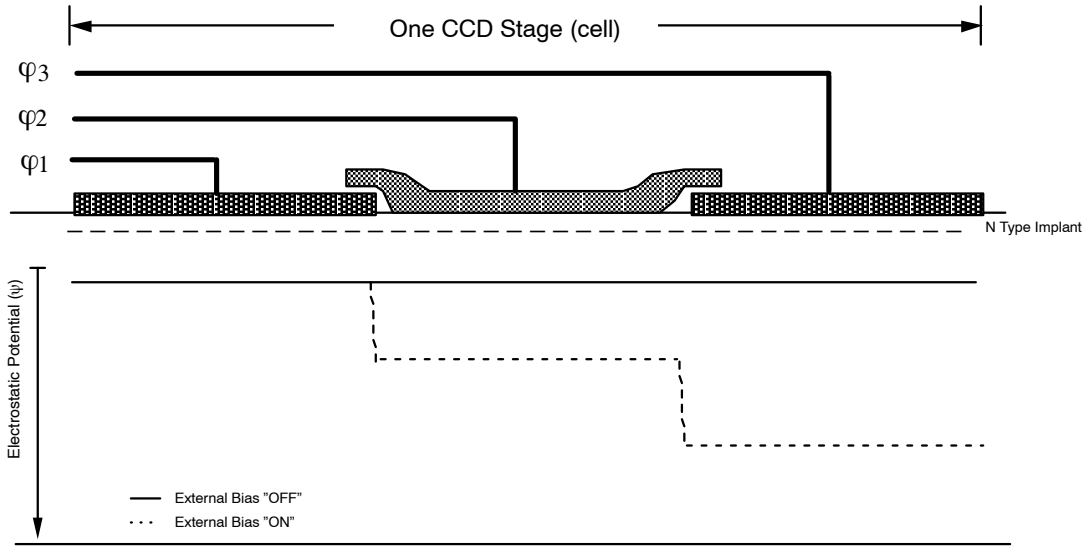

Figure 42. Three Phase CCD

Transfer Gate Clock

The transfer gate clocks are used to isolate the photogenerated charge collected in the photosite from the adjacent CCD structure. At the appropriate time, the CCD clocking is stopped and the transfer gate biases are applied, causing the photosite charge to transfer to the adjacent CCD cell.

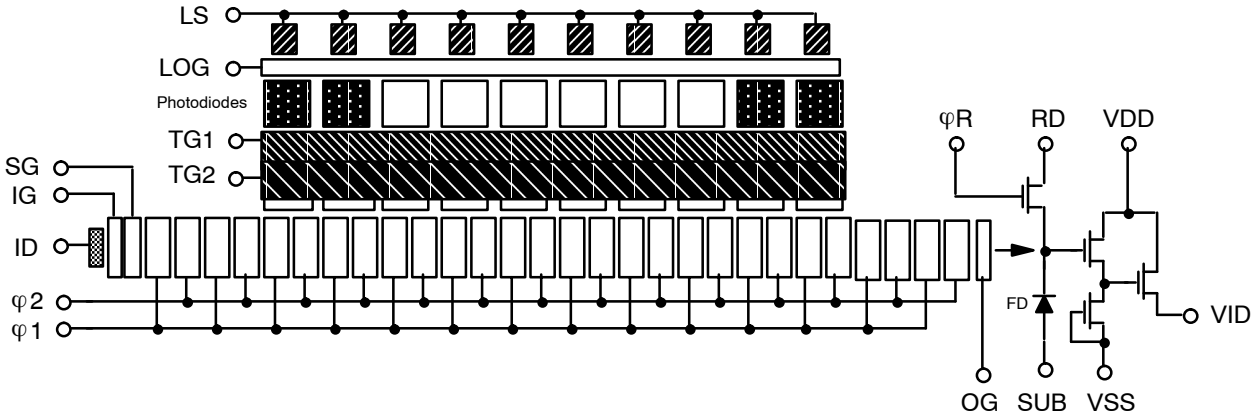

Figure 43. Single Channel of Linear CCD Imager

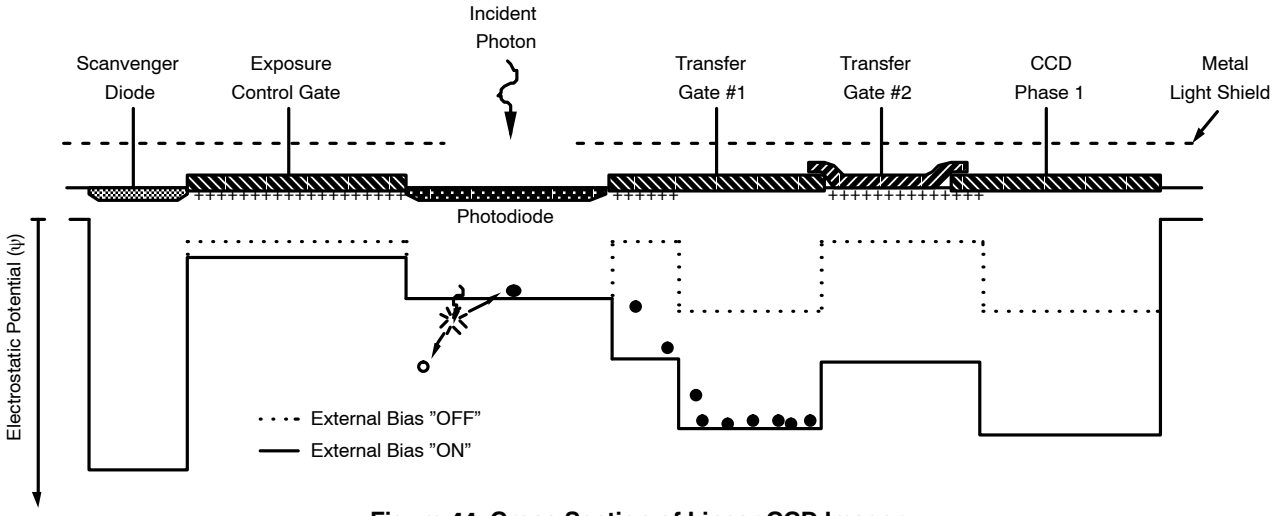

Figure 44. Cross Section of Linear CCD Imager

True Two Phase CCD

A true two phase CCD is one which uses only two polysilicon electrodes per CCD stage. This design permits very dense CCD structures to be developed, which is necessary in very high resolution image sensors.

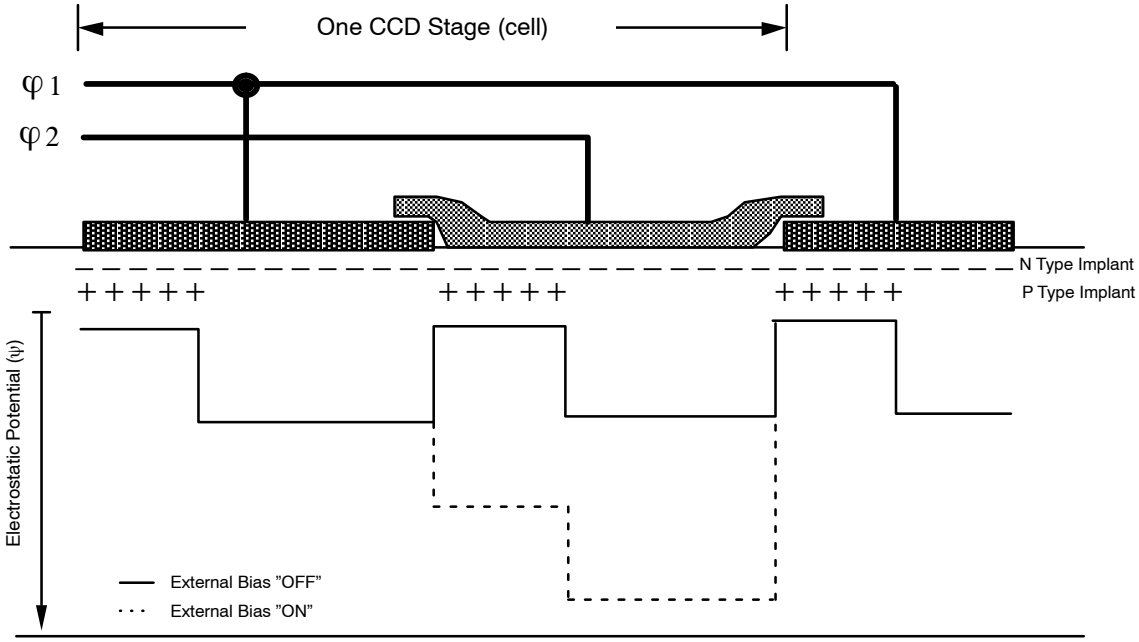

Figure 45. True Two Phase CCD Stage

UV Enhancement Coating

A UV enhancement coating is a material which can be placed on an image sensor which will increase the quantum efficiency in the UV spectrum. UV photons are absorbed in the coating and re−emitted as lower energy, longer wavelength photons which are more readily absorbed by the silicon based photo−sensitive pixels. Lumogen is a common UV enhancement material.

Vertical CCD

Vertical CCDs are used in area imagers to transfer photo−collected charge packets into the horizontal CCD, which then transports the charge packets to the output amplifier.

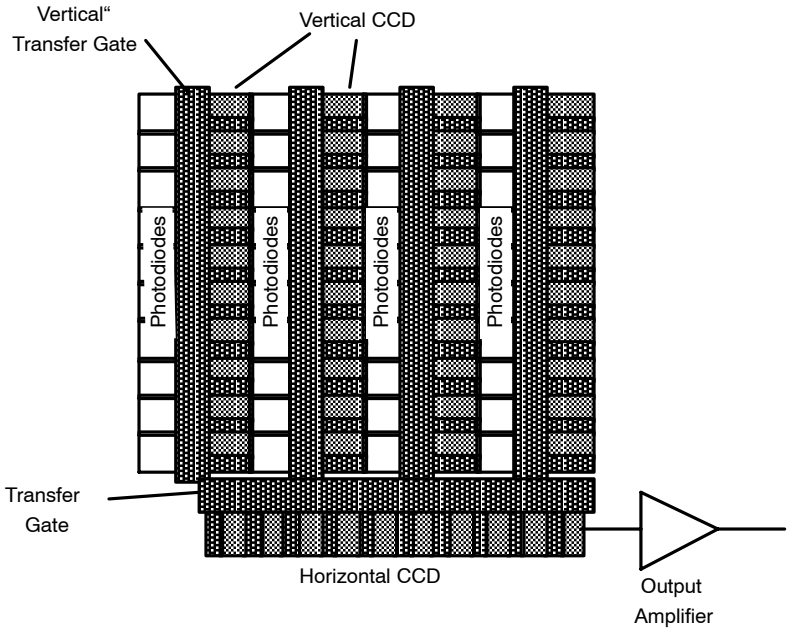

Figure 46. Orientation of CCDs and Transfer Gates on Area Imager

Vertical Overflow Drain (VOD)

See “Lateral Overflow Drain (LOD)”.

Wafer Thinning

A process in which the silicon substrate thickness is significantly reduced to enhance the quantum efficiency (sensitivity) to visible and near infrared radiation. After thinning, the backside of the substrate is passivated. In a typical application, the backside of the thinned substrate imager is positioned in the image focal plane so that the image sensor is illuminated through the thinned substrate from the backside of the device.

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