

14-Bit Binary Counter and Oscillator

MC14060B

The MC14060B is a 14–stage binary ripple counter with an on–chip oscillator buffer. The oscillator configuration allows design of either RC or crystal oscillator circuits. Also included on the chip is a reset function which places all outputs into the zero state and disables the oscillator. A negative transition on Clock will advance the counter to the next state. Schmitt trigger action on the input line permits very slow input rise and fall times. Applications include time delay circuits, counter controls, and frequency dividing circuits.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

Features

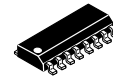
- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from Stages 4 Through 10 and 12 Through 14
- Common Reset Line
- Pin–for–Pin Replacement for CD4060B
- These Devices are Pb–Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

| Symbol | Parameter | Value | Unit |
|-------------------------|---|--------------------------|------|
| V_{DD} | DC Supply Voltage Range | –0.5 to +18.0 | V |
| V_{in} , V_{out} | Input or Output Voltage Range (DC or Transient) | –0.5 to V_{DD} +0.5 | V |
| I_{in} , I_{out} | Input or Output Current (DC or Transient) per Pin | ± 10 | mA |
| P_D | Power Dissipation, per Package (Note 1) | 500 | mW |
| T_A | Ambient Temperature Range | –55 to +125 | °C |
| T_{stg} | Storage Temperature Range | –65 to +150 | °C |
| T_L | Lead Temperature (8 Second Soldering) | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: “D/DW” Packages: –7.0 mW/°C from 65°C To 125°C.

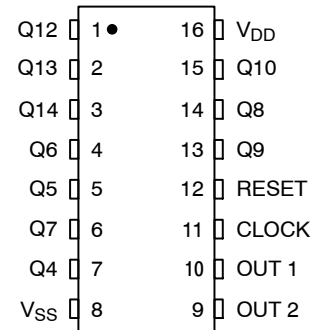


SOIC–16
D SUFFIX
CASE 751B

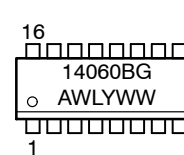


TSSOP–16
DT SUFFIX
CASE 948F

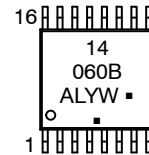
PIN ASSIGNMENT



MARKING DIAGRAMS



SOIC–16



TSSOP–16

- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G or ■ = Pb–Free Package



(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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Table 1. Truth Table

| Clock | Reset | Output State |
|---|-------|-----------------------|
|  | L | No Change |
|  | L | Advance to Next State |
| H | H | All Outputs are Low |

X = Don't Care

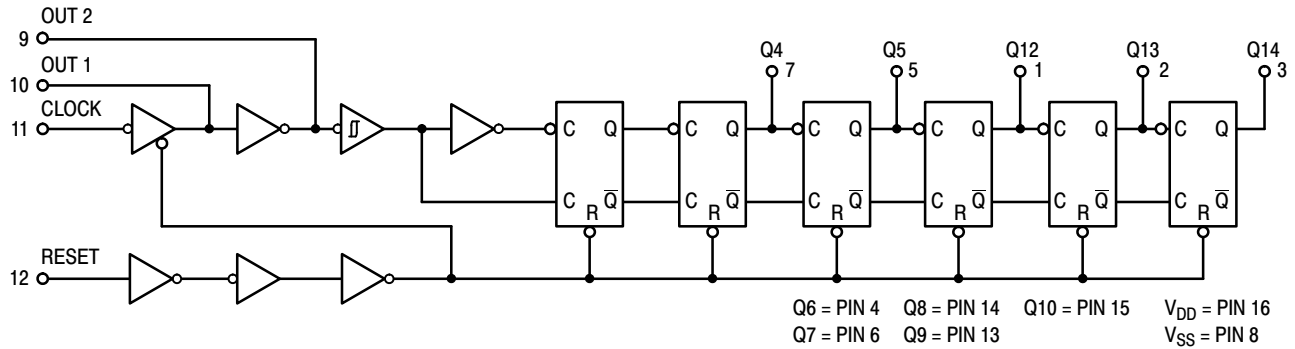


Figure 1. Logic Diagram

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|---------------|-----------------------|-----------------------|
| MC14060BDG | SOIC-16 (Pb-Free) | 48 Units / Rail |
| MC14060BDR2G | SOIC-16 (Pb-Free) | 2500 / Tape & Reel |
| MC14060BDTR2G | TSSOP-16 (Pb-Free) | 2500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Symbol | Characteristic | V_{DD} Vdc | -55°C | | 25°C | | | 125°C | | Unit |
|----------|---|-----------------|---|-----------|-------|-----------------|-----------|-------|-----------|---------|
| | | | Min | Max | Min | Typ (Note 2) | Max | Min | Max | |
| V_{OL} | Output Voltage $V_{in} = V_{DD}$ or 0 "0" Level | 5.0 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | V |
| | | 10 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | |
| | | 15 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | |
| V_{OH} | $V_{in} = 0$ or V_{DD} "1" Level | 5.0 | 4.95 | - | 4.95 | 5.0 | - | 4.95 | - | V |
| | | 10 | 9.95 | - | 9.95 | 10 | - | 9.95 | - | |
| | | 15 | 14.95 | - | 14.95 | 15 | - | 14.95 | - | |
| V_{IL} | Input Voltage ($V_O = 4.5$ or 0.5 V) ($V_O = 9.0$ or 1.0 V) ($V_O = 13.5$ or 1.5 V) "0" Level | 5.0 | - | 1.5 | - | 2.25 | 1.5 | - | 1.5 | V |
| | | 10 | - | 3.0 | - | 4.50 | 3.0 | - | 3.0 | |
| | | 15 | - | 4.0 | - | 6.75 | 4.0 | - | 4.0 | |
| V_{IH} | ($V_O = 0.5$ or 4.5 V) ($V_O = 1.0$ or 9.0 V) ($V_O = 1.5$ or 13.5 V) "1" Level | 5.0 | 3.5 | - | 3.5 | 2.75 | - | 3.5 | - | V |
| | | 10 | 7.0 | - | 7.0 | 5.50 | - | 7.0 | - | |
| | | 15 | 11.0 | - | 11.0 | 8.25 | - | 11.0 | - | |
| V_{IL} | Input Voltage ($V_O = 4.5$ Vdc) ($V_O = 9.0$ Vdc) ($V_O = 13.5$ Vdc) (For Input 11 and Output 10) "0" Level | 5.0 | - | 1.0 | - | 2.25 | 1.0 | - | 1.0 | Vdc |
| | | 10 | - | 2.0 | - | 4.50 | 2.0 | - | 2.0 | |
| | | 15 | - | 2.5 | - | 6.75 | 2.5 | - | 2.5 | |
| V_{IH} | ($V_O = 0.5$ Vdc) ($V_O = 1.0$ Vdc) ($V_O = 1.5$ Vdc) "1" Level | 5.0 | 4.0 | - | 4.0 | 2.75 | - | 4.0 | - | Vdc |
| | | 10 | 8.0 | - | 8.0 | 5.50 | - | 8.0 | - | |
| | | 15 | 12.5 | - | 12.5 | 8.25 | - | 12.5 | - | |
| I_{OH} | Output Drive Current ($V_{OH} = 2.5$ V) ($V_{OH} = 4.6$ V) ($V_{OH} = 9.5$ V) ($V_{OH} = 13.5$ V) (Except Source Pins 9 and 10) | 5.0 | -3.0 | - | -2.4 | -4.2 | - | -1.7 | - | mA |
| | | 5.0 | -0.64 | - | -0.51 | -0.88 | - | -0.36 | - | |
| | | 10 | -1.6 | - | -1.3 | -2.25 | - | -0.9 | - | |
| | | 15 | -4.2 | - | -3.4 | -8.8 | - | -2.4 | - | |
| I_{OL} | ($V_{OL} = 0.4$ V) ($V_{OL} = 0.5$ V) ($V_{OL} = 1.5$ V) Sink | 5.0 | 0.64 | - | 0.51 | 0.88 | - | 0.36 | - | mA |
| | | 10 | 1.6 | - | 1.3 | 2.25 | - | 0.9 | - | |
| | | 15 | 4.2 | - | 3.4 | 8.8 | - | 2.4 | - | |
| I_{in} | Input Current | 15 | - | ± 0.1 | - | ± 0.00001 | ± 0.1 | - | ± 1.0 | μA |
| C_{in} | Input Capacitance ($V_{in} = 0$) | - | - | - | - | 5.0 | 7.5 | - | - | pF |
| I_{DD} | Quiescent Current (Per Package) | 5.0 | - | 5.0 | - | 0.005 | 5.0 | - | 150 | μA |
| | | 10 | - | 10 | - | 0.010 | 10 | - | 300 | |
| | | 15 | - | 20 | - | 0.015 | 20 | - | 600 | |
| I_T | Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs, all buffers switching) | 5.0 10 15 | $I_T = (0.25 \mu A/kHz) f + I_{DD}$ $I_T = (0.54 \mu A/kHz) f + I_{DD}$ $I_T = (0.85 \mu A/kHz) f + I_{DD}$ | | | | | | | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.002$.

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SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

| Symbol | Characteristic | V _{DD} Vdc | Min | Typ (Note 5) | Max | Unit |
|--------------------------------------|---|------------------------|----------|-----------------|-----|------|
| t _{TLH} | Output Rise Time (Counter Outputs) | 5.0 | - | 40 | 200 | ns |
| | | 10 | - | 25 | 100 | |
| | | 15 | - | 20 | 80 | |
| t _{THL} | Output Fall Time (Counter Outputs) | 5.0 | - | 50 | 200 | ns |
| | | 10 | - | 30 | 100 | |
| | | 15 | - | 20 | 80 | |
| t _{PLH} t _{PHL} | Propagation Delay Time Clock to Q4 Clock to Q14 | 5.0 | - | 415 | 740 | ns |
| | | 10 | - | 175 | 300 | |
| | | 15 | - | 125 | 200 | |
| | | 5.0 | - | 1.5 | 2.7 | μs |
| | | 10 | - | 0.7 | 1.3 | |
| | | 15 | - | 0.4 | 1.0 | |
| t _{WH} | Clock Pulse Width | 5.0 | 100 | 65 | - | ns |
| | | 10 | 40 | 30 | - | |
| | | 15 | 30 | 20 | - | |
| f _φ | Clock Pulse Frequency | 5.0 | - | 5 | 3.5 | MHz |
| | | 10 | - | 14 | 8 | |
| | | 15 | - | 17 | 12 | |
| t _{TLH} t _{THL} | Clock Rise and Fall Time | 5.0 | No Limit | | | ns |
| | | 10 | | | | |
| | | 15 | | | | |
| t _w | Reset Pulse Width | 5.0 | 120 | 40 | - | ns |
| | | 10 | 60 | 15 | - | |
| | | 15 | 40 | 10 | - | |
| t _{PHL} | Propagation Delay Time Reset to On | 5.0 | - | 170 | 350 | ns |
| | | 10 | - | 80 | 160 | |
| | | 15 | - | 60 | 100 | |

5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

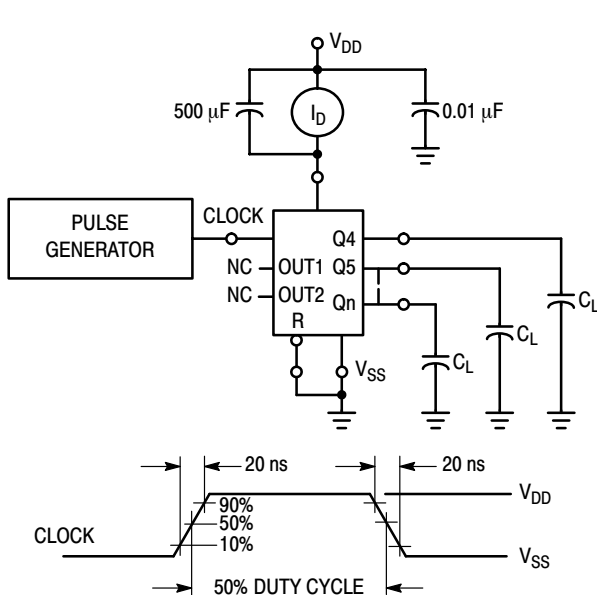


Figure 1. Power Dissipation Test Circuit and Waveform

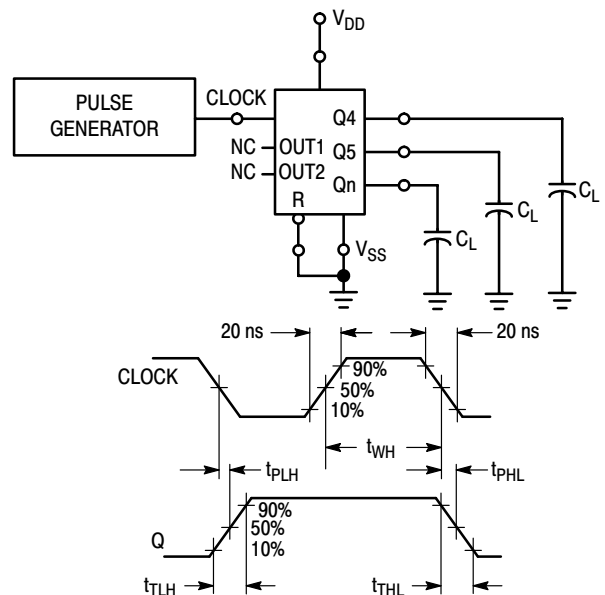
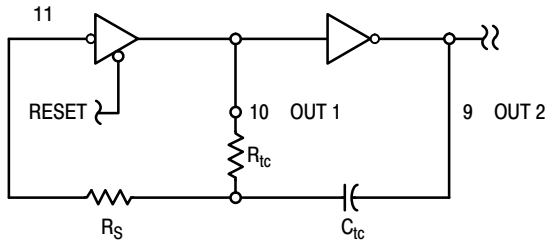


Figure 2. Switching Time Test Circuit and Waveforms

MC14060B



$$f \approx \frac{1}{2.3 R_{TC} C_{TC}}$$

if $1 \text{ kHz} \leq f \leq 100 \text{ kHz}$
and $2R_{TC} < R_S < 10R_{TC}$
(f in Hz, R in ohms, C in farads)

The formula may vary for other frequencies. Recommended maximum value for the resistors in $1 \text{ M}\Omega$.

Figure 3. Oscillator Circuit Using RC Configuration

TYPICAL RC OSCILLATOR CHARACTERISTICS

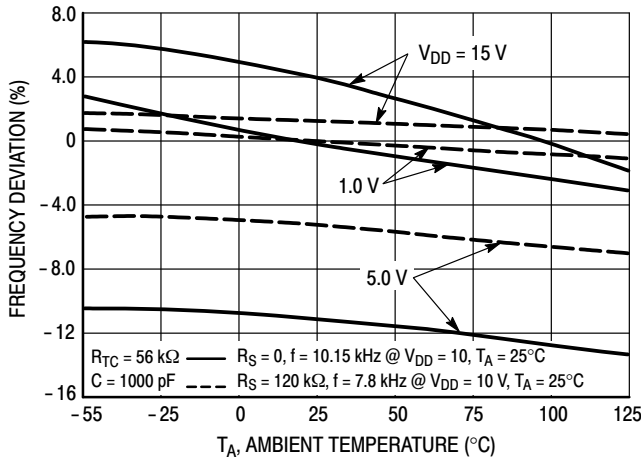


Figure 4. RC Oscillator Stability

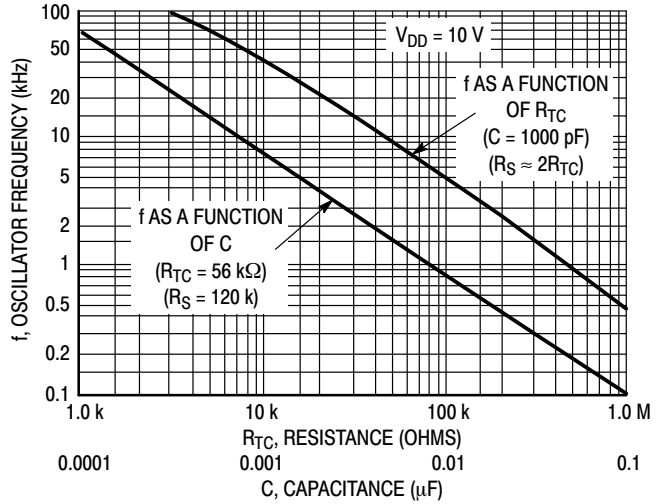


Figure 5. RC Oscillator Frequency as a Function of R_{TC} and C

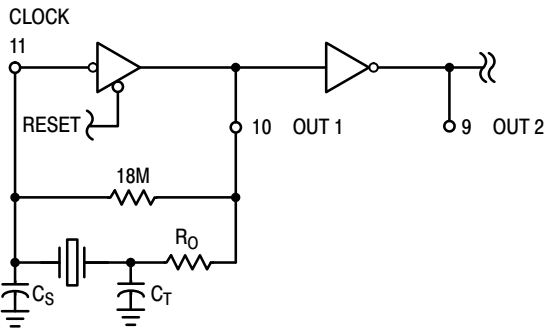


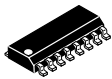
Figure 6. Typical Crystal Oscillator Circuit

Table 2. Typical Data for Crystal Oscillator Circuit

| Characteristic | 500 kHz Circuit | 32 kHz Circuit | Unit |
|--|-----------------|----------------|------------|
| Crystal Characteristics | | | |
| Resonant Frequency | 500 | 32 | kHz |
| Equivalent Resistance, R_S | 1.0 | 6.2 | k Ω |
| External Resistor/Capacitor Values | | | |
| R_0 | 47 | 750 | k Ω |
| C_T | 82 | 82 | pF |
| C_S | 20 | 20 | pF |
| Frequency Stability | | | |
| Frequency Changes as a Function of V_{DD} ($T_A = 25^\circ\text{C}$) | | | |
| V_{DD} Change from 5.0 V to 10 V | +6.0 | +2.0 | ppm |
| V_{DD} Change from 10 V to 15 V | +2.0 | +2.0 | ppm |
| Frequency Change as a Function of Temperature ($V_{DD} = 10 \text{ V}$) | | | |
| T_A Change from -55°C to $+25^\circ\text{C}$ Complete Oscillator (Note 6) | +100 | +120 | ppm |
| T_A Change from $+25^\circ\text{C}$ to $+125^\circ\text{C}$ Complete Oscillator (Note 6) | -160 | -560 | ppm |

6. Complete oscillator includes crystal, capacitors, and resistors.

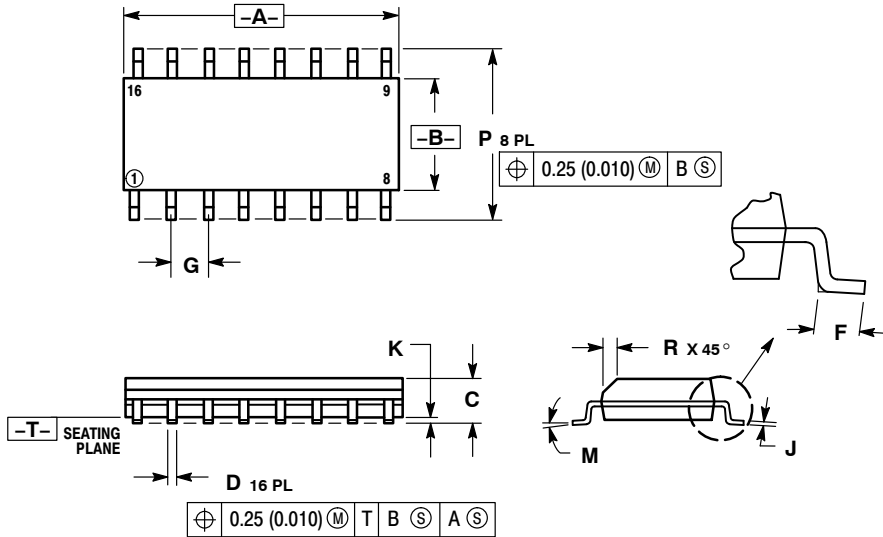
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-16
CASE 751B-05
ISSUE K

DATE 29 DEC 2006



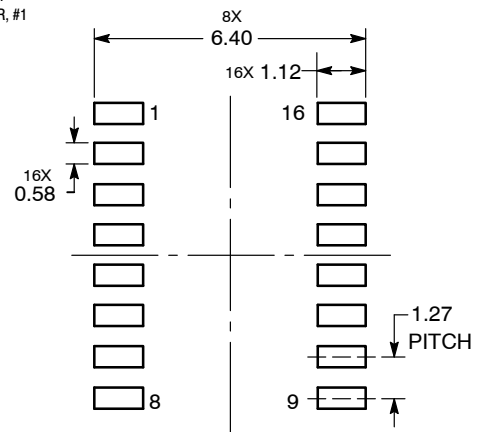
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° 7° | | 0° 7° | |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

- | | | | |
|--|--|--|--|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p> | <p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p> | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p> | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p> | |

RECOMMENDED
SOLDERING FOOTPRINT*

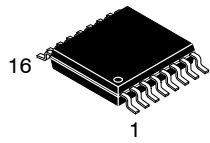


*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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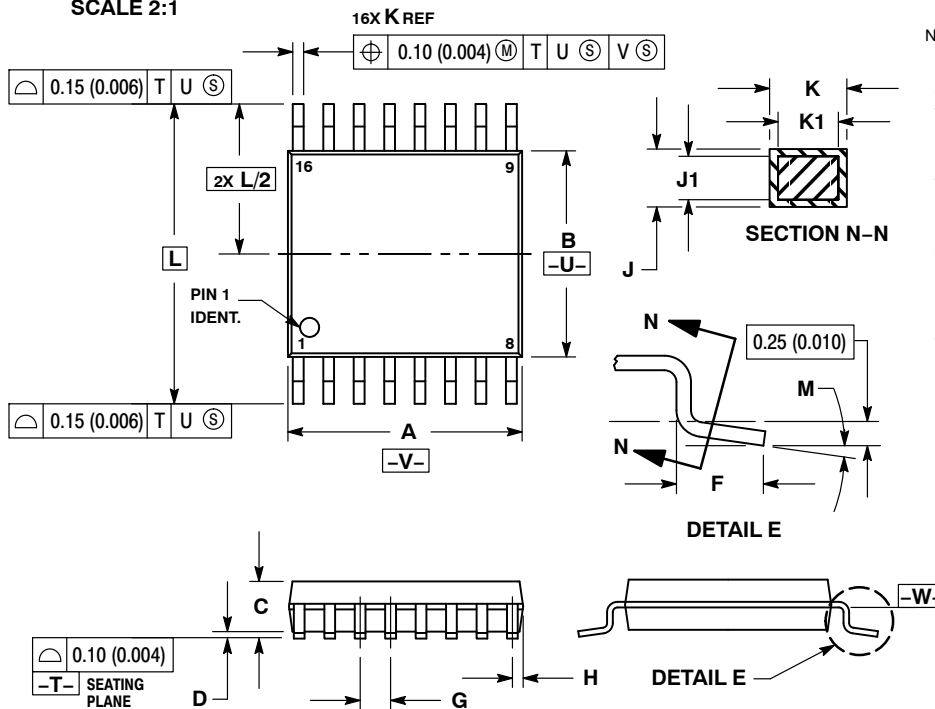
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSSOP-16 WB
CASE 948F
ISSUE B

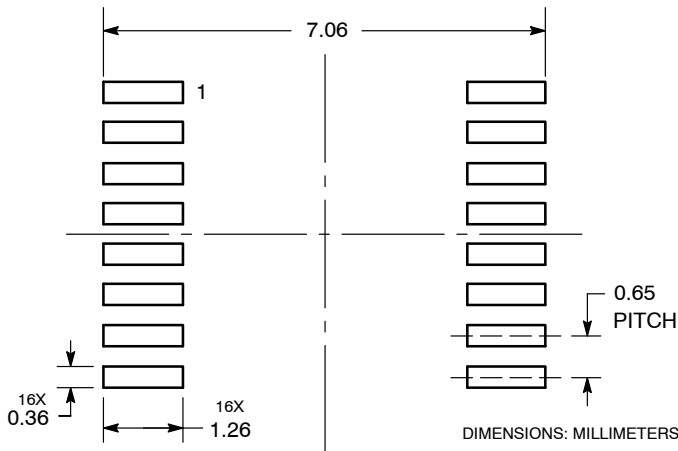
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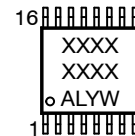
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

RECOMMENDED SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|-------------------------|--------------------|--|
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