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Automotive Smart Power Module, The 1200 V ASPM34 Series, Application Note

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APPLICATION NOTE

INTRODUCE

The 1200 V ASPM34 series extends the existing Intelligent Power Module product portfolio, qualifying them to meet the performance and reliability requirements of automotive auxiliary motor drives in Hybrid and Electric Vehicle application. This application note supports the 1200 V ASPM34 series. It should be used in conjunction with the 1200 V ASPM34 datasheets and application note AN−9076 *(Mounting Guidance)*.

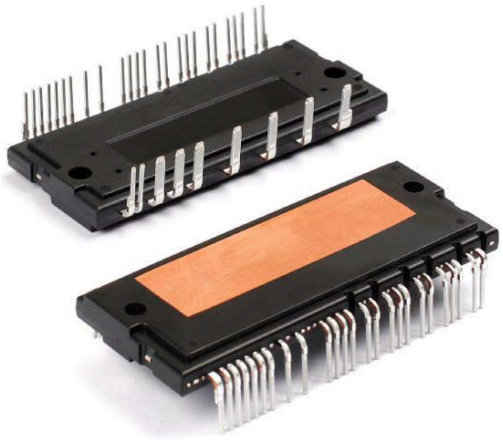


Figure 1.

Design Concept

The 1200 V ASPM34 design objective is to provide a minimized package and a low power consumption module with improved reliability. This is achieved by applying new gate−driving High−Voltage Integrated Circuit (HVIC), a new Insulated−Gate Bipolar Transistor (IGBT) of advanced silicon technology, and improved Direct Bonded Copper (DBC) substrate base transfer mold package. The 1200 V ASPM34 achieves reduced board size and improved reliability compared to existing discrete solutions. Target applications are inverter motor drives for Auto−motive use, such as E−compressor, Oil pump, Fuel pump, Water pump, cooling fans and other auxiliary motors in Hybrid and Electric Vehicles.

A design advantage integrates an NTC thermistor for temperature measuring of power chips (e.g. IGBTs, Fast−Recovery Diode (FRDs) on the same substrate. Most customers want to know the exact temperature of power chips because temperature affects the quality, reliability, and longevity of products. This desire is thwarted because integrated power chips (e.g. IGBTs, FRD) inside modules operate in high−voltage conditions. Therefore, instead of directly sensing the temperature of power chips, customers have been using an external NTC thermistor for sensing the temperature of the module or heat−sink. This method doesn't accurately reflect the temperature of power components due to cost, but is simple. The NTC thermistor of the 1200 V ASPM34 is integrated with the power chips on the same ceramic substrate and therefore more accurately reflects the temperature of power chips.

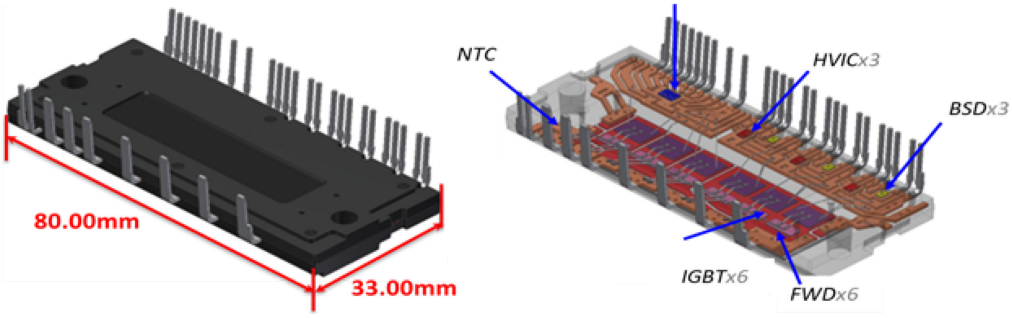


Figure 2. External View and Internal Structure of the 1200 V ASPM34

Key Features

- Automotive Qualified (AEC−Q100, Q101 and AQG324)
- 1200 V ASPM34, 3−Phase IGBT inverter with Integral gate drivers and protection
- Low−Loss, Short−Circuit Rated IGBTs
- Very Low Thermal Resistance by Adopting DBC Substrate
- Built−In Bootstrap Diode and Dedicated Vs Pins Simplify PCB Layout
- Separate Open−Emitter pins from Low−Side IGBTs for Three−Phase current sensing
- Single−Grounded Power Supply Supported
- Built−in NTC Thermistor for Temperature Monitoring and Management
- Adjustable Over−Current Protection via Integrated Sense−IGBTs
- Isolation Rating of 2500 V_{RMS} / 1 min
- Pb−Free and RoHS compliant

PRODUCT DESCRIPTION

Ordering Information

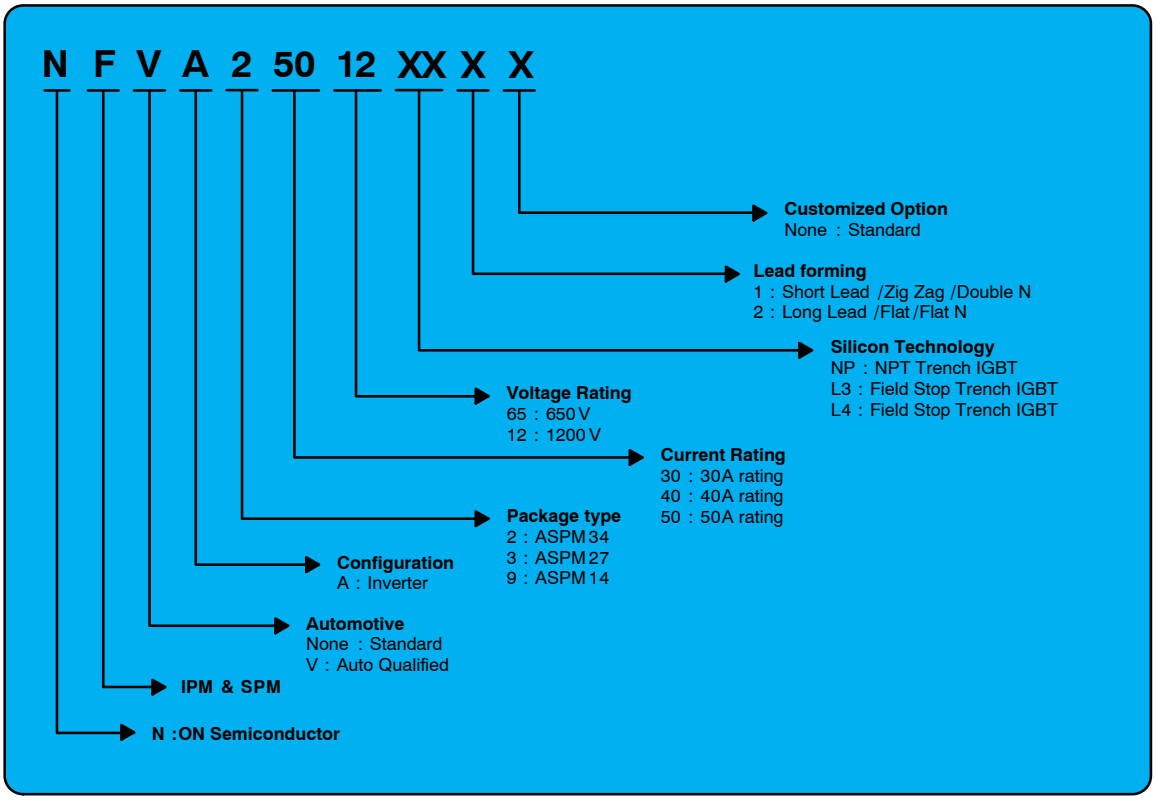


Figure 3. Ordering Information

Product Line−up

Table 1 shows the basic line up without package variations. Online loss and temperature simulation tool, Motion Control Design Tool is recommended to find out the right the 1200 V ASPM34 product for the desired application.

Table 1. PRODUCT LINE−UP

Target Application	Device	IGBT Rating	Motor Rating (Note 1)	Isolation Voltage
E−compressor, Oil pump, Fuel pump, Water pump, Cooling Fans	NFVA22512NP2T	25 A / 1200 V	3.7 kW / 440 V_{AC}	V_{ISO} = 2500 V_{RMS} (Sine 60 Hz, 1−min All Shorted Pins Heat Sink)
	NFVA23512NP2T	35 A / 1200 V	5.5 kW / 440 V_{AC}	
	NFVA25012NP2T	50 A / 1200 V	7.5 Kw / 440 V_{AC}	

1. These motor ratings are simulation results under following conditions: V_{AC} = 440 V, V_{DD} = 15 V, T_C = 100°C, T_j = 150°C, f_{PWM} = 5 kHz, PF = 0.8, MI = 0.9, Motor efficiency = 0.75, overload 150% for 1min.
These motor ratings are general ratings, so may be changed by conditions.

PACKAGE

Internal Circuit Diagram

There is the internal circuit diagram of the 1200 V ASPM34 as shown in Figure 4.

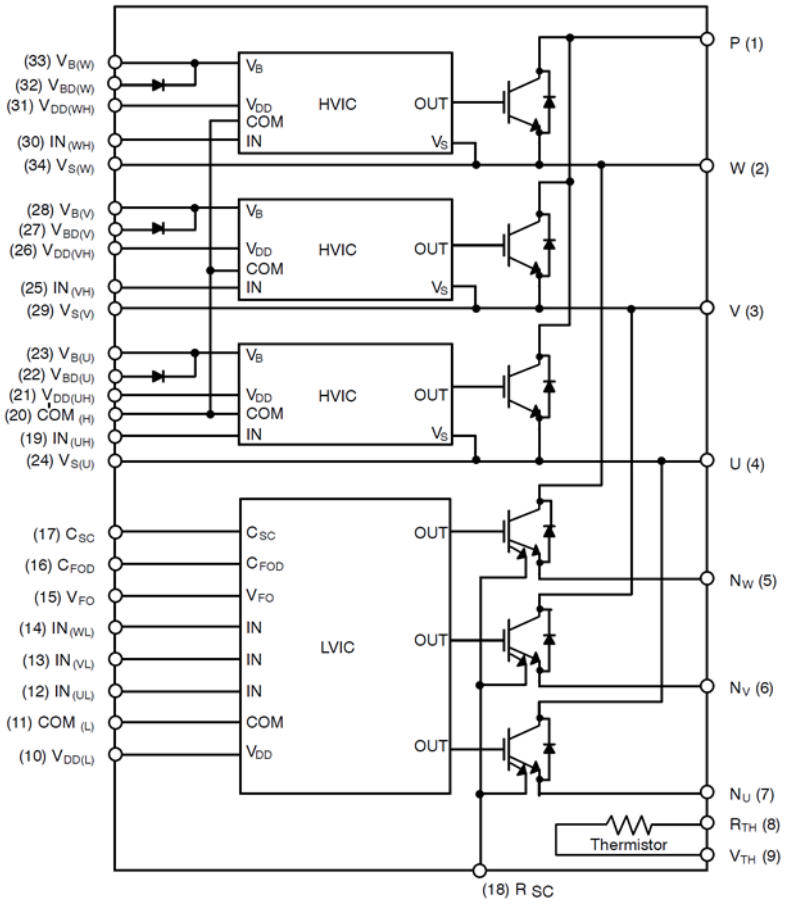


Figure 4. The 1200 V ASPM34 Version Internal Circuit

Pin Description

Figure 5 shows the location of pins and the names of the 1200 V ASPM34 series.

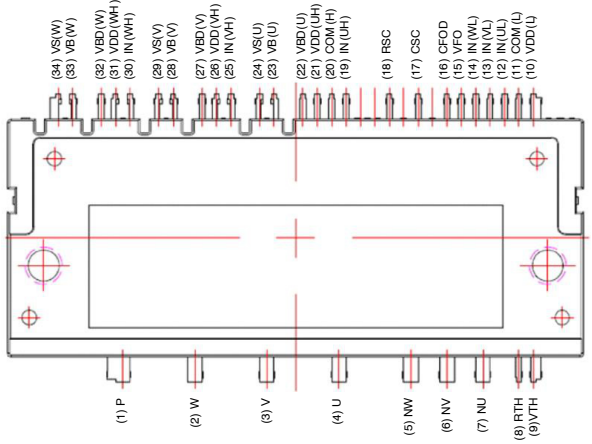


Figure 5. Package Top−View and Pin Assignment

In the later section illustrates the internal structure of the module in more detail. The detail functional descriptions are provided in Table 2.

Table 2. PIN DESCRIPTION

Pin No.	Name	Description
1	P	Positive DC Link Input
2	W	Output for W Phase
3	V	Output for V Phase
4	U	Output for U Phase
5	N_W	Negative DC Link Input for W Phase
6	N_V	Negative DC Link Input for V Phase
7	N_U	Negative DC Link Input for U Phase
8	R_{TH}	Series Resistor for Thermistor (Temperature Detection)
9	V_{TH}	Thermistor Bias Voltage
10	$V_{DD(L)}$	Low−Side Bias Voltage for IC and IGBT Driving
11	$COM_{(L)}$	Low−Side Common Supply Ground
12	$IN_{(UL)}$	Signal Input for Low−Side U Phase
13	$IN_{(VL)}$	Signal Input for Low−Side V Phase
14	$IN_{(WL)}$	Signal Input for Low−Side W Phase
15	V_{FO}	Fault Output
16	C_{FOD}	Capacitor for Fault Output Duration Selection
17	C_{SC}	Capacitor (Low−Pass Filter) for Short−Circuit Current Detection Input
18	R_{SC}	Resistor for Short−Circuit Current Detection
19	$IN_{(UH)}$	High−Side Common Supply Ground
20	$COM_{(H)}$	No Connection
21	$V_{DD(UH)}$	High−Side Bias Voltage for U Phase IGBT Driving
22	$V_{BD(U)}$	Anode of Bootstrap Diode for High−Side U Phase
23	$V_{B(U)}$	High−Side Bias Voltage for U Phase IGBT Driving
24	$VS_{(U)}$	High−Side Bias Voltage Ground for U Phase IGBT Driving
25	$IN_{(VH)}$	Signal Input for High−Side V Phase
26	$V_{DD(VH)}$	High−Side Bias Voltage for V Phase IC
27	$V_{BD(V)}$	Anode of Bootstrap Diode for High−Side V Phase
28	$V_{B(V)}$	High−Side Bias Voltage for V Phase IGBT Driving
29	$V_{S(V)}$	High−Side Bias Voltage Ground for V Phase IGBT Driving
30	$IN_{(WH)}$	Signal Input for High−Side W Phase
31	$V_{DD(WH)}$	High−Side Bias Voltage for W Phase IC
32	$V_{BD(W)}$	Anode of Bootstrap Diode for High−Side W Phase
33	$V_{B(W)}$	High−Side Bias Voltage for W Phase IGBT Driving
34	$V_{S(W)}$	High−Side Bias Voltage Ground for W Phase IGBT Driving

Detailed Pin Definition and Notification

Pins: $V_{B(U)}$−$V_{S(U)}$, $V_{B(V)}$−$VS_{(V)}$, $V_{B(W)}$−$V_{S(W)}$

- High−side bias voltage pins for driving the IGBT / high−side bias voltage ground pins for driving the IGBTs.
- These are drive power supply pins for providing gate drive power to the high−side IGBTs.
- By virtue of the ability of bootstrap, the circuit scheme is that no external power supplies are required for the high−side IGBTs.
- Each bootstrap capacitor is charged from the V_{DD} supply during ON state of the corresponding low−side IGBT.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a low−ESR, low−ESL filter capacitor should be mounted very close to these pins.

Pins: $V_{DD(L)}$, $V_{DD(WH)}$, $V_{DD(VH)}$, $V_{DD(UH)}$

- Low−Side Bias Voltage Pin / High−Side Bas Voltage.
- These are control supply pins for the built−in ICs.
- These four pins should be connected externally.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a low−ESR, low−ESL filter capacitor should be mounted very close to these pins.

Pins: $COM_{(L)}$, $COM_{(H)}$

- Low−Side Common Supply Ground pins.
- These are supply ground pins for the built−in ICs.
- These two pins should be connected externally.
- *Important!* To avoid noise influences, the main power circuit current should not be allowed to flow through this pin.

Pins: $V_{BD(UH)}$, $V_{BD(VH)}$, $V_{BD(WH)}$

- Anode Pins of Bootstrap Diode pins.
- These are pins to connect internal bootstrap diode for each high−side bootstrapping.
- External resistor should be connected between these pins and each V_{DD}(xH).

Pins: $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$

- Signal Input Pins.
- These pins control the operation of the built−in IGBTs.
- They are activated by voltage input signals. The terminals are internally connected to a Schmitt−trigger circuit composed of 5 V−class CMOS.
- The signal logic of these pins is active HIGH. The IGBT associated with each of these pins is turned ON when a sufficient logic voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the 1200 V ASPM34 against noise influences.
- To prevent signal oscillations, an RC coupling as illustrated in Figure 45 is recommended.

Pin: RSC

- Resistor Connection Pin for Short−Circuit Current Detection.
- Low−side sense IGBT current flows through this pin. Short−circuit and over−current can be detected at this pin through an external resistor. (Refer to Figure 45)
- If using three shunt resistors at N terminals for OCP and SCP without sense detecting from RSC, RSC should be connected to COM.

Pin: C_{SC}

- Short−Circuit and Over−Current Detection Input Pin.
- The current sense current detecting resistor (R_{SC}) should be connected between C_{SC} and COM pins to detect over−current and short−circuit current. (Refer to Figure 45)
- The shunt resistor should be selected to meet the detection levels matched for the specific application. The RC filter should be connected to the C_{SC} pin to eliminate noise.
- The connection length between the shunt resistor and C_{SC} pin should be minimized.

Pin: V_{FO}

- Fault output pin.
- This is the fault output alarm pin. An active LOW output is given on this pin for a fault state condition in the ASPM34.
- The alarm conditions are: Short−Circuit Current Protection (SCP), and low−side bias Under−Voltage Lockout (UVLO).
- The VFO output is open drain configured. The VFO signal line should be pulled to the 5 V logic power supply with approximately 4.7 kΩ resistance.

Pin: V_{TH}

- Thermistor Bias Voltage.
- This is the bias voltage pin of internal thermistor. This pin should be connected to the 5 V logic power supply.

Pin: R_{TH}

- Thermistor Bias Voltage.
- For case temperature (T_C) detection, this pin should be connected to an external series resistor.
- The external series resistor should be selected to meet the detection range matched for the specification of each application. (For details, Refer to Table 22)

Pin: P

- Positive DC−link pin.
- This is the DC−link positive power supply pin of the inverter.
- It is internally connected to the collectors of the high−side IGBTs.

- To suppress surge voltage caused by the DC−link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin (Tip: metal film capacitor is typically used).

Pins: N_U, N_V, N_W

- Negative DC−link pins.
- These are the DC−link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low−side IGBT emitters of the each phase.
- These pins have to be connected shunt resistor (one or three) for current sensing.

Pins: U, V, W

- Inverter output pins for connecting to the inverter load (e.g. motor).

Package Structure

Since heat dissipation is an important factor limiting the power module's current capability, the heat dissipation characteristics of a package are important in determining the performance. A trade−off exists among heat dissipation characteristics, package size, and isolation characteristics. The key to good package technology lies in the optimization package size while maintaining outstanding heat dissipation characteristics without compromising the isolation rating.

In 1200 V ASPM34, technology was developed with DBC substrate that resulted in good heat dissipation characteristics. Power chips are attached directly to the DBC substrate. This technology is applied 1200 V ASPM34 achieving improved reliability and heat dissipation.

Figure 6 and Figure 7 show the package outline and the cross−sections of the 1200 V ASPM34 package.

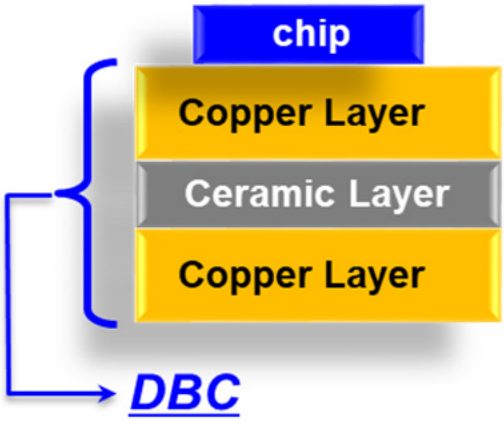


Figure 6. Vertical Structure for Heat Dissipation

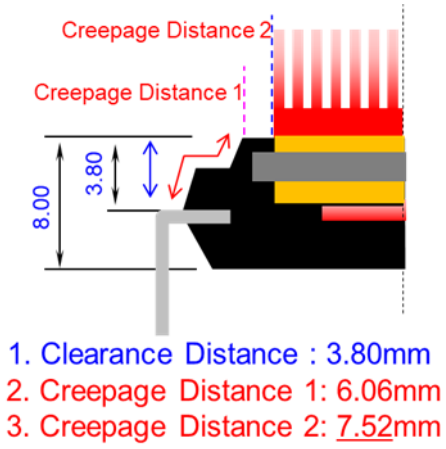


Figure 7. Distance for Isolation

Detailed Package Outline Drawings

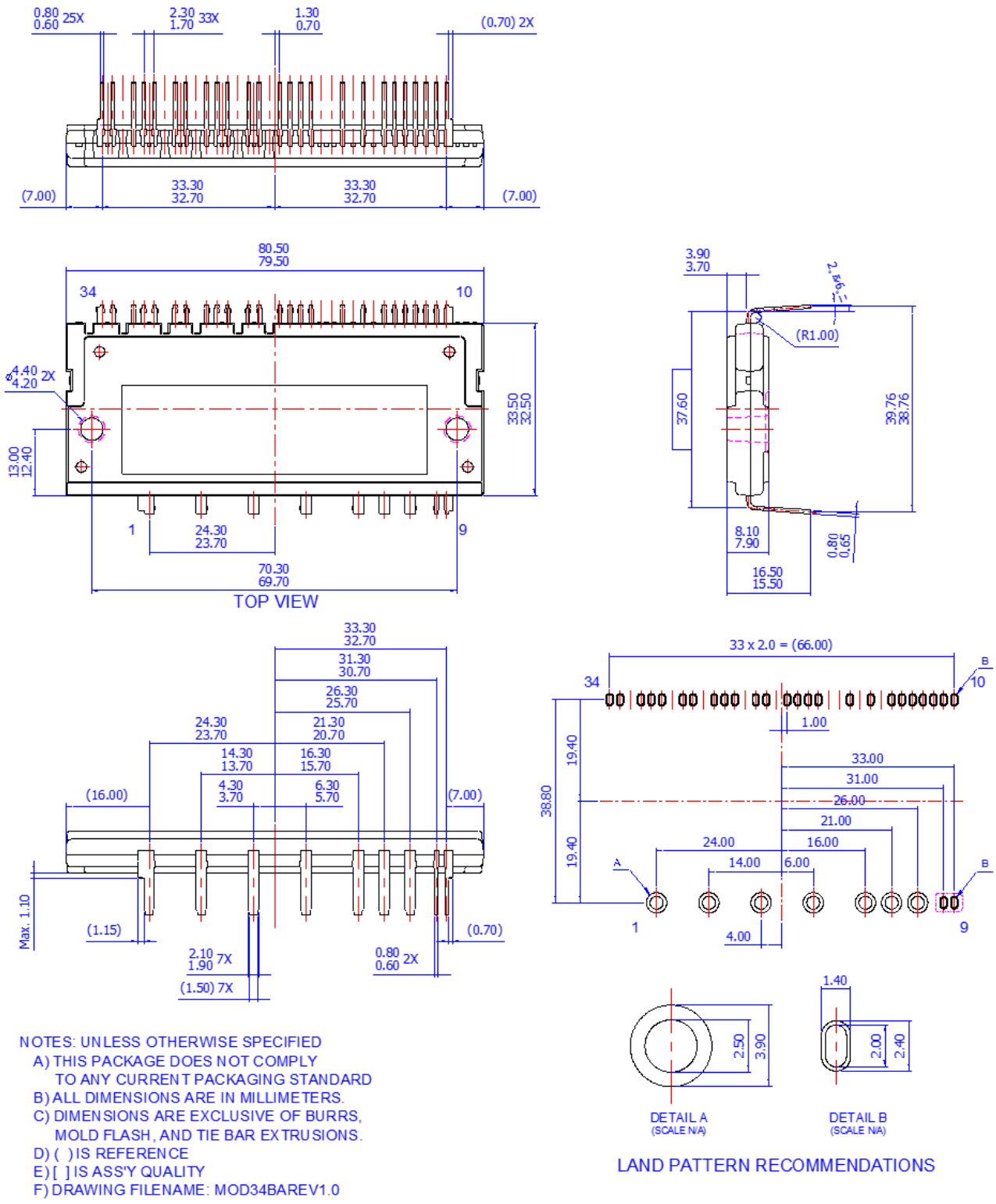
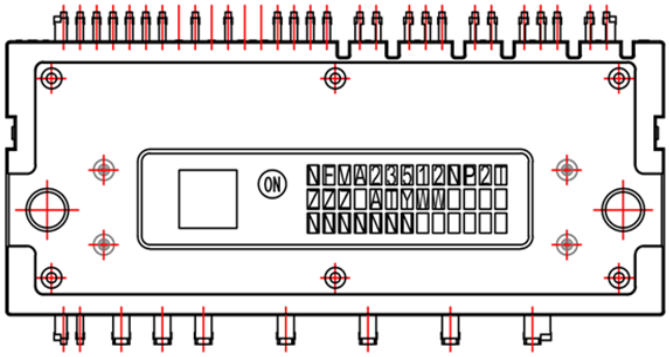
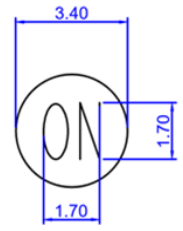


Figure 8. Package Outline Drawing

Marking Specification

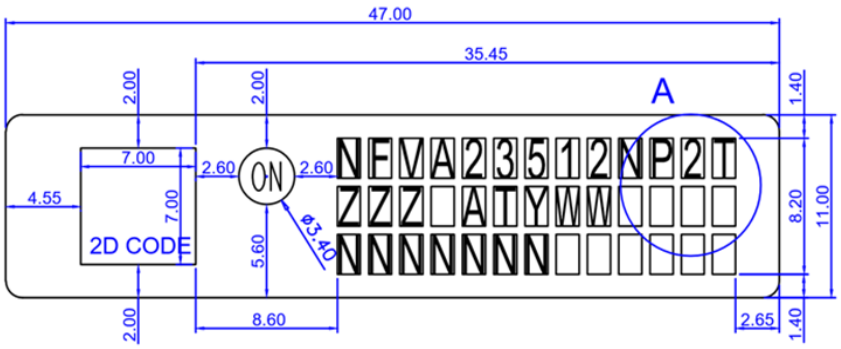
* MARKING LAY-OUT (SCALE 1 : 1)



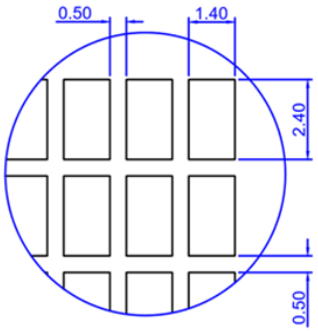


COMPANY LOGO
(SCALE N/A)

* MARKING DIMENSION



(SCALE 2 : 1)



DEATIL A (SCALE 4 : 1)

* 2D CODE

NFVA23512NP2Tzzz11H24A0000001

Part Number
Lot Number
Assembly & Test Site
Date Code
Marking Machine ID
Serial Number

Y	Alphabet
2017	J
2018	K
2019	L
2020	M
2021	N
2022	O
2023	P
2024	Q
2025	R
2026	S
2027	T

* NOTE
1. ON : COMPANY LOGO
2. NFVA~ : OPN
3. ZZZ : LAST 3 DIGITS OF LOT NO
4. AT : ASSEMBLY & TEST SITE (SUZHOU : 1)
5. YWW : DATE CODE (Y : YEAR-SEE THE TABLE, WW : WORK WEEK)
6. NNNN : SERIAL NUMBER

Figure 9. Marking Layout

PRODUCT SYNOPSIS

This section discusses electrical specification, characteristics and mechanical characteristics.

Absolute Maximum Rating (T_J = 25°C, Unless Otherwise Specified)

Table 3. INVERTER PART (BASE ON NFVA25012NP2T)

Symbol	Parameter	Conditions		Rating	Unit
V_{PN}	Supply Voltage	Applied between P –NU, NV, NW		900	V
$V_{PN(Surge)}$	Supply Voltage (Surge)	Applied between P – NU, NV, NW		1000	V
V_{CES}	Collector – Emitter Voltage			1200	V
$\pm I_C$	Each IGBT Collector Current	T_C = 100°C, $T_{DD} \le$ 15V, $T_J \le$ 150°C (Note 2)		50	A
$\pm I_{CP}$	Each IGBT Collector Current (Peak)	T_C = 25°C, $T_J \le$ 150°C, Under 1 ms Pulse Width (Note 3)		75	A
P_C	Collector Dissipation	T_C = 25°C per One Chip (Note 3)		347	W
T_J	Operating Junction Temperature (Note 3)	IGBT and Diode	V_{CES} = 960 V	–40~150	°C
			V_{CES} = 1200 V	–40~125	
		Driver IC		–40~150	

2. These values had been made an acquisition by the calculation considered to design factor.
3. The maximum junction temperature rating of power chips integrated within the 1200 V ASPM34 products is 150°C.

Table 4. CONTROL PART

Symbol	Parameter	Conditions	Rating	Unit
V_{DD}	Control Supply Voltage	Applied between $V_{DD(H)}$, $V_{DD(L)}$ – COM	20	V
V_{BS}	High–Side Control Bias Voltage	Applied between $V_{B(U)}$–$V_{S(U)}$, $V_{B(V)}$–$V_{S(V)}$, $V_{B(W)}$–$V_{S(W)}$	20	V
V_{IN}	Input Signal Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ – COM	–0.3~V_{DD} + 0.3	V
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO} – COM	–0.3~V_{DD} + 0.3	V
I_{FO}	Fault Output Current	Sink Current at V_{FO} Pin	2	mA
V_{SC}	Current Sensing Input Voltage	Applied between C_{SC} – COM	–0.3~V_{DD} + 0.3	V

Table 5. BOOTSTRAP DIODE PART

Symbol	Parameter	Conditions	Rating	Unit
V_{RRM}	Maximum Repetitive Reverse Voltage		1200	V
I_F	Forward Current	TC = 25°C, TJ ≤ 150°C (Note 3)	1.0	A
I_{FP}	Forward Current (Peak)	TC = 25°C, TJ ≤ 150°C, Under 1 ms Pulse Width (Note 3)	2.0	A
T_j	Operating Junction Temperature (Note 5)		–40~150	°C

Table 6. TOTAL SYSTEM

Symbol	Parameter	Conditions	Rating	Unit
t_{SC}	Short Circuit Withstand Time	VDD = VBS ≤ 16.5 V, VPN ≤ 800 V, TJ = 150°C Non–repetitive	3	μs
T_{STG}	Storage Temperature		–40~150	°C
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, 1–Minute, Connect Pins to Heat Sink	2500	Vrms

Table 7. THERMAL RESISTANCE

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance (Note 4)	Inverter IGBT Part (per 1/6 Module)	–	–	0.36	°C/W
$R_{th(j-c)F}$		Inverter FWD Part (per 1/6 Module)	–	–	0.66	
Lσ	Package Stray Inductance	P to N_U, N_V, N_W (Note 5)	–	32	–	nH

4. For the measurement point of case temperature (T_C), please refer Figure 10. DBC discoloration and Picker Circle Printing allowed, please refer to application note AN−9190 (Impact of DBC Oxidation on SPM® Module Performance).
5. Stray inductance per phase measured per IEC 60747−15.

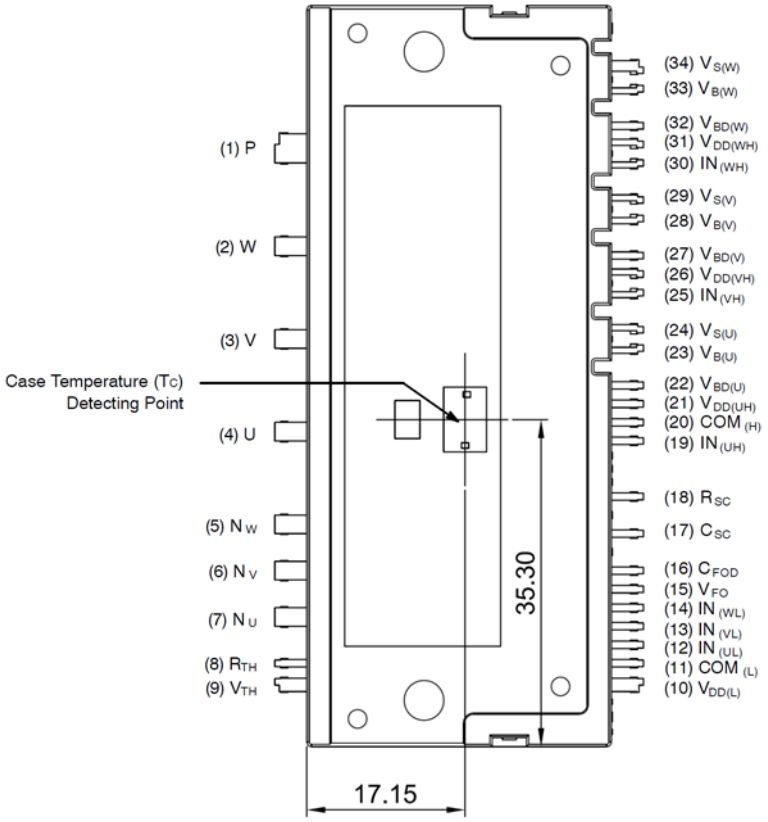


Figure 10. Case Temperature (T_C) Detecting Point

Electrical Characteristic (T_J = 25°C, Unless Otherwise Specified)

Table 8. INVERTER PART (BASE ON NFVA25012NP2T)

Symbol		Parameter	Condition		Min	Typ	Max	Unit
$V_{CE(SAT)}$		Collector–Emitter Saturation Voltage	V_{DD}, V_{BS} = 15 V, V_{IN} = 5 V	I_C = 50 A, T_J = 25°C	–	2.20	2.80	V
				I_C = 50 A, T_J = 150°C	–	2.75	3.25	V
V_F		FWDi Forward Voltage	V_{IN} = 0 V	I_F = 50 A, T_J = 25°C	–	2.40	3.00	V
				I_F = 50 A, T_J = 150°C	–	2.25	2.85	V
HS	t_{ON}	Switching Times	V_{PN} = 600 V, V_{DD} = 15 V, I_C = 30 A T_J = 25°C, V_{IN} = 0 V ↔ 5 V, Inductive Load See Figure 12 (Note 6)		0.90	1.40	2.00	μs
	$t_{C(ON)}$				–	0.50	0.95	μs
	t_{OFF}				–	1.10	1.70	μs
	$t_{C(OFF)}$				–	0.15	0.55	μs
	t_{rr}				–	0.20	–	μs
LS	t_{ON}				0.50	1.00	1.60	μs
	$t_{C(ON)}$				–	0.50	0.95	μs
	t_{OFF}				–	1.10	1.70	μs
	$t_{C(OFF)}$				–	0.25	–	μs
	t_{rr}				–	0.15	–	μs
I_{CES}		Collector – Emitter Leakage Current	T_J = 25°C, V_{CE} = V_{CES}		–	–	3	mA

6. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detail information, please see Figure 11 and Figure 12.

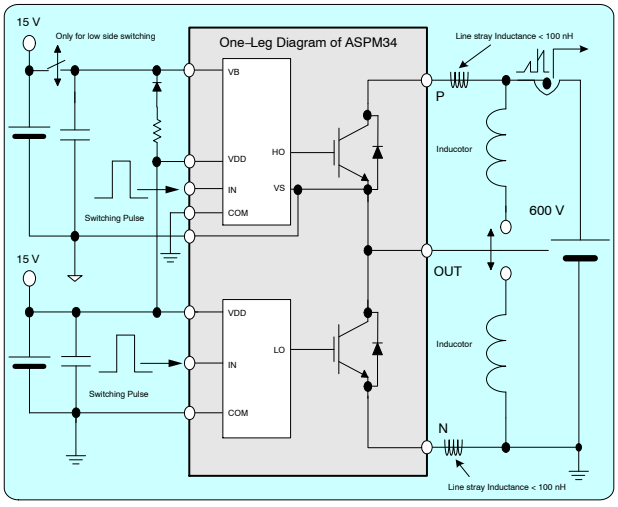


Figure 11. Switching Evaluation Circuit

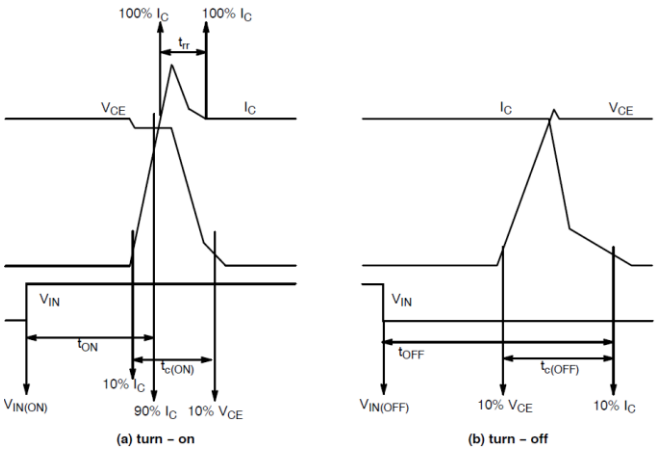


Figure 12. Switching Evaluation Circuit and Switching Time Definition

Table 9. BOOTSTRAP DIODE PART (BASE ON NFVA25012NP2T, T_j AS SPECIFIED)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_F	Forward Voltage	I_F = 1.0 A, Tj = 25°C	–	2.2	–	V
t_{rr}	Reverse–Recovery Time	I_F = 1.0 A, dI_F / dt = 50 A/ms, TJ = 25°C	–	80	–	ns

Table 10. CONTROL PART (BASE ON NFVA25012NP2T)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
I_{QDDH}	Quiescent V_{DD} Supply Current	$V_{DD(UH,VH,WH)}$ = 15 V, $IN_{(UH,VH,WH)}$ = 0 V	$V_{DD(UH)} - COM_{(H)}$, $V_{DD(VH)} - COM_{(H)}$, $V_{DD(WH)} - COM_{(H)}$	–	–	0.15	mA
I_{QDDL}		$V_{DD(L)}$ = 15 V, $IN_{(UL,VL,WL)}$ = 0 V	$V_{DD(L)} - COM_{(L)}$	–	–	4.80	
I_{PDDH}	Operating V_{DD} Supply Current	$V_{DD(UH,VH,WH)}$ = 15 V, f_{PWM} = 20 kHz, Duty = 50%, Applied to one PWM Signal Input for High Side	$V_{DD(UH)} - COM_{(H)}$, $V_{DD(VH)} - COM_{(H)}$, $V_{DD(WH)} - COM_{(H)}$	–	–	0.30	mA
I_{PDDL}		$V_{DD(L)}$ = 15 V, f_{PWM} = 20 kHz, Duty = 50%, Applied to One PWM Signal Input for Low Side	$V_{DD(L)} - COM_{(L)}$	–	–	15.5	mA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{BS} = 15 V, $IN_{(UH,VH,WH)}$ = 0 V	$VB_{(U)} - VS_{(U)}$, $VB_{(V)} - VS_{(V)}$, $VB_{(W)} - VS_{(W)}$	–	–	0.30	mA
I_{PBS}	Operating V_{BS} Supply Current	V_{DD} = V_{BS} = 15 V, f_{PWM} = 20 kHz, Duty = 50%, Applied to One PWM Signal Input for High Side	$VB_{(U)} - VS_{(U)}$, $VB_{(V)} - VS_{(V)}$, $VB_{(W)} - VS_{(W)}$	–	–	12.0	mA
V_{FOH}	Fault Output Voltage	V_{DD} = 15 V, V_{SC} = 0 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull−up		4.5	–	–	V
V_{FOL}		V_{DD} = 15 V, V_{SC} = 1 V, V_{FO} Circuit: 4.7kΩ to 5 V Pull−up		–	–	0.5	
I_{SEN}	Sensing Current of Each Sense IGBT	V_{DD} = 15 V, V_{IN} = 5 V, R_{SC} = 0 Ω, No Connection of Shunt Resistor at NU,V,W Terminal	I_c = 50 A	–	43	–	mA
$V_{SC(ref)}$	Short−Circuit Trip Level	V_{DD} = 15 V (Note 7)	$C_{SC} - COM_{(L)}$	0.43	0.50	0.57	V
I_{SC}	Short Circuit Current Level for Trip	RSC = 13 Ω (±1%), No Connection of Shunt Resistor at NU, V, W Terminal (Note 7)		–	75	–	A
UV_{DDD}	Supply Circuit, Under−Voltage Protection	Detection Level		10.3	–	12.8	V
UV_{DDR}		Reset Level		10.8	–	13.3	
UV_{BSD}		Detection Level		9.5	–	12.0	
UV_{BSR}		Reset Level		10.0	–	12.5	
t_{FOD}	Fault−Out Pulse Width	C_{FOD} = Open	(Note 8)	50	–	–	μs
		C_{FOD} = 2.2 nF		1.7	–	–	ms
$V_{IN(ON)}$	ON Threshold Voltage	Applied between $IN_{(UH,VH,WH)} - COM_{(H)}$, $IN_{(UL,VL,WL)} - COM_{(L)}$		–	–	2.6	V
$V_{IN(OFF)}$	OFF Threshold Voltage			0.8	–	–	
R_{TH}	Resistance of Thermistor	at T_{TH} = 25°C	See Figure 13 (Note 9)	–	47	–	kΩ
		at T_{TH} = 100°C		–	2.9	–	

7. Short−circuit current protection is functioning only at the low-sides.
8. The fault−out pulse width t_{FOD} depends on the capacitance value of C_{FOD} according to the following approximate equation: t_{FOD} = 0.8 x 106 x CFOD [s].
9. T_{TH} is the temperature of thermistor itself. To know case temperature (T_C), conduct experiments considering the application.

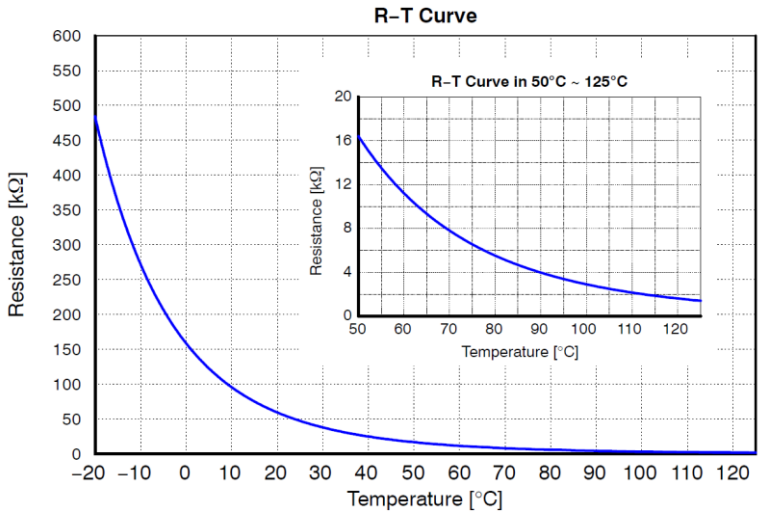


Figure 13. Temperature Profile of V_{TS} (Typical)

Table 11. RECOMMENDED OPERATING CONDITIONS (BASE ON NFVA25012NP2T)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PN}	Supply Voltage	Applied between P – N_U, N_V, N_W	300	600	800	V
V_{DD}	Control Supply Voltage	Applied between $V_{DD(UH,VH,WH)}$ – $COM_{(H)}$, $V_{DD(L)}$ – $COM_{(L)}$	14.0	15.0	16.5	V
V_{BS}	High−Side Bias Voltage	Applied between $V_{B(U)}$ – $V_{S(U)}$, $V_{B(V)}$ – $V_{S(V)}$, $V_{B(W)}$ – $V_{S(W)}$	13.0	15.0	18.5	V
dV_{DD}/dt, dV_{BS}/dt	Control Supply Variation		−1	–	1	V/μs
t_{dead}	Blanking Time for Preventing Arm−Short	For Each Input Signal	2.0	–	–	μs
f_{PWM}	PWM Input Signal	−40°C ≤ T_C ≤ 125°C, −40°C ≤ T_J ≤ 150°C	–	–	20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between N_U, N_V, N_W – $COM_{(H,L)}$ (Including Surge Voltage)	−5	–	5	V
$P_{WIN(ON)}$	Minimum Input Pulse Width	V_{DD} = V_{BS} = 15 V, I_C ≤ 75 A, Wiring Inductance between $N_{U,V,W}$ and DC Link N < 10 nH (Note 10)	2.5	–	–	μs
$P_{WIN(OFF)}$			2.5	–	–	
T_J	Junction Temperature		−40	–	150	°C

10. This product might not make response if input pulse with is lee than the recommended value.

Table 12. MECHANICAL CHARACTERISTICS

Parameter	Condition		Min	Typ	Max	Unit
Device Flatness	See Figure 14		0	–	+150	μm
Mounting Torque	Mounting Screw: M4 See Figure 15	Recommended 1.0 N·m	0.9	1.0	1.5	N·m
		Recommended 10.1 kg·cm	9.1	10.1	15.1	kg·cm
Terminal Pulling Strength	Load 19.6 N		10	–	–	s
Terminal Bending Strength	Load 9.8 N, 90° Bend		2	–	–	Times
Weight	Module Weight		–	50	–	g

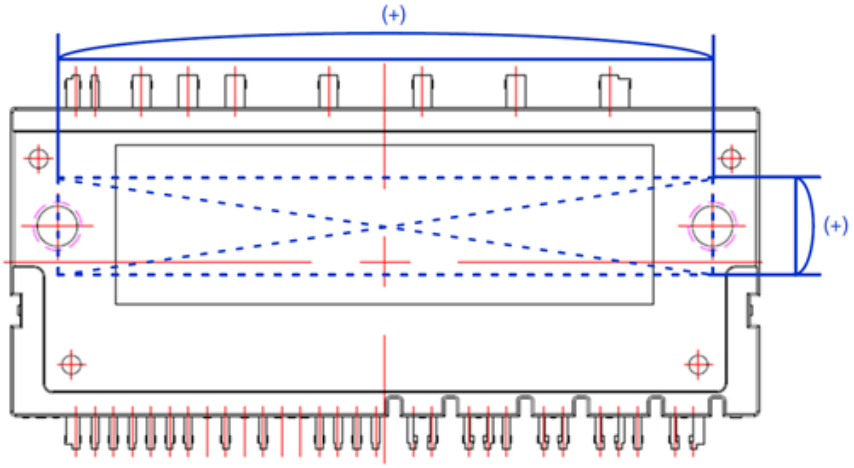
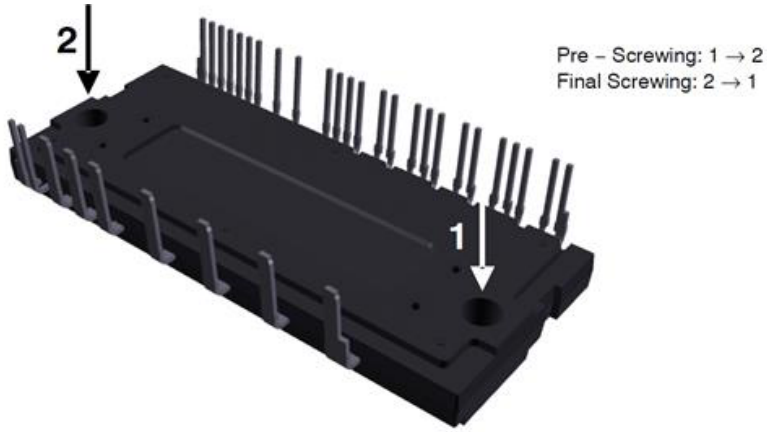


Figure 14. Flatness Measurements Position



NOTES:

11. Do not make over torque when mounting screws. Much mounting torque may cause DBC crack, as well as bolts Al heat sink destruction.
12. Avoid one−sided tightening stress, Figure 15 shows the recommended torque order for mounting order for mounting screws. Uneven mounting can cause the DBC substrate of package to be damaged. The pre−screwing torque is set to 20~30% of maximum torque rating.

Figure 15. Mounting Screw Torque Order

OPERATION SEQUENCE FOR PROTECTIONS

Short Circuit Protection

The 1200 V ASPM34 uses a sense current detecting resistor (R_{SC}) for the short circuit current detection, as shown in Figure 16. LVIC has a built−in short−circuit current protection function. This protection function senses the voltage to the C_{SC} pin. If this voltage exceeds the V_{SC}(ref) (the threshold voltage trip level of the short−circuit) specified in the device datasheets (typ. V_{SC}(ref) is 0.5 V), a fault signal is asserted and the all low side IGBTs are turned off. Typically, the maximum short−circuit current magnitude is gate−voltage dependent: higher gate voltage (V_{DD} & V_{BS}) results in larger short−circuit current. To avoid potential problems, the maximum short−circuit trip level is set below 1.7 times the nominal rated collector current. The LVIC short−circuit current protection−timing chart is shown in Figure 17.

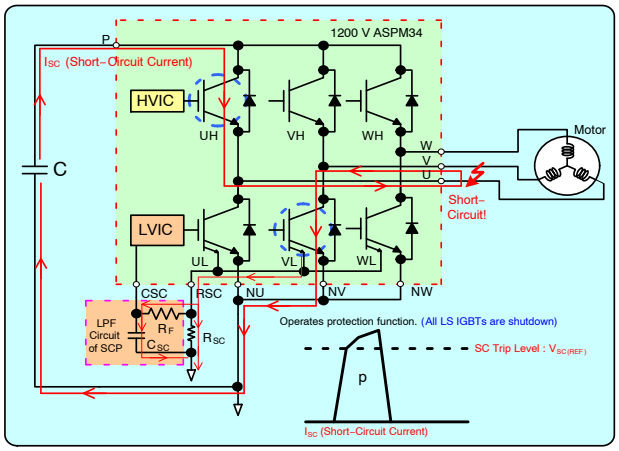
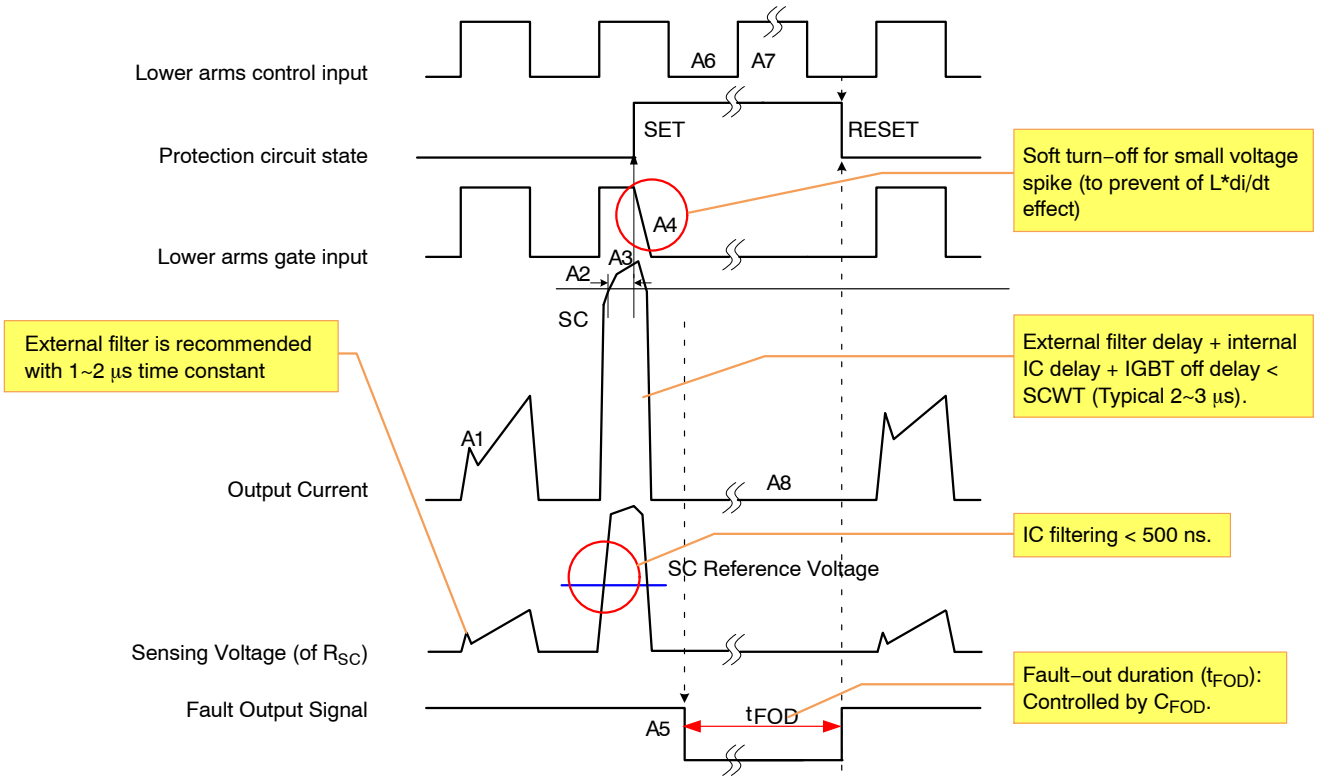


Figure 16. Operation of Short−Circuit Protection

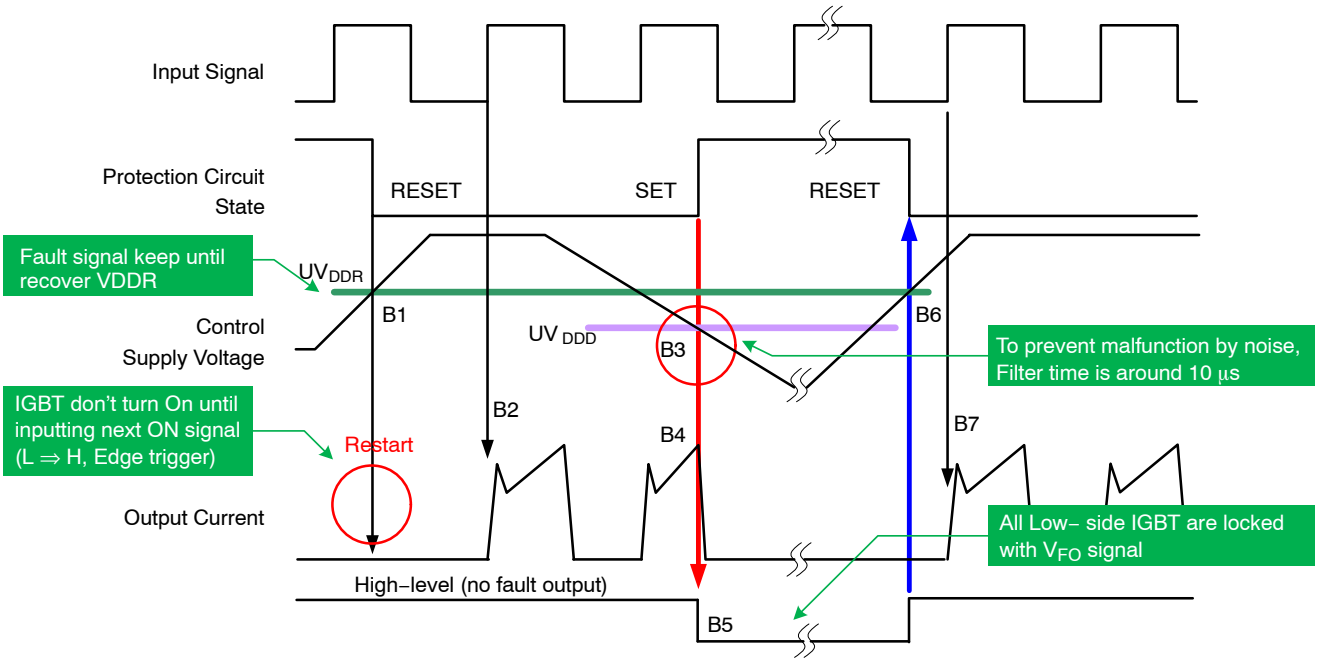


NOTES:
13. A1 - normal operation: IGBT on and carrying current.
14. A2 - short−circuit current detection (SC trigger).
15. A3 - hard IGBT gate interrupt.
16. A4 - IGBT turns OFF by soft−off function.
17. A5 - fault output timer operation start with internal delay (typ. 2.0 μs), t_{FOD} = controlled by C_{FOD}.
18. A6 - input “L”: IGBT OFF state.
19. A7 - input “H”: IGBT ON state, but during the active period of fault output the IGBT doesn’t turn ON.
20. A8 - IGBT keeps OFF state

Figure 17. Timing Chart of Short−Circuit Protection Function

Under−Voltage Lockout Protection (Low−side UVLO)

The LVIC has an Under−Voltage Lockout protection (UVLO) function to protect the low−side IGBTs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 18.



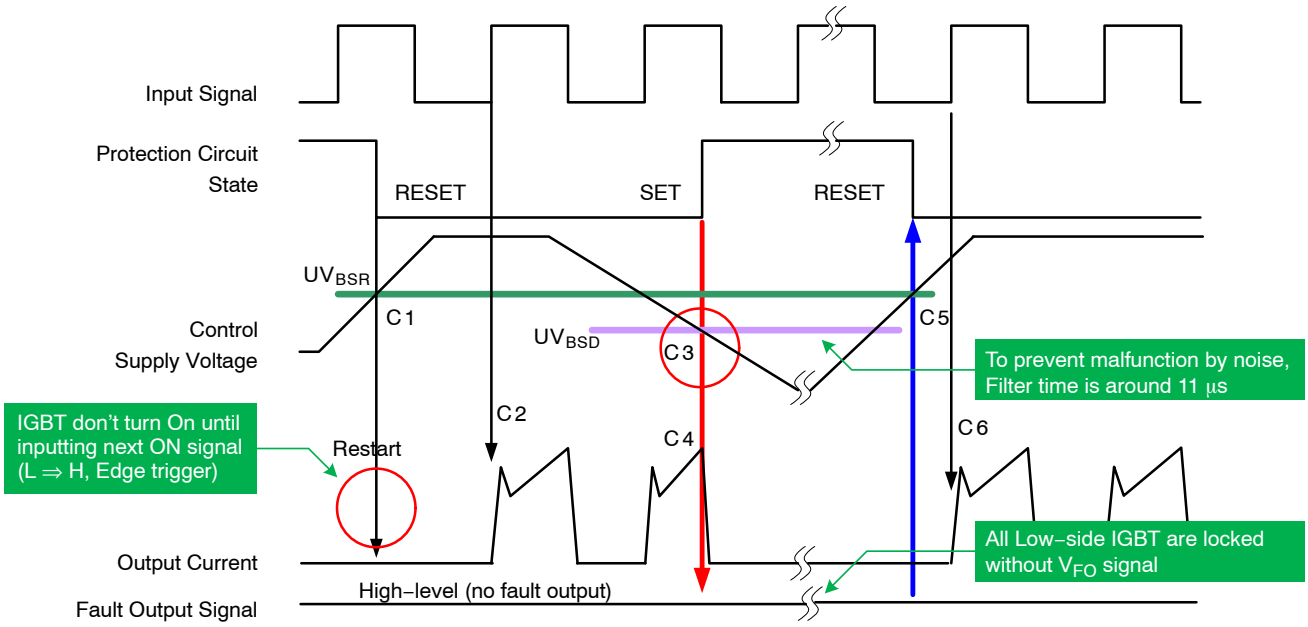
NOTES: *(Low−Side Protection Sequence)*

21. B1 − control supply voltage rise: after the voltage rises UV_{DDR}, the circuits starts to operate when the next input is applied (L ⇒ H)
22. B2 − normal operation: IGBT ON and carrying current.
23. B3 − under−voltage detection (UV_{DDD}).
24. B4 − IGBT OFF in spite of control input is alive.
25. B5 − Fault output signal starts.
26. B6 − under−voltage reset (UV_{DDR}).
27. B7 − normal operation: IGBT ON and carrying current. If fault−out duration (t_{FOD}) by external capacitor at C_{FOD} pin is longer than UV_{DDR} timing, fault output and IGBT state are cleared after t_{FOD}.

Figure 18. Timing Chart of Low−side Under−Voltage Protection Function

Under−Voltage Lockout Protection (High−side UVLO)

The HVIC has an under−voltage lockout function to protect the high−side IGBT from insufficient gate driving voltage. A timing chart for this protection is shown in Figure 19. The fault−out (FO) alarm is not given for low HVIC bias conditions.



NOTES: (High−Side Protection Sequence)
28. C1 − control supply voltage rises: after the voltage reaches UV_{BSR}, the circuit starts when the next input is applied (L ⇒ H).
29. C2 − normal operation: IGBT ON and carrying current.
30. C3 − under−voltage detection (UV_{BSD}).
31. C4 − IGBT OFF in spite of control input is alive, but there is no fault output signal.
32. C5 − under−voltage reset (UV_{BSR}).
33. C6 − normal operation: IGBT ON and carrying current

Figure 19. Timing Chart of High-Side Under-Voltage Protection Function

KEY PARAMETER DESIGN GUIDANCE

For stable operation, there are recommended parameters for passive components and bias conditions, considering operating characteristics of the 1200 V ASPM34.

Selection of RSC Resistor for Protection

Figure 20 is an example circuit of the short−circuit protection using the R_{SC} resistor. Sense IGBT is employed for the low side. The designer can use the R_{SC} pin for Over−Current Protection (OCP) and Short−Circuit Protection (SCP) without an external shunt resistor at the N−terminal. The line current on R_{SC} is detected and the protective operation signal is passed through the RC filter. If the current exceeds the V_{SC}(ref), all the gates of the N−side three IGBTs are turned off and the fault signal is transmitted from the 1200 V ASPM34 to MCU. Since repetitive short circuit is not allowable, IGBT operation should be immediately halted when the fault signal is given.

Figure 21 shows "R_{SC} resistance vs. trip current" curve of NFVA22512NP2T under the shunt resistor = 0 Ω condition.

For current sensing, apply an external shunt resistor at each N terminal. Sensing voltage from R_{SC} pin is influenced by an external shunt resistor, as shown in Figure 22.

For adequate R_{SC} value in a three−shunt structure, the R_{SC} value needs to be considered by the N−terminal shunt resistor value and target protection current level.

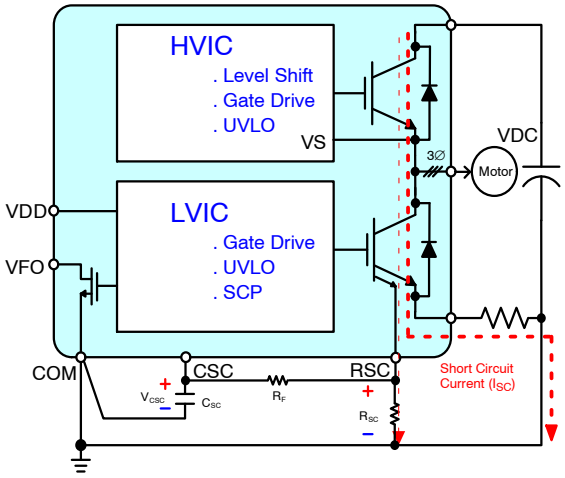


Figure 20. Current Path in Short−Circuit Condition by Leg Short Circuit

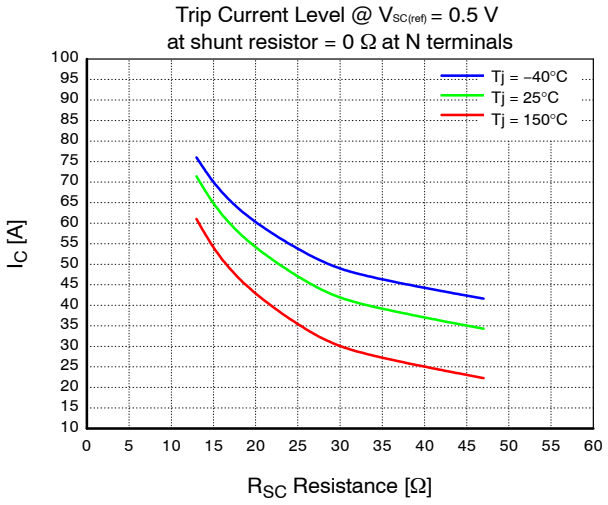


Figure 21. RSC Resistance vs. Trip Current Level for Protection at Variable Junction Temperature of NFVA22512NP2T

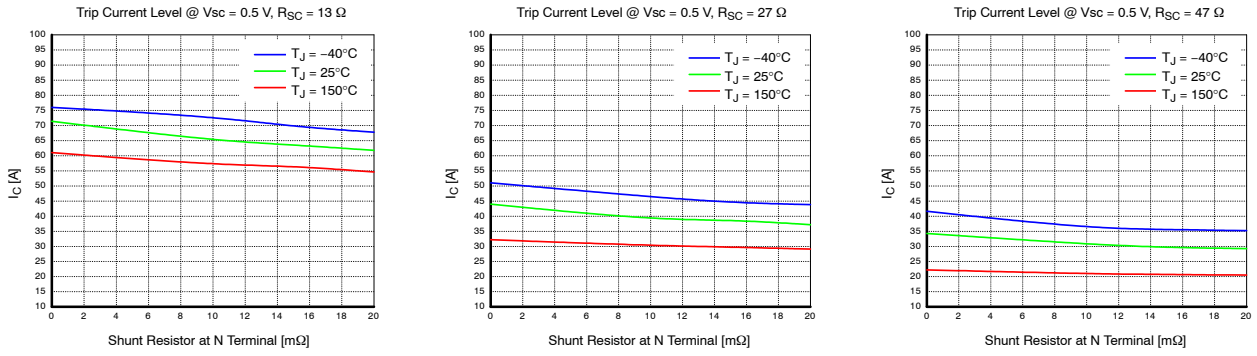


Figure 22. Trip Current Level vs. Shunt Resistor of NFVA22512NP2T (a): R_{SC} = 13 Ω, (b): R_{SC} = 27 Ω, (c): R_{SC} = 47 Ω

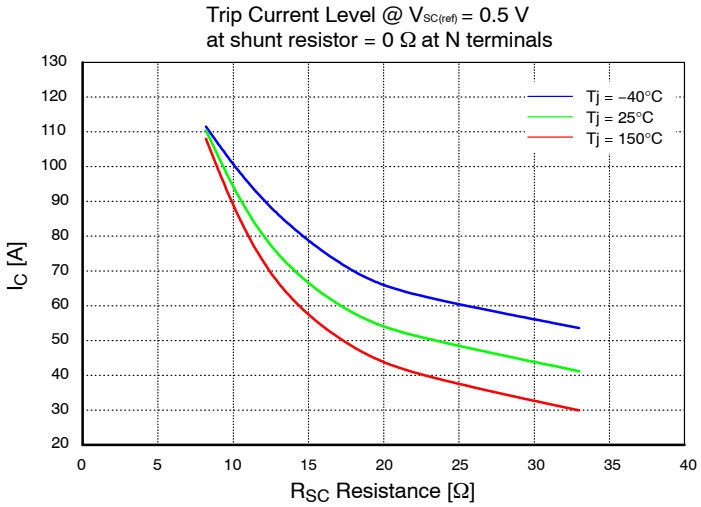


Figure 23. RSC Resistance vs. Trip Current Level for Protection at Variable Junction Temperature of NFVA235(50)12NP2T

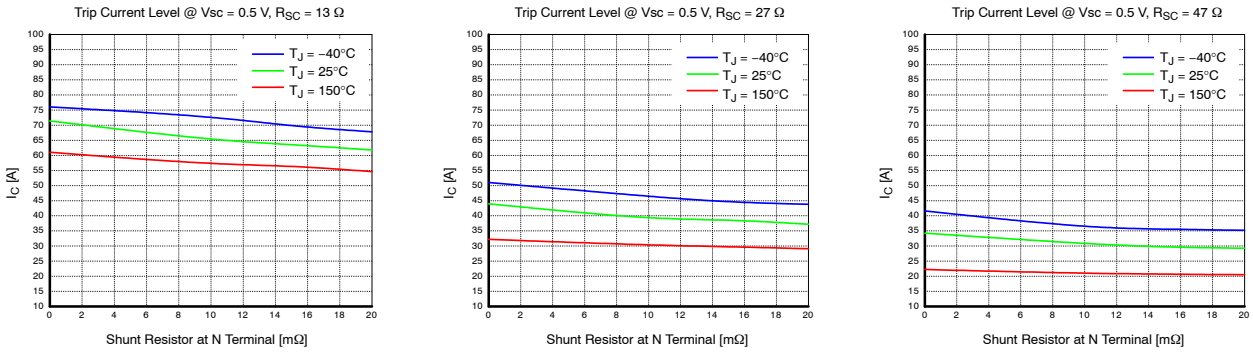


Figure 24. Trip Current Level vs. Shunt Resistor of NFVA235(50)12NP2T (a): R_{SC} = 8.2 Ω, (b): R_{SC} = 16 Ω, (c): R_{SC} = 30 Ω

Shunt Resistor Selection at N−Terminal for Current Sensing & Protection

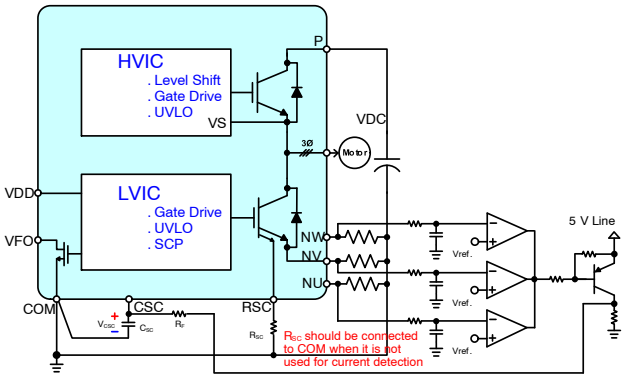


Figure 25. Recommended Circuitry for Over−Current & Short−Circuit Protection without RSC Pin Usage

If using three shunt resistors at N terminals for OCP and SCP without sense detecting from R_{SC}, R_{SC} should be connected to COM. The external RC time constant from the N−terminal shunt resistor to C_{SC} must be lower than 2 μs in short circuit for stable shutdown.

The proper shunt resistance can be calculated by simple equations as below.

$V_{SC(ref)}$ = min.0.43 V / typ. 0.5 V / max. 0.57 V (see Table 13.)

- Shunt Resistance:

$$I_{SC(max)} = V_{SC(max)} / R_{SHUNT(min)}$$
$$\rightarrow R_{SHUNT(min)} = V_{SC(max)} / I_{SC(max)} \quad \text{(eq. 1)}$$

If the deviation of shunt resistor is limited below ±5%:

$$R_{SHUNT(typ)} = R_{SHUNT(min)} / 0.95$$
$$\rightarrow R_{SHUNT(max)} = R_{SHUNT(typ)} \times 1.05 \quad \text{(eq. 2)}$$

- The Actual SC Trip Current Level becomes:

$$I_{SC(typ)} = V_{SC(typ)} / R_{SHUNT(typ)}$$
$$\rightarrow I_{SC(min)} = V_{SC(min)} / R_{SHUNT(max)} \quad \text{(eq. 3)}$$

- Inverter Output Power:

$$P_{OUT} = \sqrt{3} \times V_{O\_LL} \times I_{RMS} \times PF \quad \text{(eq. 4)}$$

$$V_{O\_LL} = \frac{\sqrt{3}}{\sqrt{2}} \times MI \times \frac{1}{2} \times V_{DC\_Link} \quad \text{(eq. 5)}$$

Where:

V_{O_LL}: Inverter Output Lin to Line

MI = Modulation Index

V_{DC_Link} = DC link voltage

I_{RMS} = Maximum load current of inverter

PF = Power Factor

- Average DC Current:

$$IDC\_AVG = VDC\_Link / (Pout \rightarrow Eff) \quad \text{(eq. 6)}$$

Where: Eff = Inverter efficiency

- The power rating of shunt resistor is calculated by:

$$P_{SHUNT} = (I^2_{DC\_AVG} \times R_{SHUNT} \times Margin) / De\text{−}rating\ Ratio \quad \text{(eq. 7)}$$

Where:

I_{DC_AVG}: Average load current of inverter

R_{SHUNT}: Shunt resistor typical value at TC = 25 [°C]

De-rating ratio:

Shunt resistor at T_{SHUNT} = 100 [°C] from datasheet of shunt resistor

Margin: Safety margin determined by customer's system.

Table 13. OCP & SCP LEVEL (VSC (REF)) SPECIFICATION

Conditions	Min	Typ	Max	Unit
Specification at T_J = 25°C, V_{DD} = 15 V	0.43	0.50	0.57	V

Shunt Resistor Calculation Examples Calculation Conditions:

- DUT: NFVA25012NP2T
- Tolerance of shunt resistor: ±5%
- T.C.R: 350 ppm/°C
- SC Trip Reference Voltage: $V_{SC(min)}$ = 0.43 V, $V_{SC(typ)}$ = 0.50 V, $V_{SC(max)}$ = 0.57 V
- Maximum Load Current of Inverter (I_{RMS}): 12 A_{rms}
- Maximum Peak Load Current of Inverter ($I_{C(max)}$): 25 A
- Modulation Index(MI): 0.9
- DC Link Voltage(V_{DC_Link}): 600V
- Power Factor(PF): 0.8
- Inverter Efficiency(Eff): 0.95
- De−rating Ratio of Shunt Resistor at T_{SHUNT} = 100°C: 70% (refer to Figure 26.)
- Safety Margin: 20%

Calculation Results:

- $I_{SC(min)} = I_{c(max)}$ = 25 A
- $R_{SHUNT(max)}$ @ Tj = 150°C = VSC(min) / Isc(min) = 0.43 V / 25 A = 17.2 mΩ
- $R_{SHUNT(max)} = R_{SHUNT(max)}$ @ Tj = 150°C / [1 + T.C.R x (150°C − 25°C)] = 17.2 mΩ / (1 + 350 x 10−6%/°C x 100°C) = 16.6 mΩ
- $R_{SHUNT(typ)} = R_{SHUNT(max)}$ / 1.05 = 15.8 mΩ
- $R_{SHUNT(min)} = R_{SHUNT(typ)}$ x 0.95 = 15.0 mΩ
- $I_{SC(typ)} = V_{SC(typ)} / R_{SHUNT(typ)}$ = 0.5 V / 15.8 mΩ = 31.6 A
- $I_{SC(max)} = V_{SC(max)} / R_{SHUNT(min)}$ = 0.57 V / 15.0 mΩ = 38.0 A

- $V_{O\_LL} = \frac{\sqrt{3}}{\sqrt{2}} \times MI \times \frac{1}{2} \times V_{DC\_Link}$
  $= \frac{\sqrt{3}}{\sqrt{2}} \times 0.9 \times 0.5 \times 600\ V = 330.7\ V$
- $P_{OUT} = \sqrt{3} \times V_{O\_LL} \times I_{RMS} \times PF$
  $= \sqrt{3} \times 330.7\ V \times 12\ A \times 0.8 = 5499\ W$
- I_{DC_AVG} = (P_{OUT} / Eff) / V_{DC_Link} = 5499 W / 0.95 / 600 V = 9.65 A
- P_{SHUNT} = ($I^2_{DC\_AVG}$ x $R_{SHUNT(max)}$ x Margin) / Derating Ratio = (9.65^2 x 0.0166 x 1.2) / 0.7 = 2.65 W

(Therefore, the proper power rating of shunt resistor is over 3.0 W)

When over−current events are detected, the 1200 V ASPM34 series shuts down all low−side IGBTs and sends out the fault−out (F_O) signal. Fault−out pulse width is fixed; minimum value is 50 μs.

To prevent malfunction, it is recommended that an RC filter be inserted at the C_{SC} pin. To shut down IGBTs within 3 μs when over−current situation occurs, a time constant of 1.5~2 μs is recommended.

Table 14. OPERATION SHORT−CIRCUIT RANGE OF FNVA22512NP2T

Conditions	Min	Typ	Max	Unit
R_{Shunt}	15.0	15.8	16.6	mΩ
Operation SC Level	25.0	31.6	38.0	A

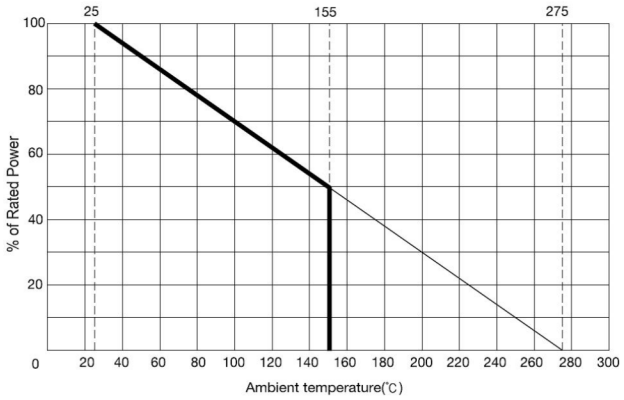
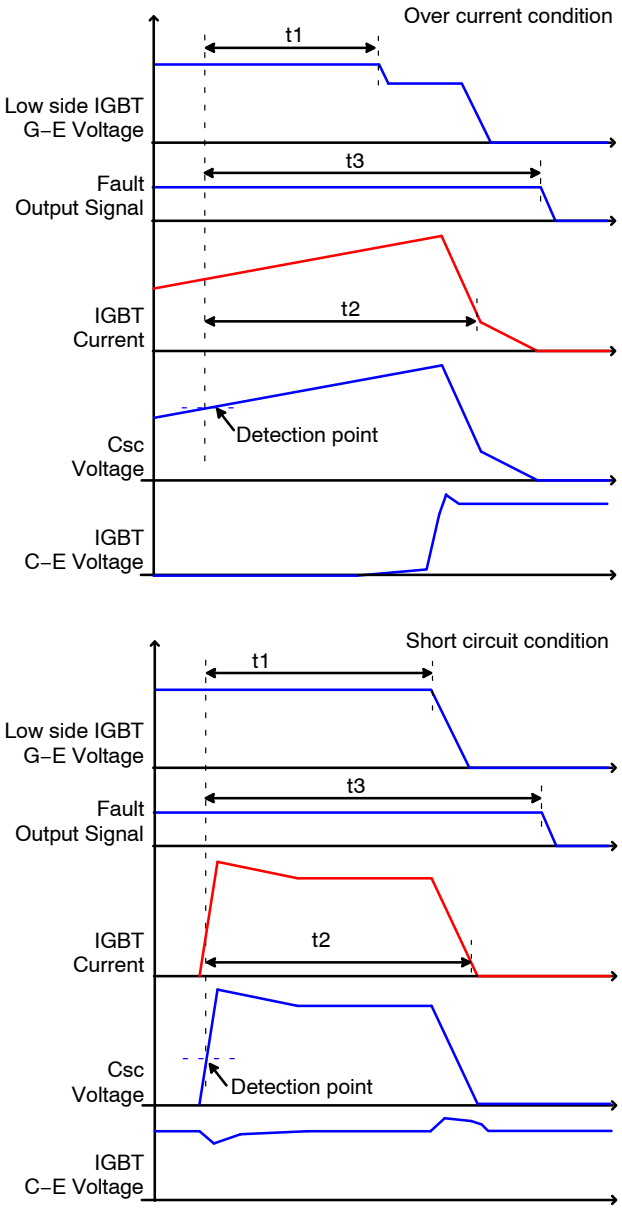


Figure 26. De−rating Curve Example of Shunt Resistor (from RARA Elec.)

Time Constant of Internal Delay

An RC filter is prevents noise−related Short−Circuit Current Protection (SCP) circuit malfunction. The RC time constant is determined by the applied noise time and the Short−Circuit Current Withstanding Time (SCWT) of the 1200 V ASPM34. When the R_{SC} voltage exceeds the SCP level, this is applied to the C_{SC} pin via the RC filter. The RC filter delay (T1) is the time required for the C_{SC} pin voltage to rise to the referenced SCP level. The LVIC has an internal filter time (logic filter time for noise elimination: T2). Consider this filter time when designing the RC filter of V_{CSC}.



NOTES:
34. t1: From CIN detection to gate driver LO shut down
35. t2: From CIN detection to collector current 10%
36. From CIN detection to fault out signal activation

Figure 27. Timing Diagram

Table 15. TIME TABLE OF OVER AND SHORT CIRCUIT CONDITIONS; $V_{SC(ref)}$ TO LOW SIDE GATE, COLLECTOR CURRENT AND V_{FO}

Ref. Condition V_{DCbus} = 600 V, V_{DD} = 15 V		Over Circuit Condition						Short Circuit Condition					
		t1 [μs]		t2 [μs]		t3 [μs]		t1 [μs]		t2 [μs]		t3 [μs]	
Device	Tj [°C]	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max
NFVA23512NP2T	25	1.90	2.40	2.40	3.00	3.45	4.30	2.25	2.80	2.50	3.15	3.75	4.70
	150	1.80	2.25	2.30	2.90	3.10	3.90	2.15	2.70	2.40	3.00	3.45	4.30

37. To guarantee safe short−circuit protection under all operating conditions, C_{SC} should be triggered within 1.0 μs after short−circuit occurs. (Recommendation: SCWT < 5.0 μs, Conditions: V_{DC} = 800 V, V_{DD} = 16.5 V, T_J = 150°C).
38. It is recommended that delay from short−circuit to C_{SC} triggering should be minimized.

Fault Output Circuit

Table 16. FAULT−OUTPUT MAXIMUM RATINGS

Symbol	Item	Condition	Rating	Unit
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO}−COM	−0.3~V_{DD} + 0.3	V
I_{FO}	Fault Output Current	Sink Current at V_{FO} Pin	2	mA

Table 17. ELECTRICAL CHARACTERISTICS

Symbol	Item	Conditions	Min	Max	Unit
V_{FOH}	Fault Output Supply Voltage	V_{DD} = 15 V, V_{SC} = 0, V_{FO} Circuit: 4.7kΩ to 5 V Pull−Up	4.5	−	V
V_{FOL}			−	0.5	V

Because V_{FO} terminal is an open−drain type; it should be pulled up via a pull−up resistor. The resistor must satisfy the above specifications.

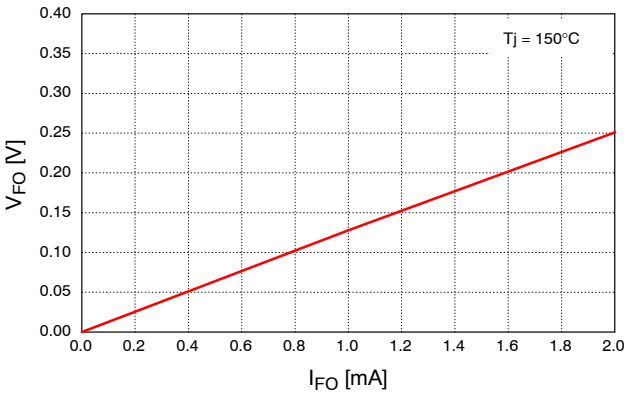


Figure 28. Voltage−Current Characteristics of V_{FO} Terminal

Circuit of Input Signal (IN(xH), IN(xL))

Figure 29 shows the I/O interface circuit between the MCU and 1200 V ASPM34. Because the 1200 V ASPM34 input logic is an active HIGH and there are built−in pull−down resistors, external pull−down resistors are not needed.

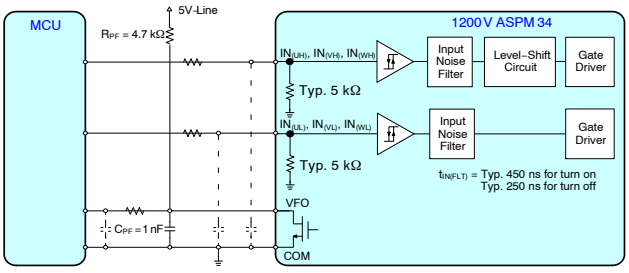


Figure 29. Recommended CPU I/O Interface Circuit

The input and fault output maximum rated voltages are shown in Table 18. Since the fault output is open drain, its rating is V_{DD} + 0.3 V, 15 V supply interface is possible. However, it is recommended that the fault output be configured with the 5 V logic supplies, which is the same as the input signals. It is also recommended that the de−coupling capacitors be placed at both the MCU and 1200 V ASPM34 ends of the V_{FO} signal line, as close as possible to each device. The RC coupling at each input (parts shown dotted in Figure 29) can be changed depending on the PWM control scheme used in the application and the wiring impedance of the PCB layout.

The input signal section of the 1200 V ASPM34 series integrates a 5 kΩ (typical) pull−down resistor. Therefore, when using an external filtering resistor between the MCU output and the 1200 V ASPM34 input, attention should be given to the signal voltage drop at the 1200 V ASPM34 input terminals to satisfy the turn−on threshold voltage requirement.

Table 18. MAXIMUM RATINGS OF INPUT AND V_{FO} PINS

Symbol	Item	Condition	Rating	Unit
VIN	Input Signal Voltage	Applied between $IN_{(xH)}$, $IN_{(xL)}$−COM(x)	−0.3~ V_{DD} + 0.3	V
VFO	Fault Output Supply Voltage	Applied between V_{FO}−COM(L)	−0.3~ V_{DD} + 0.3	V

Table 19. INPUT THRESHOLD VOLTAGE RATINGS (V_{DD} = 15 V, TJ = 25°C)

Symbol	Item	Condition	Min	Max	Unit
$V_{IN(ON)}$	Turn−On Threshold Voltage	$IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$−COM(H)	−	2.6	V
$V_{IN(OFF)}$	Turn−Off Threshold Voltage	$IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$−COM(L)	0.8	−	V

Bootstrap Circuit Design

Operation of Bootstrap Circuit

The V_{BS} voltage, which is the voltage difference between V_B (U, V, W) and V_S (U, V, W), provides the supply to the HVIC within the 1200 V ASPM34 series. This supply must be in the range of 13.0 V~18.5 V to ensure that the HVIC can fully drive the high−side IGBT. The under−voltage lockout protection for V_{BS} ensures that the HVIC does not drive the high−side IGBT if the V_{BS} voltage drops below a specific voltage (refer to the datasheet). This function prevents the IGBT from operating in a high−dissipation mode.

There are a number of ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described here. This method has the advantage of being simple and inexpensive. However, the duty cycle and on−time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap supply is formed by a combination of a bootstrap diode, resistor, and capacitor. The current flow path of the bootstrap circuit is shown in Figure 30. When V_S is pulled down to ground (low−side IGBT turn−on or low−side FRD freewheeling), the bootstrap capacitor (C_{BS}) is charged through the bootstrap diode (D_{BS}) and the resistor (RBS) from the V_{DD} supply.

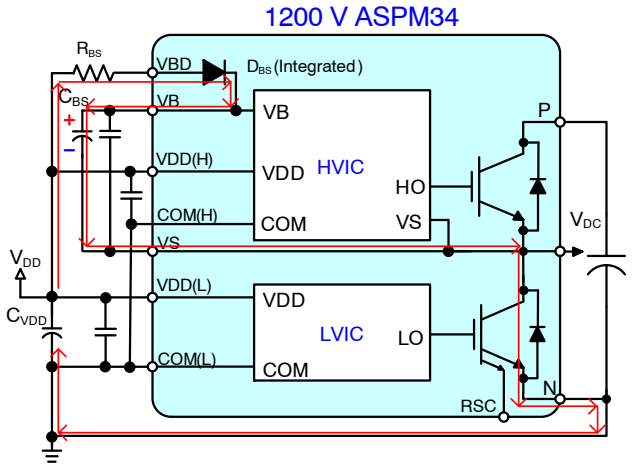


Figure 30. Current Path of Bootstrap Circuit for the Supply Voltage (VBS) when Low−Side IGBT Turns On

Selection of Bootstrap Capacitor Considering Initial Charging

Adequate on−time of the low−side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (tcharge) can be calculated by:

$$t_{charge} = C_{BS} \times R_{BS} \times \frac{1}{\Delta} \times \ln \frac{V_{CC}}{V_{CC} - V_{BS(min)} - V_F - V_{LS}} \quad \text{(eq. 8)}$$

Where:

V_F = *Forward voltage drop across the bootstrap diode;*

$V_{BS(min)}$ = *The minimum value of the bootstrap capacitor;*

V_{LS} = *Voltage drop across the low−side IGBT or load; and*

Δ = Duty ratio of PWM.

When the bootstrap capacitor is charged initially; V_{DD} drop voltage is generated based on initial charging method, V_{DD} line SMPS output current, V_{DD} source capacitance, and bootstrap capacitance. If V_{DD} drop voltage reaches UV_{CCD} level, the low side is shutdown and a fault signal is activated. To avoid this malfunction, related parameter and initial charging method should be considered. To reduce V_{DD} voltage drop at initial charging, a large V_{DD} source capacitor and selection of optimized low−side turn−on method are recommended. Adequate on−time duration of the low−side IGBT to fully charge the bootstrap capacitor is initially required before normal operation of PWM starts.

Figure 32 shows an example of initial bootstrap charging sequence. Once V_{DD} establishes, V_{BS} needs to be charged by turning on the low−side IGBTs. PWM signals are typically generated by an interrupt triggered by a timer with a fixed interval, based on the switching carrier frequency. Therefore, it is desired to maintain this structure without creating complementary high−side PWM signals. The capacitance of V_{DD} should be sufficient to supply necessary charge to V_{BS} capacitance in all three phases. If a normal PWM operation starts before V_{BS} reaches V_{UVLO} reset level, the high−side IGBTs cannot switch without creating a fault signal. It may lead to a failure of motor start in some applications. If three phases are charged synchronously, initial charging current through a single shunt resistor may exceed the over−current protection level. Therefore, initial charging time for bootstrap capacitors should be separated, as shown in Figure 32. The effect of the bootstrap capacitance factor and charging method (low−side IGBT driving method) is shown in Figure 33.

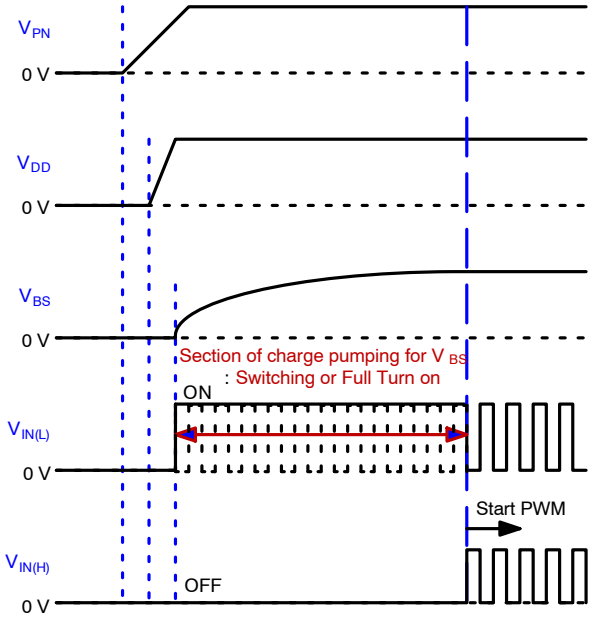


Figure 31. Timing Chart of Initial Bootstrap Charging

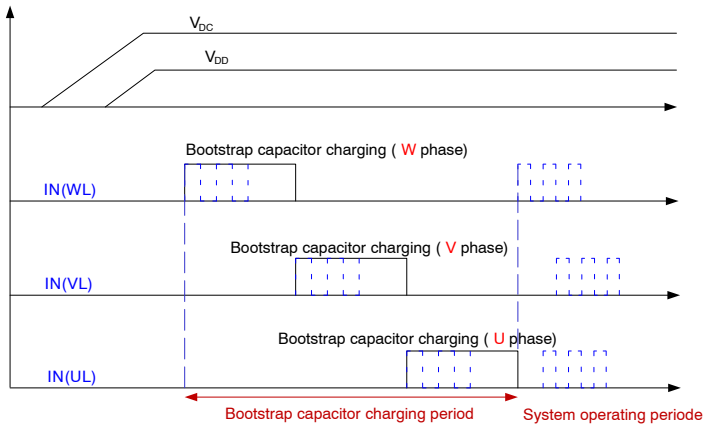


Figure 32. Recommended Initial Bootstrap Capacitors Charging Sequence

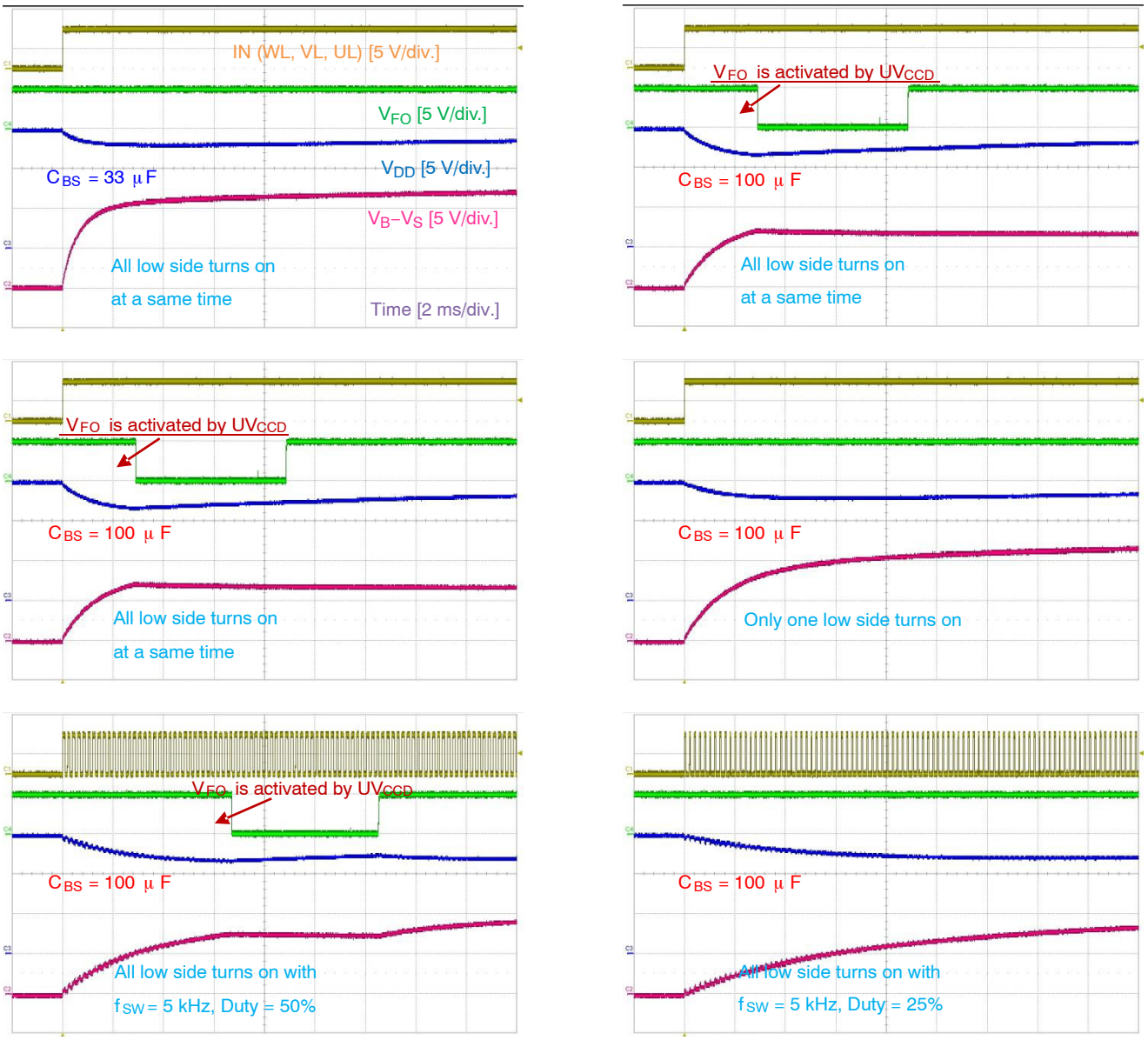


Figure 33. Initial Charging According to Bootstrap Capacitance and Charging Method (Ref. Condition: V_{DD} = 15 V/300 mA, V_{DD} Capacitor = 220 μF, Bootstrap Capacitor = 100 μF, R_{BS} = 20 Ω)

Selection of Bootstrap Capacitor Considering Operating

The bootstrap capacitance can be calculated by

$$C_{BS} = \frac{I_{leak} \times \Delta t}{\Delta V_{BS}} \quad \text{(eq. 9)}$$

Where:

Δt: maximum on pulse width of high−side IGBT;

ΔV_{BS}: the allowable discharge voltage of the C_{BS} (voltage ripple)

I_{Leak}: maximum discharge current of the CBS.

Mainly via the following mechanisms:

- Gate charge for turning the high−side IGBT on
- Quiescent current to the high−side circuit in HVIC
- Level−shift charge required by level−shifters in HVIC
- Leakage current in the bootstrap diode
- C_{BS} capacitor leakage current (ignored for non−electrolytic capacitors)
- Bootstrap diode reverse recovery charge

Practically, 12.0 mA of I_{Leak} is recommended for the 1200 V ASPM34 family. By considering dispersion and reliability, the capacitance is generally selected to be 2~3 times the calculated one. The C_{BS} is only charged when the high−side IGBT is off and the $V_{S(x)}$ voltage is pulled down to ground.

The on−time of the low−side IGBT must be sufficient to for the charge drawn from the CBS capacitor to be fully replenished. This creates an inherent minimum on−time of the low−side IGBT (or off−time of the high−side IGBT).

Calculation Example of Bootstrap Capacitance A

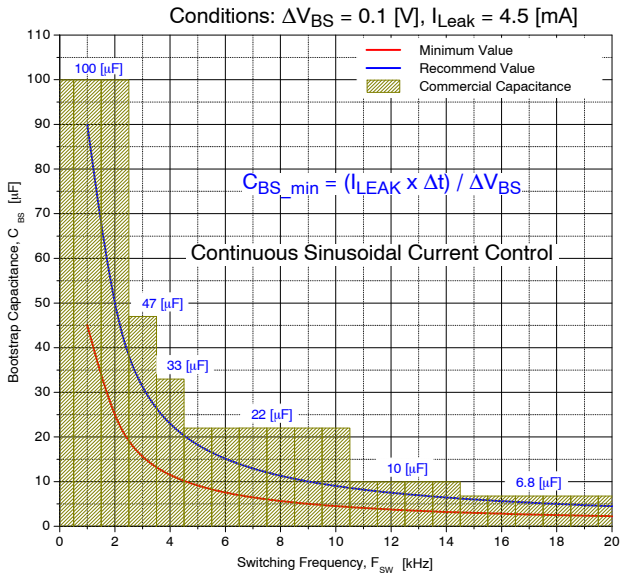


Figure 34. Capacitance of Bootstrap Capacitor on Variation of Switching Frequency

Based on switching frequency and recommended ΔV_{BS}

- I_{Leak}: circuit current = 12.0 mA (Refer to the Table 20)
- ΔVBS: discharged voltage = 0.1 V (recommended value)
- Δt: maximum on pulse width of high−side IGBT = 0.2 ms (depends on application)

$$C_{BS\_min} = \frac{I_{leak} \times \Delta t}{\Delta V_{BS}} = \frac{4.5\ mA \times 0.2\ ms}{0.1\ V} = 19 \times 10^{-6} \quad \text{(eq. 10)}$$

→ More than 2 times → 18 μF (22 μF STD value)

Table 20. OPERATING V_{BS} SUPPLY CURRENT

Symbol	Conditions	Device	Max	Unit
IPBS	V_{DD} = V_{BS} = 15 V, f_{PWM} = 20 kHz, Duty = 50%, Applied to one PWM Signal Input for High−Side	NFVA23512NP2T	12.0	mA

39. The capacitance value can be changed according to the switching frequency, the capacitor selected, and the recommended V_{BS} voltage of 13.0~18.5 V (from datasheet). The above result is just a calculation example. This value can be changed according to the actual control method and lifetime of the component.

Calculation Example of Bootstrap Capacitance B

Based on operating conditions, UVBS function, and allowable recommended $V_{B(x)}-V_{S(x)}$.

To avoid unexpected under−voltage protection and to keep V_{BS} within recommended value, bootstrap capacitance should be selected based on the operating conditions. Bootstrap voltage ripple is influenced by bootstrap resistor, load condition, output frequency, and switching frequency. Check the bootstrap voltage under the maximum load condition in the system. Figure 35 shows example of $V_{B(x)}-V_{S(x)}$ ripple voltage during operation.

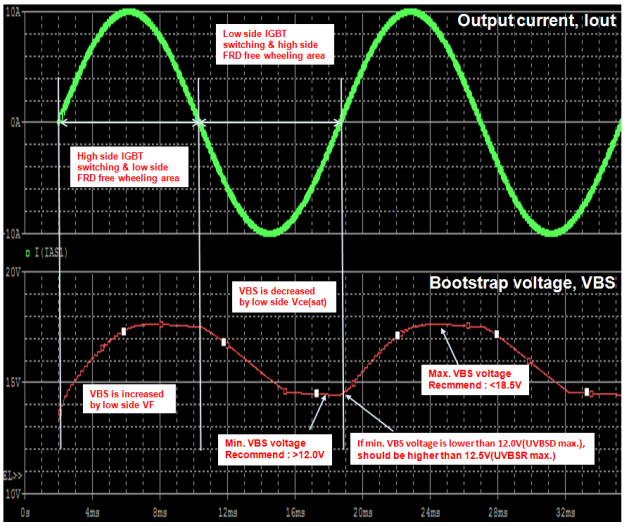


Figure 35. Recommendation of Bootstrap Ripple Voltage during Operation

Built−in Bootstrap Diode

When the high−side IGBT or FRD conducts, the bootstrap diode (D_{BS}) supports the entire bus voltage. A withstand voltage of more than 1200 V is recommended for the bootstrap diode. It is important that this diode should be fast recovery (recovery time < 100 ns) to minimize the amount of charge fed back from the bootstrap capacitor into the V_{DD} supply. Normally, bootstrap circuit consists of bootstrap diode (D_{BS}), bootstrap resistor (R_{BS}), and bootstrap capacitor (C_{BS}). I−V characteristics of 1200 V ASPM34 bootstrap diode are shown in Figure 36 and Figure 37. The bootstrap resistor (R_{BS}) slows down the dV_{BS}/dt and limits initial charging current (I_{charge}) of bootstrap capacitor. To prevent large inrush current at initial bootstrap capacitor charging, an additional series resistor should be used for current limitation. Large inrush current can result in over−current protection and stress of bootstrap diode. Guaranteed pulse current of bootstrap diode is limited by 2 A; therefore, minimum 10 Ω series resistor should be used for the current limitation. Generally, tens of Ω is recommended as R_{BS}. For the selection of R_{BS}, pulse power rating should be considered for initial charging of bootstrap capacitor. To use a large bootstrap capacitor, high pulse power rating is required for the bootstrap resistor. An example of resistor pulse power rating is shown in Figure 38.

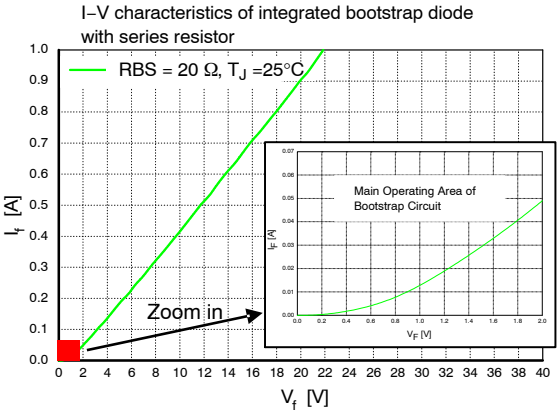


Figure 36. I–V Characteristics of Integrated Bootstrap Diode Series with Series Resistor

The characteristics of 1200 V ASPM34 bootstrap diode are:

- Fast recovery diode: 1200 V/1 A
- trr: 80 ns (typical)

Table 21. SPECIFICATION FOR BOOTSTRAP DIODE

Symbol	Parameter	Conditions	Typ	Unit
V_F	Forward−Drop Voltage	I_F = 1A, T_C = 25°C	2.2	V
t_{rr}	Reverse−Recovery Time	I_F = 1 A, T_C = 25°C, dI_F/dt = 50 A/μs	80	ns

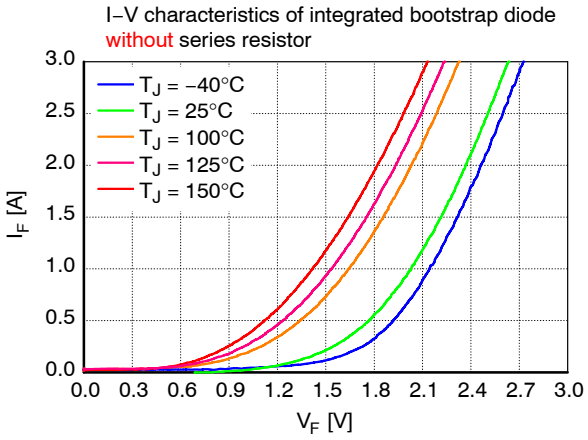


Figure 37. I–V Characteristics of Integrated Bootstrap Diode Series without Series Resistor

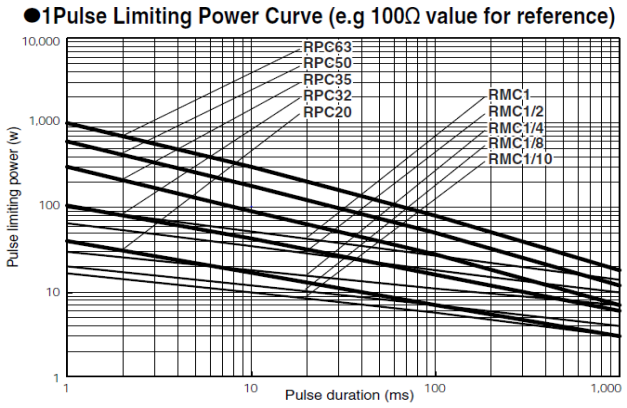


Figure 38. Example of Pulse Power Curve of Resistor (from KAMAYA OHM)

Circuit of NTC Thermistor (Temperature Monitoring of Module)

1200 V ASPM34 series include a Negative Temperature Coefficient (NTC) thermistor for temperature sensing inside the module. This thermistor is located in the DBC substrate with the power chip (IGBT/FRD) and accurately reports the temperature of the power chip (see Figure 39 and Figure 40.). Normally, circuit designers use two kinds of circuit for temperature protection (monitoring) by NTC thermistor. One is circuit by Analog−Digital Converter (ADC). The other is circuit by comparator. Figure 42 and Figure 43 show examples of both circuits for NTC thermistor.

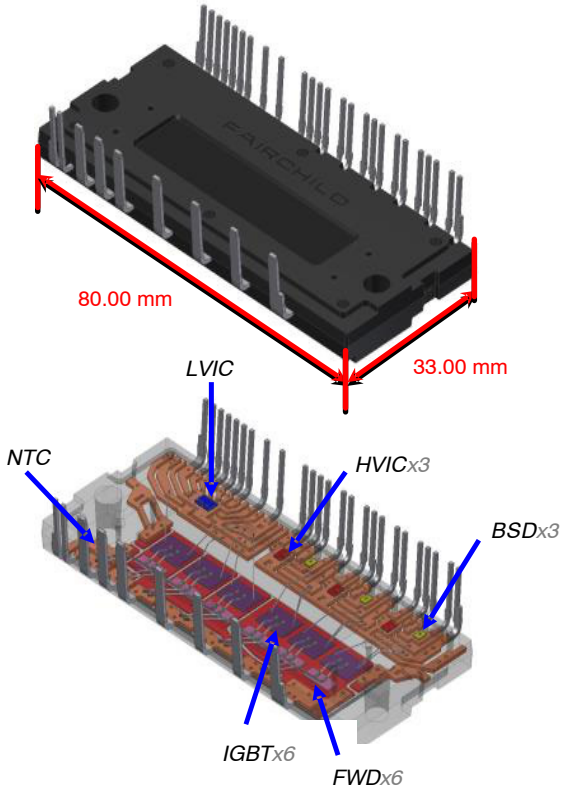


Figure 39. 1200 V ASPM34

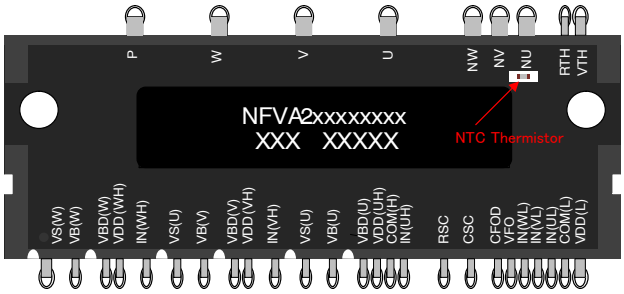


Figure 40. Location of NTC Thermistor in 1200 V ASPM34

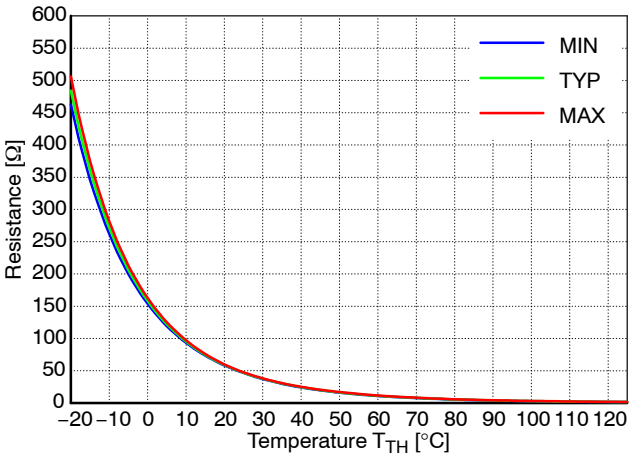


Figure 41. R−T Curve of NTC Thermistor

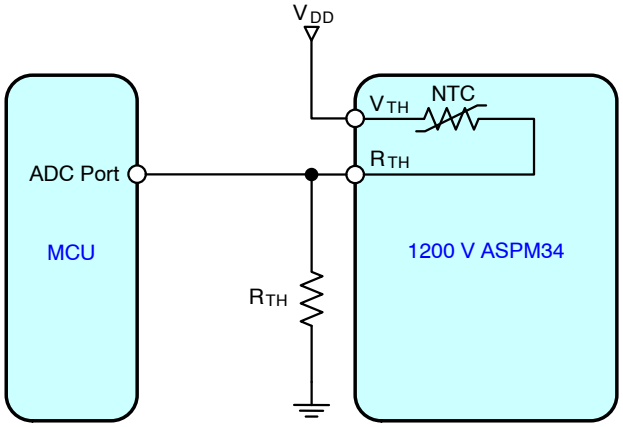


Figure 42. OT Protection Circuit by MCU

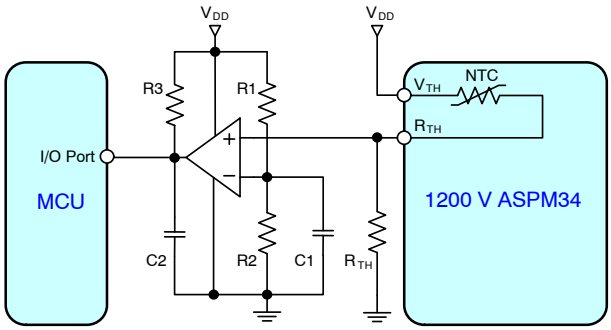


Figure 43. OT Protection Circuit by Comparator

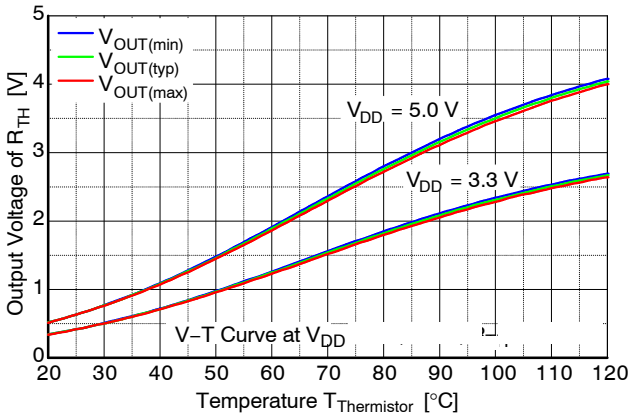


Figure 44. V−T Curve of Figure 42

Table 22. R−T TABLE OF NTC THERMISTOR

T_{NTC} (°C)	R_{min} (kΩ)	R_{cent} (kΩ)	R_{max} (kΩ)	T_{NTC} (°C)	R_{min} (kΩ)	R_{cent} (kΩ)	R_{max} (kΩ)
0	153.8063	158.2144	162.7327	61	10.4594	10.8007	11.1520
1	146.0956	150.1651	154.3326	62	10.0746	10.4091	10.7536
2	138.8168	142.5725	146.4152	63	9.7058	10.0336	10.3714
3	131.9431	135.4081	138.9502	64	9.3522	9.6734	10.0046
4	125.4497	128.6453	131.9091	65	9.0133	9.3279	9.6525
5	119.3135	122.2594	125.2655	66	8.6882	8.9963	9.3145
6	113.5129	116.2273	118.9947	67	8.3764	8.6782	8.9899
7	108.0276	110.5275	113.0739	68	8.0773	8.3727	8.6782
8	102.8388	105.1398	107.4814	69	7.7902	8.0795	8.3787
9	97.9288	100.0454	102.1974	70	7.5147	7.7979	8.0910
10	93.2812	95.2267	97.2031	71	7.2496	7.5268	7.8138
11	88.8803	90.6673	92.4810	72	6.9950	7.2663	7.5474
12	84.7119	86.3519	88.0148	73	6.7505	7.0160	7.2913
13	80.7624	82.2661	83.7894	74	6.5157	6.7755	7.0450
14	77.0190	78.3963	79.7903	75	6.2901	6.5443	6.8082
15	73.4700	74.7302	76.0043	76	6.0739	6.3227	6.5810
16	70.1042	71.2558	72.4189	77	5.8662	6.1096	6.3624
17	66.9112	67.9620	69.0224	78	5.6665	5.9046	6.1521
18	63.8812	64.8386	65.8039	79	5.4745	5.7075	5.9498
19	61.0050	61.8759	62.7530	80	5.2899	5.5178	5.7549
20	58.2739	59.0647	59.8601	81	5.1129	5.3358	5.5680
21	55.6798	56.3961	57.1160	82	4.9426	5.1607	5.3879
22	53.2152	53.8628	54.5127	83	4.7788	4.9921	5.2145
23	50.8732	51.4569	52.0422	84	4.6211	4.8299	5.0475
24	48.6469	49.1715	49.6969	85	4.4694	4.6736	4.8866
25	46.5300	47.0000	47.4700	86	4.3228	4.5226	4.7310
26	44.4567	44.9360	45.4159	87	4.1817	4.3771	4.5811
27	42.4868	42.9737	43.4618	88	4.0459	4.2369	4.4366
28	40.6147	41.1075	41.6021	89	3.9150	4.1019	4.2973
29	38.8351	39.3323	39.8319	90	3.7890	3.9717	4.1629
30	37.1428	37.6431	38.1463	91	3.6675	3.8463	4.0334
31	35.5329	36.0351	36.5408	92	3.5505	3.7253	3.9084
32	34.0011	34.5041	35.0111	93	3.4377	3.6087	3.7879
33	32.5433	33.0462	33.5534	94	3.3290	3.4963	3.6716
34	31.1555	31.6573	32.1640	95	3.2242	3.3878	3.5593
35	29.8340	30.3339	30.8392	96	3.1235	3.2836	3.4515
36	28.5760	29.0734	29.5764	97	3.0264	3.1830	3.3473
37	27.3776	27.8717	28.3720	98	2.9328	3.0860	3.2468
38	26.2356	26.7260	27.2228	99	2.8425	2.9923	3.1497
39	25.1472	25.6332	26.1261	100	2.7553	2.9019	3.0559
40	24.1094	24.5907	25.0792	101	2.6712	2.8146	2.9654
41	23.1198	23.5960	24.0796	102	2.5901	2.7303	2.8779

Table 22. R−T TABLE OF NTC THERMISTOR (continued)

T_{NTC} (°C)	R_{min} (kΩ)	R_{cent} (kΩ)	R_{max} (kΩ)	T_{NTC} (°C)	R_{min} (kΩ)	R_{cent} (kΩ)	R_{max} (kΩ)
42	22.1759	22.6466	23.1249	103	2.5117	2.6489	2.7933
43	21.2753	21.7401	22.2129	104	2.4360	2.5703	2.7117
44	20.4158	20.8746	21.3416	105	2.3630	2.4943	2.6327
45	19.5953	20.0478	20.5088	106	2.2921	2.4206	2.5560
46	18.8120	19.2580	19.7126	107	2.2236	2.3493	2.4819
47	18.0638	18.5032	18.9514	108	2.1575	2.2805	2.4102
48	17.3492	17.7818	18.2234	109	2.0936	2.2139	2.3409
49	16.6663	17.0921	17.5269	110	2.0319	2.1496	2.2739
50	16.0137	16.4325	16.8605	111	1.9725	2.0877	2.2094
51	15.3899	15.8016	16.2227	112	1.9151	2.0278	2.1470
52	14.7934	15.1981	15.6122	113	1.8596	1.9699	2.0866
53	14.2230	14.6205	15.0277	114	1.8060	1.9139	2.0282
54	13.6773	14.0677	14.4678	115	1.7541	1.8598	1.9716
55	13.1552	13.5385	13.9316	116	1.7042	1.8076	1.9171
56	12.6556	13.0318	13.4178	117	1.6559	1.7572	1.8644
57	12.1774	12.5465	12.9255	118	1.6092	1.7083	1.8134
58	11.7195	12.0815	12.4536	119	1.564	1.6611	1.7639
59	11.2810	11.6361	12.0011	120	1.5203	1.6153	1.7161
60	10.8610	11.2091	11.5673				

PRINT CIRCUIT BOARD (PCB) DESIGN

General Application Circuit Example

Figure 45 shows a general application circuitry of interface schematic with control signals connected directly to a MCU. Figure 45 shows guidance of PCB layout for the 1200 V ASPM34 series.

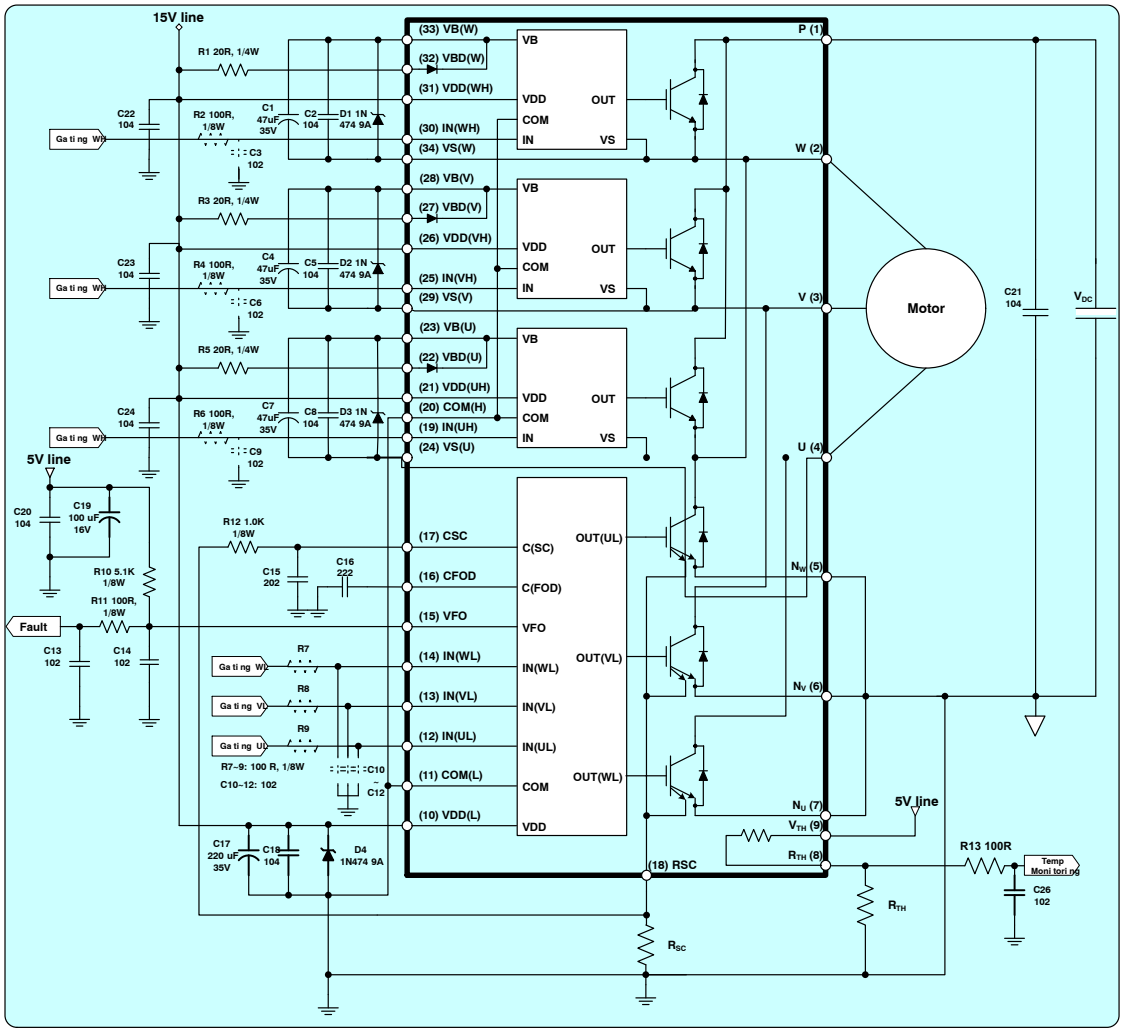


Figure 45. General Application Circuitry for the 1200 V ASPM34 Series

PCB Layout Guidance

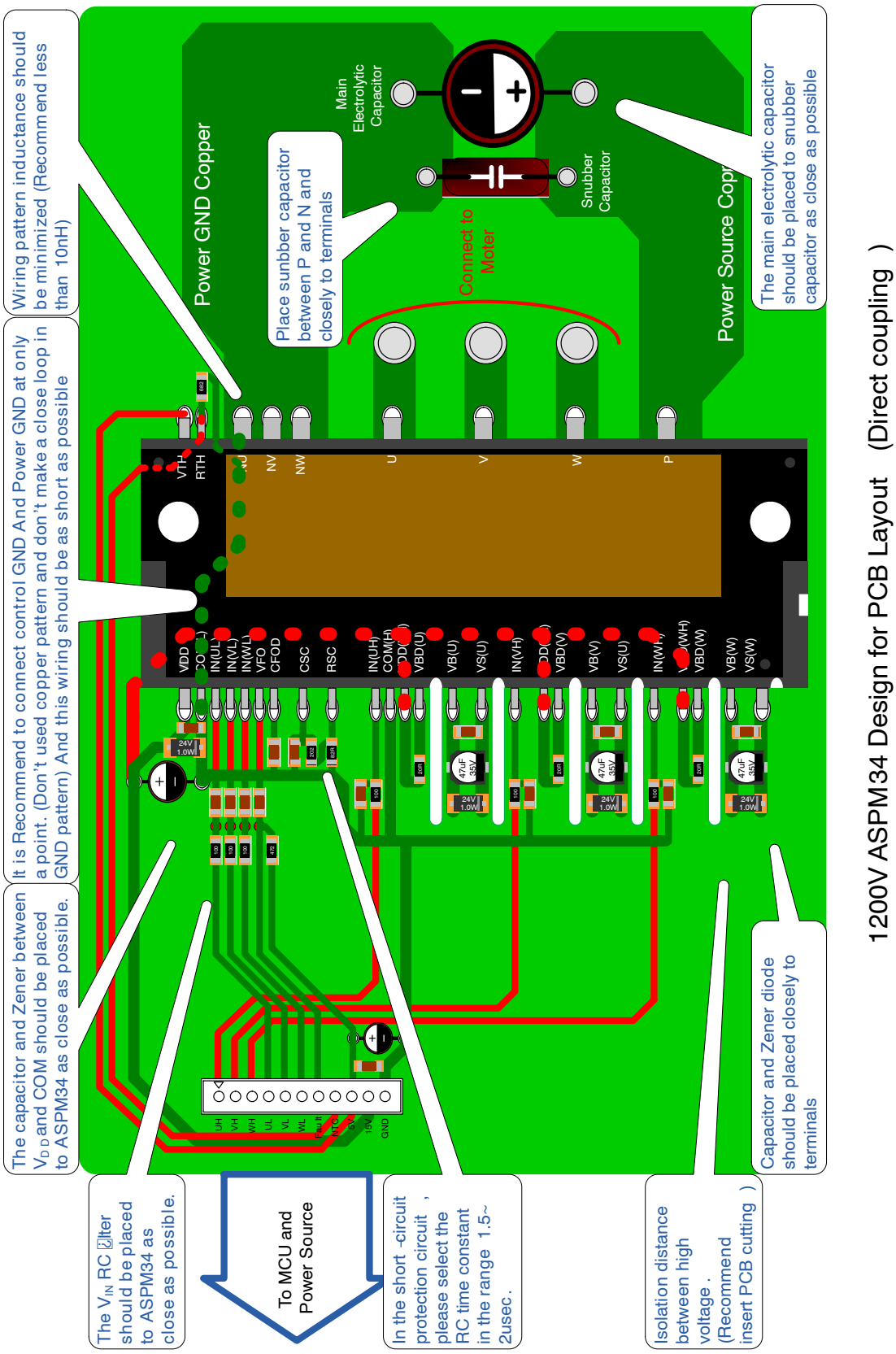


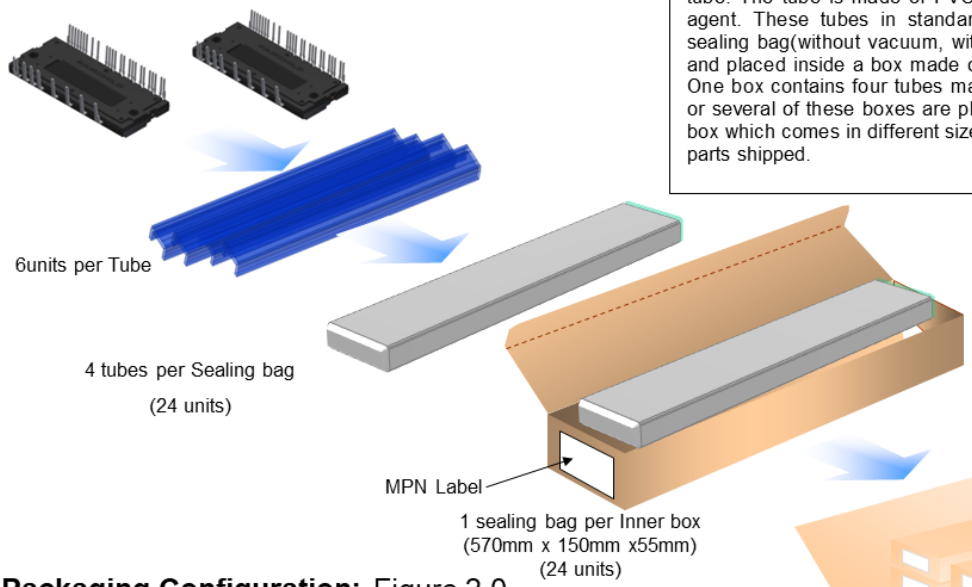
Figure 46. Print Circuit Board (PCB) Layout Guidance for the 1200 V ASPM34

PACKING INFORMATION

SPM34/ASPM34 Series Tube Packing Configuration: Figure 1.0

Packaging Description:

SPM34 and ASPM34 Series parts are shipped normally in tube. The tube is made of PVC plastic treated with anti-static agent. These tubes in standard option are placed inside a sealing bag(without vacuum, with desiccant), barcode labeled, and placed inside a box made of recyclable corrugated paper. One box contains four tubes maximum (see fig. 1.0). And one or several of these boxes are placed inside a labeled shipping box which comes in different sizes depending on the number of parts shipped.

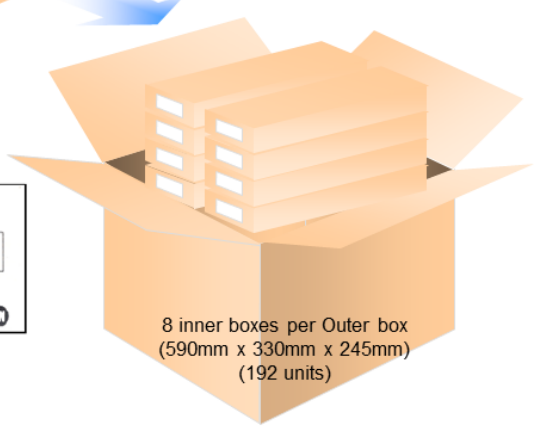


Packaging Configuration: Figure 2.0

Packaging Information	
Packaging Option	Standard (no flow code)
Packaging type	Rail/Tube
Qty per Tube/ Inner Box	6
Inner Box Dimension (mm)	570x150x55
Max qty per Box	24
Outer Box Dimension (mm)	590x330x245
Max qty per Box	192
Weight per unit (gm)	-
Note/Comments	

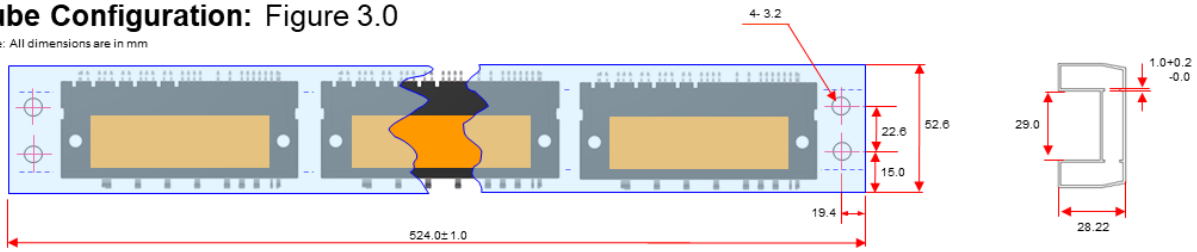
Inner Box Barcode Label Sample

Sample MPN Label



Tube Configuration: Figure 3.0

Note: All dimensions are in mm



NOTES:

A : ALL DIMENSION ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED

ON Semiconductor

Figure 47. Packing Information

RELATED RESOURCES

FAM65V05DF1 Product Folder
NFVA33065L32, NFVA34065L32, NFVA35065L32 Product Folder
AN−9086 − 600 V SPM®3 Series Mounting Guidance

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