MJ15022 (NPN), MJ15024 (NPN)

Silicon Power Transistors

The MJ15022 and MJ15024 are power transistors designed for high power audio, disk head positioners and other linear applications.

Features

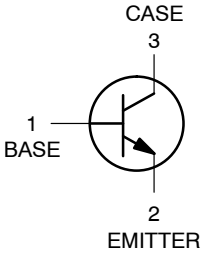
- High Safe Operating Area
- High DC Current Gain
- These Devices are Pb−Free and are RoHS Compliant*
- Complementary to MJ15023 (PNP), MJ15025 (PNP)

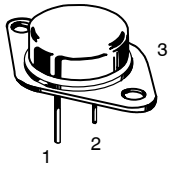
ON Semiconductor®

http://onsemi.com

16 AMPERES
SILICON POWER TRANSISTORS
200 – 250 VOLTS, 250 WATTS

SCHEMATIC





TO−204AA (TO−3)
CASE 1−07
STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage MJ15022 MJ15024	V_{CEO}	 200 250	Vdc
Collector−Base Voltage MJ15022 MJ15024	V_{CBO}	 350 400	Vdc
Emitter−Base Voltage	V_{EBO}	5	Vdc
Collector−Emitter Voltage	V_{CEX}	400	Vdc
Collector Current − Continuous	I_C	16	Adc
Collector Current − Peak (Note 1)	I_{CM}	30	Adc
Base Current − Continuous	I_B	5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

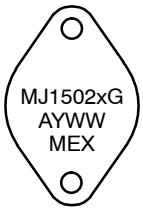
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	0.70	°C/W

MARKING DIAGRAM



MJ1502x = Device Code
x = 2 or 4
G = Pb−Free Package
A = Assembly Location
Y = Year
WW = Work Week
MEX = Country of Origin

ORDERING INFORMATION

Device	Package	Shipping
MJ15022G	TO−204 (Pb−Free)	100 Units / Tray
MJ15024G	TO−204 (Pb−Free)	100 Units / Tray

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 2) (I_C = 100 mAdc, I_B = 0)	 MJ15022 MJ15024	$V_{CEO(sus)}$	 200 250	 − −	−
Collector Cutoff Current (V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	 MJ15022 MJ15024	I_{CEX}	 − −	 250 250	μAdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 200 vdc, I_B = 0)	 MJ15022 MJ15024	I_{CEO}	 − −	 500 500	μAdc
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_B = 0)		I_{EBO}	−	500	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 0.5 s (non−repetitive)) (V_{CE} = 80 Vdc, t = 0.5 s (non−repetitive))		$I_{S/b}$	 5 2	 − −	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 8 Adc, V_{CE} = 4 Vdc) (I_C = 16 Adc, V_{CE} = 4 Vdc)		h_{FE}	 15 5	 60 −	−
Collector−Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc) (I_C = 16 Adc, I_B = 3.2 Adc)		$V_{CE(sat)}$	 − −	 1.4 4.0	Vdc
Base−Emitter On Voltage (I_C = 8 Adc, V_{CE} = 4 Vdc)		$V_{BE(on)}$	−	2.2	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain − Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	4	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)		C_{ob}	−	500	pF

2. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

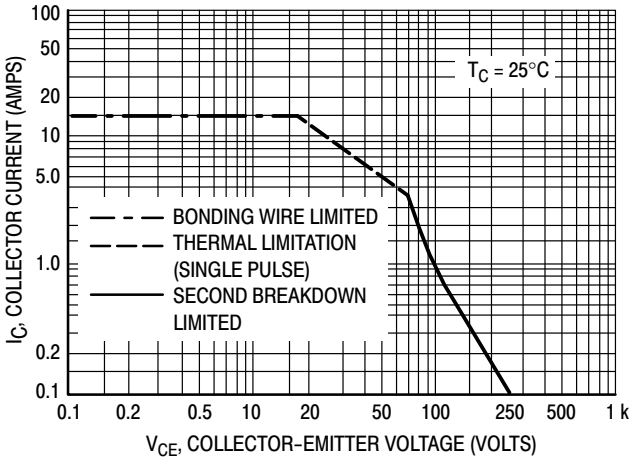


Figure 1. Active−Region Safe Operating Area

There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values Ion than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

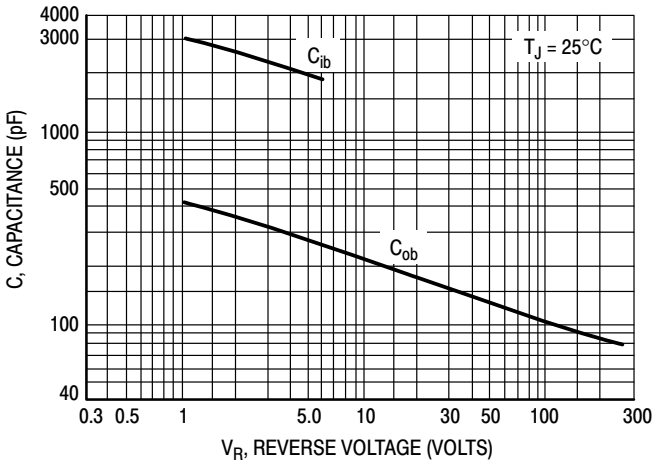


Figure 2. Capacitances

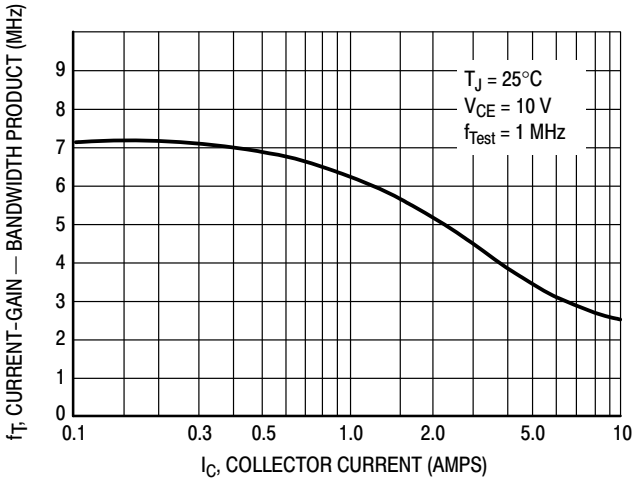


Figure 3. Current−Gain — Bandwidth Product

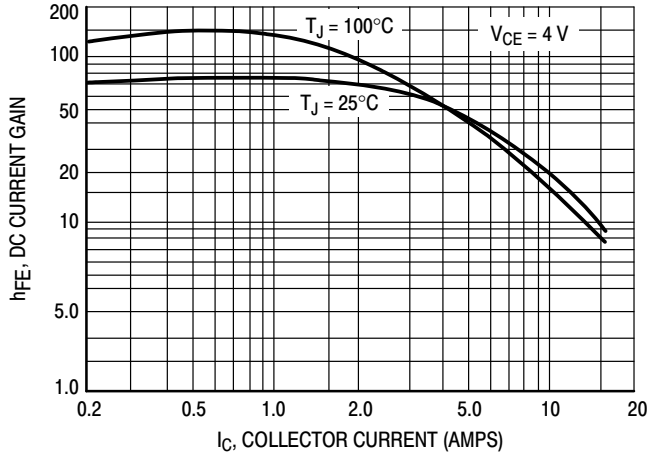


Figure 4. DC Current Gain

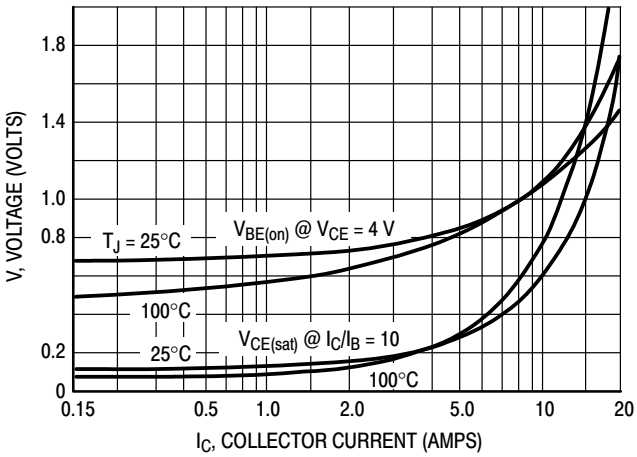


Figure 5. “On” Voltage

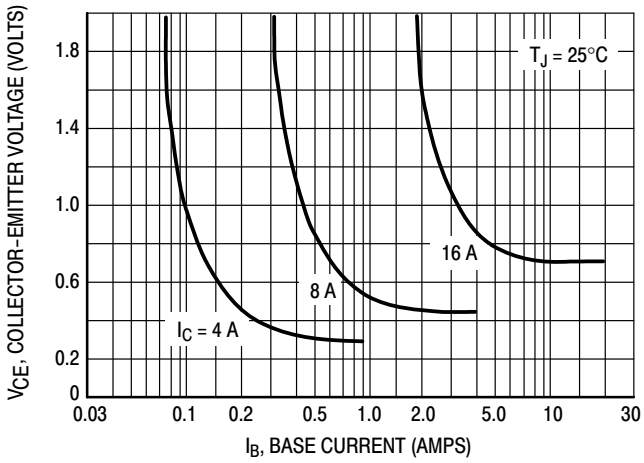
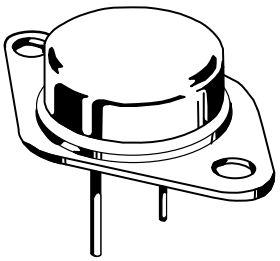


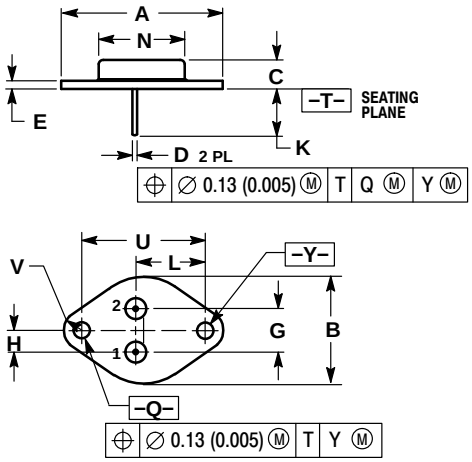
Figure 6. Collector Saturation Region



SCALE 1:1

TO−204 (TO−3)
CASE 1−07
ISSUE Z

DATE 05/18/1988



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO−204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE: EMITTER

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE: DRAIN

STYLE 4:
PIN 1. GROUND
2. INPUT
CASE: OUTPUT

STYLE 5:
PIN 1. CATHODE
2. EXTERNAL TRIP/DELAY
CASE: ANODE

STYLE 6:
PIN 1. GATE
2. EMITTER
CASE: COLLECTOR

STYLE 7:
PIN 1. ANODE
2. OPEN
CASE: CATHODE

STYLE 8:
PIN 1. CATHODE #1
2. CATHODE #2
CASE: ANODE

STYLE 9:
PIN 1. ANODE #1
2. ANODE #2
CASE: CATHODE

ADDITIONAL INFORMATION

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