

CAT310

LED Driver, 10-Channel

Description

The CAT310 is a 10-channel LED driver for automotive and other lighting applications. All LED output channels are driven from a low on-resistance open-drain High Voltage CMOS Nch-FETs and are fully compliant with “Load Dump” transients of up to 40 volts. The LED bias current of each channel can be set independently using an external series ballast resistor, making the device ideal for multi-color instrumentation displays.

A high-speed serial interface (suitable with both 3.3 volt and 5 volt systems) feeding a 10 bit shift register is used to program the desired state (on/off) of each channel. The device offers a blanking control pin (BLANK) which can be used to disable all channels on demand. A serial output data pin (SOUT) is provided to daisy-chain devices in large cluster LED applications.

During initial power up all channels are reset and cleared via an under-voltage lock out (UVLO) detector and for added protection all channels are disabled in the event of a battery over-voltage condition (19 volts or more).

Features

- Automotive “Load Dump” Protection (40 V)
- 10 Independent LED Channels
- Up to 50 mA Output per Channel
- Overvoltage Detection at 19 V
- Serial Interface for Channel Programming
- Daisy Chain Output for Multi-driver Cascading
- LED Blanking Control
- Operating Temperature from -40°C to $+125^{\circ}\text{C}$
- 20-pin SOIC Package
- This Device is Pb-Free, Halogen Free/BFR Free and RoHS Compliant

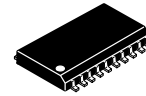
Applications

- Automotive Lighting
- White and Other Color High Brightness LEDs
- Multi-color High-brightness LED Cluster Displays
- General LED Lighting



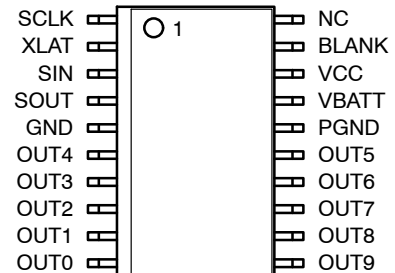
ON Semiconductor®

<http://onsemi.com>

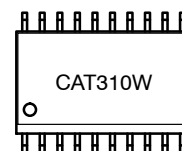


SOIC-20
W SUFFIX
CASE 751BJ

PIN CONNECTIONS



MARKING DIAGRAM



CAT310W = Specific Device Code

ORDERING INFORMATION

| Device | Package | Shipping |
|---------|----------------------|-------------------|
| CAT310W | SOIC-20 (Pb-Free) | 1,000/Tape & Reel |

CAT310

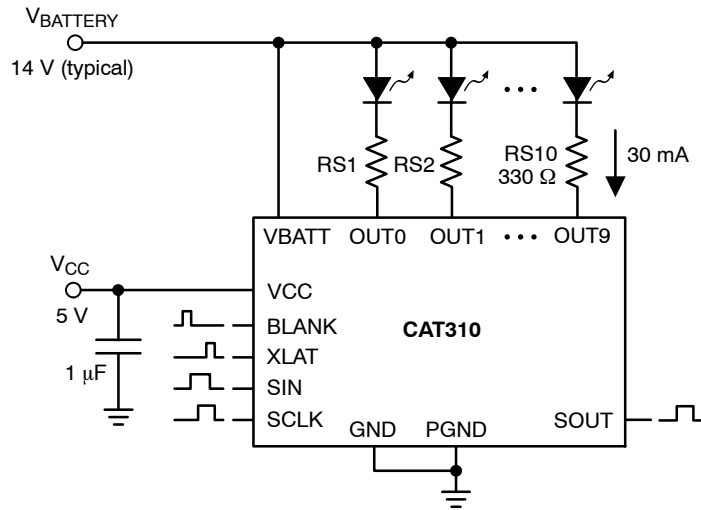


Figure 1. Typical Application Circuit

Table 1. ABSOLUTE MAXIMUM RATINGS

| Parameter | Rating | Unit |
|--|-----------------------|------|
| VCC voltage | 7 | V |
| Input voltage range (SIN, SCLK, BLANK, XLAT) | -0.3 V to VCC + 0.3 V | V |
| SOUT voltage range | -0.3 V to VCC + 0.3 V | V |
| Peak OUT0 to OUT9 voltage | 40 | V |
| VBATT input voltage | 40 | V |
| DC output current on OUT0 to OUT9 | 70 | mA |
| Storage Temperature Range | -55 to +160 | °C |
| Operating Junction Temperature Range | -40 to +150 | °C |
| Lead Soldering Temperature (10 sec.) | 300 | °C |
| ESD Rating: Low Voltage Pins | | V |
| Human Body Model | 3000 | |
| Machine Model | 300 | |
| ESD Rating: VBATT, OUT[0:9] pins | | V |
| Human Body Model | 1000 | |
| Machine Model | 100 | |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 2. RECOMMENDED OPERATING CONDITIONS

| Parameter | Range | Unit |
|---------------------------------|-------------|------|
| VCC | 3.0 to 5.5 | V |
| Voltage applied to OUT0 to OUT9 | 9 to 17 | V |
| Output current on OUT0 to OUT9 | 0 to 50 | mA |
| Ambient Temperature Range | -40 to +125 | °C |

CAT310

Electrical Operating Characteristics

Table 3. DC CHARACTERISTICS

(VCC = 5.0 V, -40°C ≤ T_A ≤ 125°C, over recommended operating conditions unless specified otherwise.)

| Symbol | Name | Conditions | Min | Typ | Max | Units |
|------------------------------------|---|---|-------------------------|---------|---------------------|-------|
| I _{STBY} | Standby Quiescent Current | Static input signal. All outputs turned off. | | 1 | 10 | μA |
| V _{OVP} | VBATT Over Voltage Protection Trigger threshold | | 17 | 19 | 21 | V |
| V _{UVLO} | VCC Under Voltage Lockout Trigger threshold | | | 1.7 | 2.5 | V |
| R _{SW} | Switch on resistance for OUT0 to OUT9 | I _{O(n)} = 30 mA | 2 | 5 | 12 | Ω |
| I _{O(n)LKG} | OUT0 to OUT9 Output Switch Leakage | V _{(OUT(n))} = 15 V | | 0.1 | 10 | μA |
| I _{XLAT} | XLAT Internal Pull-down current | XLAT = V _{CC} XLAT = 0.3 V | 4 1 | 10 3 | 30 6 | μA |
| I _{BLANK} | BLANK Internal Pull-up current | BLANK = 0 V BLANK = V _{CC} - 0.3 V | 4 1 | 10 3 | 30 6 | μA |
| V _{IH} V _{IL} | Logic high input voltage Logic low input voltage | | 0.3 V _{CC} | | 0.7 V _{CC} | V |
| I _{IL} | Logic Input leakage current (SCLK, SIN) | V _I = V _{CC} or GND | -5 | 0 | 5 | μA |
| V _{OH} V _{OL} | SOUT logic high output voltage SOUT logic low output voltage | I _{OH} = -1 mA I _{OL} = 1 mA | V _{CC} - 0.3 V | | 0.3 | V |

Table 4. SWITCHING CHARACTERISTICS

(VCC = 5.0 V, -40°C ≤ T_A ≤ 125°C, over recommended operating conditions unless specified otherwise.)

| Symbol | Name | Conditions | Min | Typ | Max | Units |
|--------------------|-----------------------------|------------------------|-----|-----|-----|-------|
| SCLK | | | | | | |
| f _{SCLK} | SCLK Clock Frequency | | | | 10 | MHz |
| t _{wh/wl} | SCLK Pulse width | High or Low | 30 | | | ns |
| SIN | | | | | | |
| t _{su} | Setup time SIN to SCLK | | 10 | | | ns |
| t _h | Hold time SIN to SCLK | | 10 | | | ns |
| XLAT | | | | | | |
| t _w | XLAT Pulse width | SIN to SCLK | 20 | | | ns |
| t _h | Hold time SCLK to XLAT | | 20 | | | ns |
| t _r | SOUT rise time (10% to 90%) | C _L = 15 pF | | 20 | | ns |
| t _f | SOUT fall time (90% to 10%) | C _L = 15 pF | | 15 | | ns |
| t _{pd} | Propagation delay time | Blank ↑ to OUT(n) | | 25 | | ns |
| t _{pd} | Propagation delay time | Blank ↓ to OUT(n) | | 25 | | ns |
| t _{pd} | Propagation delay time | SCLK to SOUT | | 25 | | ns |

1. All logic inputs contain Schmitt trigger inputs.

CAT310

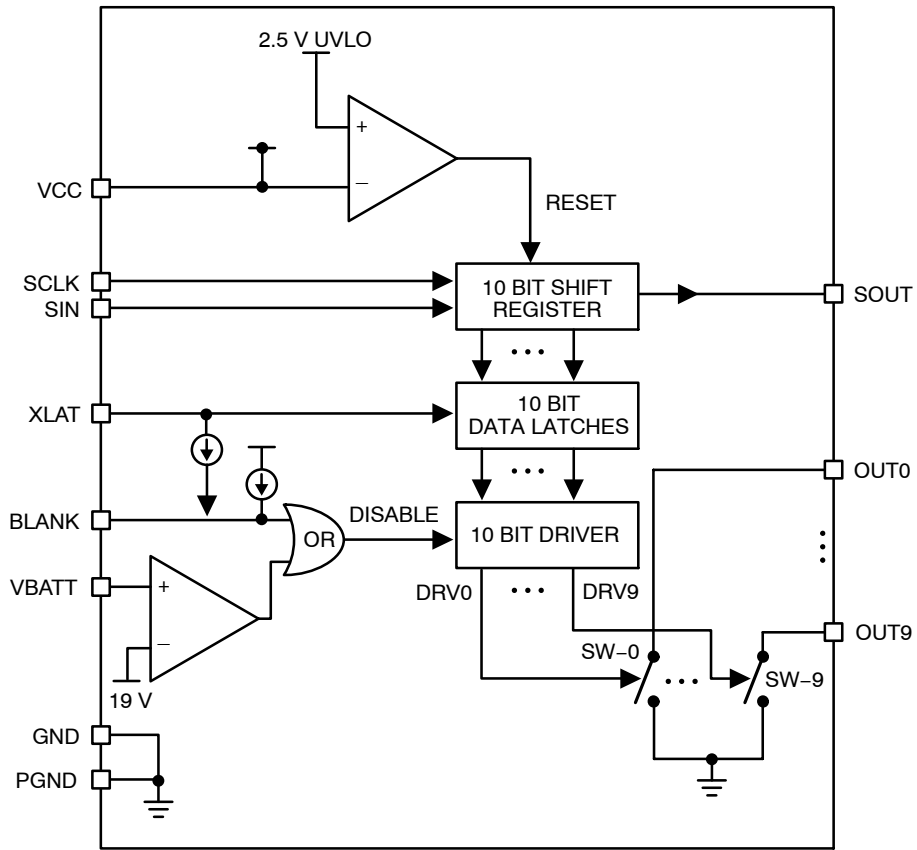


Figure 2. Block Diagram

PIN DESCRIPTIONS

VCC is the supply input for the internal logic and is compatible with both 3.3 V and 5 V systems. The logic is held in a reset state until VCC exceeds 2.5 V. It is recommended that a small bypass ceramic capacitor (1 μ F) be placed between VCC and GND pins on the device.

SIN is the CMOS logic pin for delivering the serial input data stream into the internal 10-bit shift register. The most recent or last data value in the serial stream is used to configure the state of output channel “zero” (OUT0). During the initial power up sequence all contents of the shift register are reset and cleared to zero.

SCLK is the CMOS logic pin used to clock the internal shift register. On each rising edge of clock, the serial data will advance through one stage of the shift register.

XLAT is the CMOS logic input used to transfer data from the 10-bit shift register into the output channel latches. An internal pull-down current of 10 microampere is present on this pin. When XLAT is low, the state of each output channel remains unchanged. When XLAT is driven high, the contents of the shift register appear at their respective output channels. An external pull-up resistance of 10 k Ω or less is adequate for logic high.

PGND, GND pins should be connected to the ground on the PCB.

BLANK is the CMOS logic input (active high) used to temporarily disable all outputs. An internal pull-up current of 10 microampere is present on this pin. The BLANK pin must be driven to a logic low in order for channel outputs to resume normal operation. An external pull-down resistance of 10 k Ω or less is adequate for logic low.

SOUT is the CMOS logic output used for daisy chain applications. The serial output data stream is fed from the last stage of the internal 10-bit shift register. On each rising edge of the clock, the SOUT value will be updated. The data value present on this pin is identical to the data value being used for configuring the state of output channel nine (OUT9). At initial power up, the SOUT data stream will contain all zeroes until the shift register has been fully loaded.

VBATT input monitors the battery voltage. If an over-voltage, above 19 V typical, is detected, all outputs are disabled. Upon conclusion of the over-voltage condition, all outputs resume normal operation. The current drawn by the VBATT pin is less than 1 microampere during normal operation.

OUT0-OUT9 are the ten LED outputs connected internally to the switch N-channel FETs. They sink currents up to 50 mA per channel and can withstand transients up to 40 V compatible with automotive “load dump”. The output on-resistance is 5 Ω , and the off-resistance is 5 M Ω .

Table 5. PIN TABLE

| Pin Number | Pin Name | Description/Function |
|------------|-------------|---|
| 1 | SCLK | Clock input for the data shift register. |
| 2 | XLAT | Control input for the data latch. |
| 3 | SIN | Serial data input. |
| 4 | SOUT | Serial data output. |
| 5 | GND | Ground. |
| 6-10 | OUT4 - OUT0 | Open drain outputs. |
| 11-15 | OUT9 - OUT5 | Open drain outputs. |
| 16 | PGND | Ground for LED driver outputs. |
| 17 | VBATT | Battery sense input. |
| 18 | VCC | Power supply voltage for the logic |
| 19 | BLANK | Blank input. When BLANK is high, all the output drivers are turned off. |
| 20 | N.C. | No connect. |

CAT310

TYPICAL CHARACTERISTICS

(VCC = 5 V, VBATT = 14 V, T_{AMB} = 25°C, unless otherwise specified.)

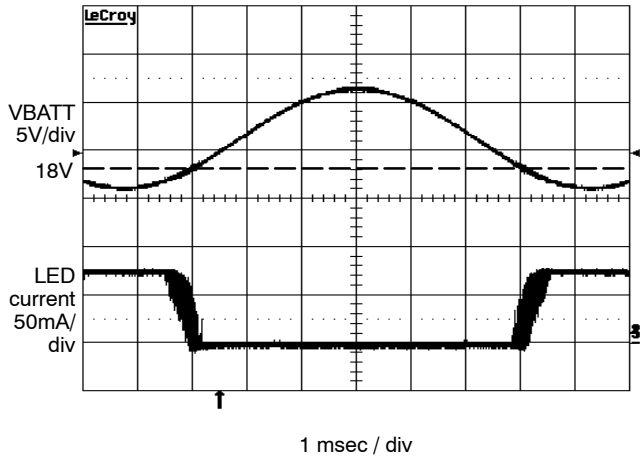


Figure 3. VBATT Overvoltage Detection Amplitude between 16 V and 26 V

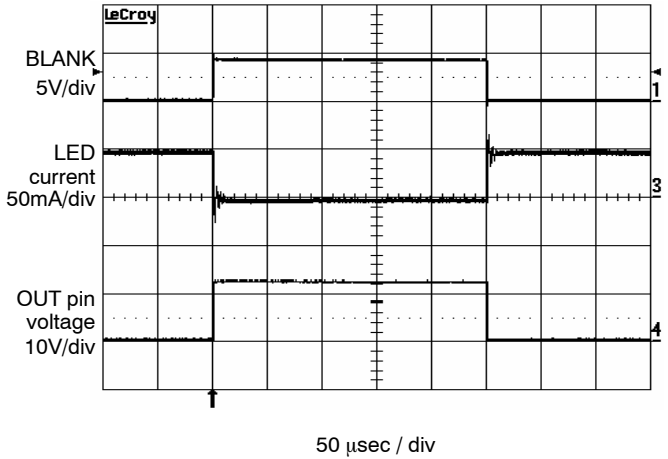


Figure 4. BLANK and Output Waveform

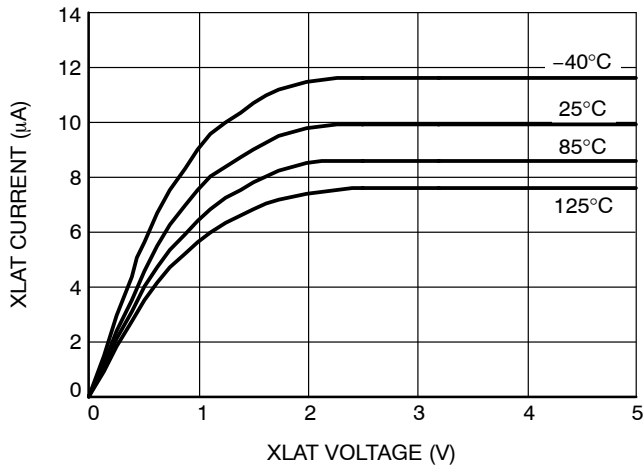


Figure 5. XLAT Pull-down Current vs. Input Voltage

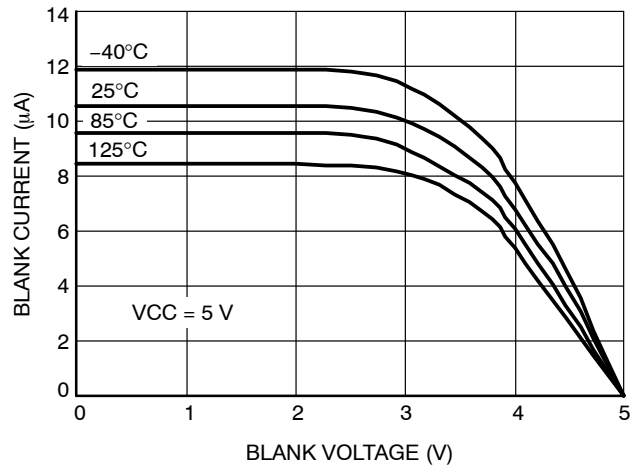


Figure 6. BLANK Pull-up Current vs. Input Voltage

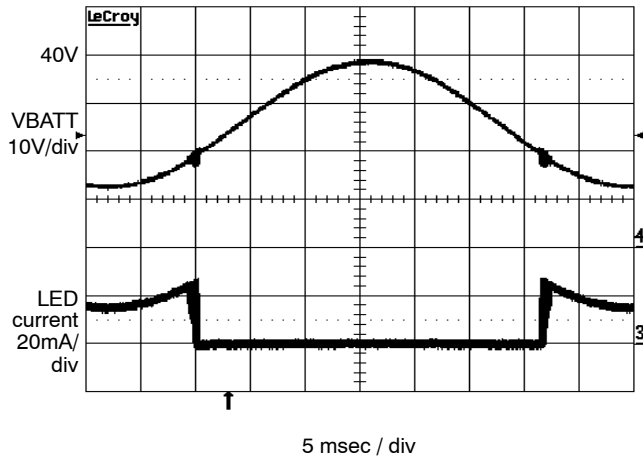


Figure 7. VBATT Load Dump

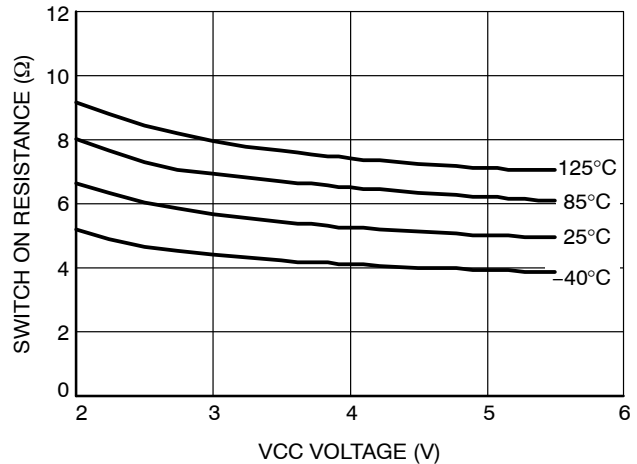


Figure 8. Switch On-resistance vs. VCC

CAT310

TYPICAL CHARACTERISTICS

(VCC = 5 V, VBATT = 14 V, T_{AMB} = 25°C, unless otherwise specified.)

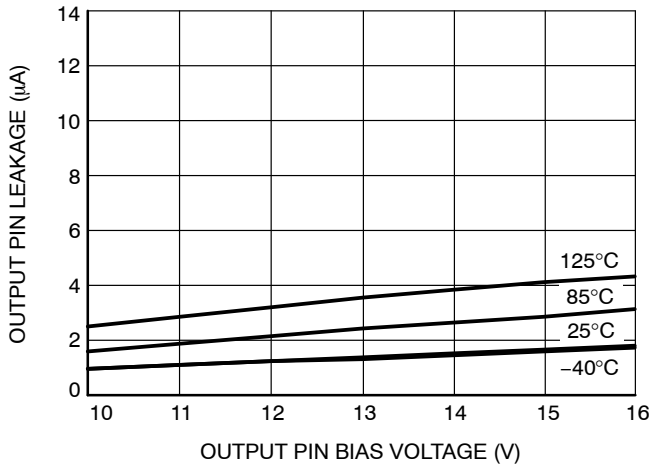


Figure 9. Output Channel Leakage vs. Bias Voltage

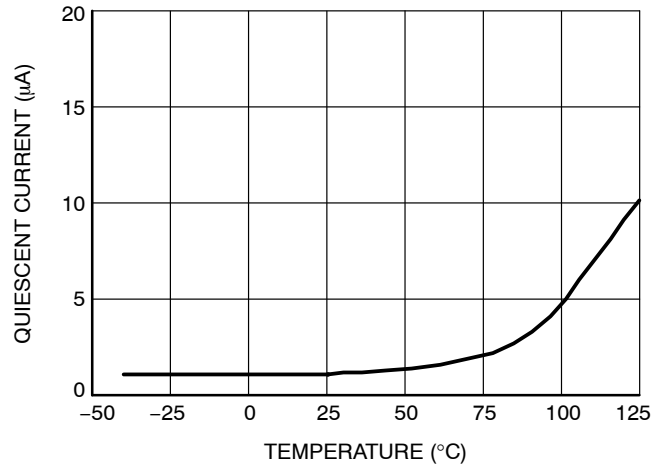


Figure 10. Quiescent Current vs. Temperature

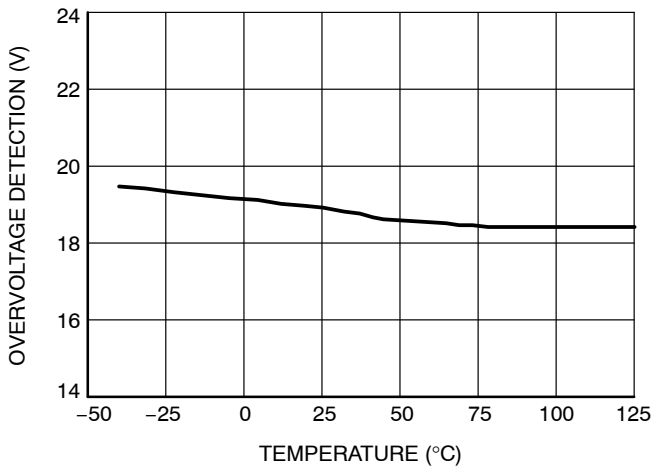


Figure 11. VBATT Overvoltage Detection vs. Temperature

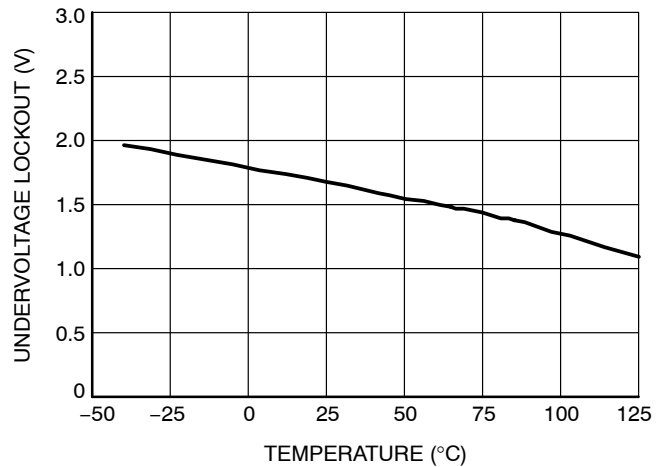


Figure 12. VCC Undervoltage Lockout vs. Temperature

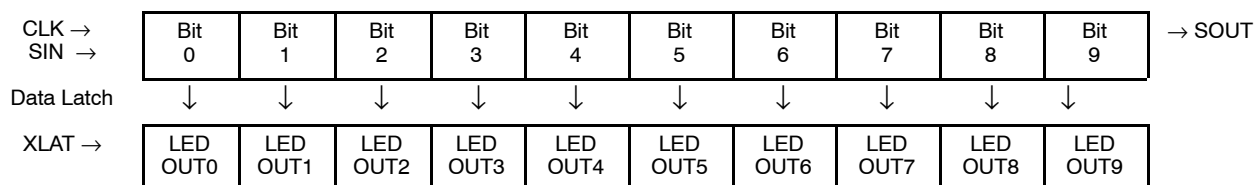
Functional Description

The CAT310 implements a 10-bit serial-in shift register for storing the setting of the ten outputs. Serial input data SIN are clocked into the shift register on the rising edge of the clock. At the 10th clock pulse, the first data bit entered is outputted from the shift register to SOUT. The following clock pulses will output the following data bits onto SOUT. The output data pattern replicates the input data stream with a delay of ten clock pulses.

The 10-bit data pattern present in the shift register is stored in the 10-bit data latch when the latch signal XLAT

is logic high. When XLAT transitions to logic low, data are latched and stay unchanged for as long as XLAT remains low. The last serial input data corresponds to OUT0. The serial input data that was received 10 clock pulse ago is stored in OUT9. When the BLANK input is logic high, all the output switches are in the off state. If the BLANK input is low, the 10-bit data latches control the 10 output switches. A data bit value of zero keeps the switch off. A data bit value of one keeps the switch on.

Serial to Parallel Shift Register



CAT310

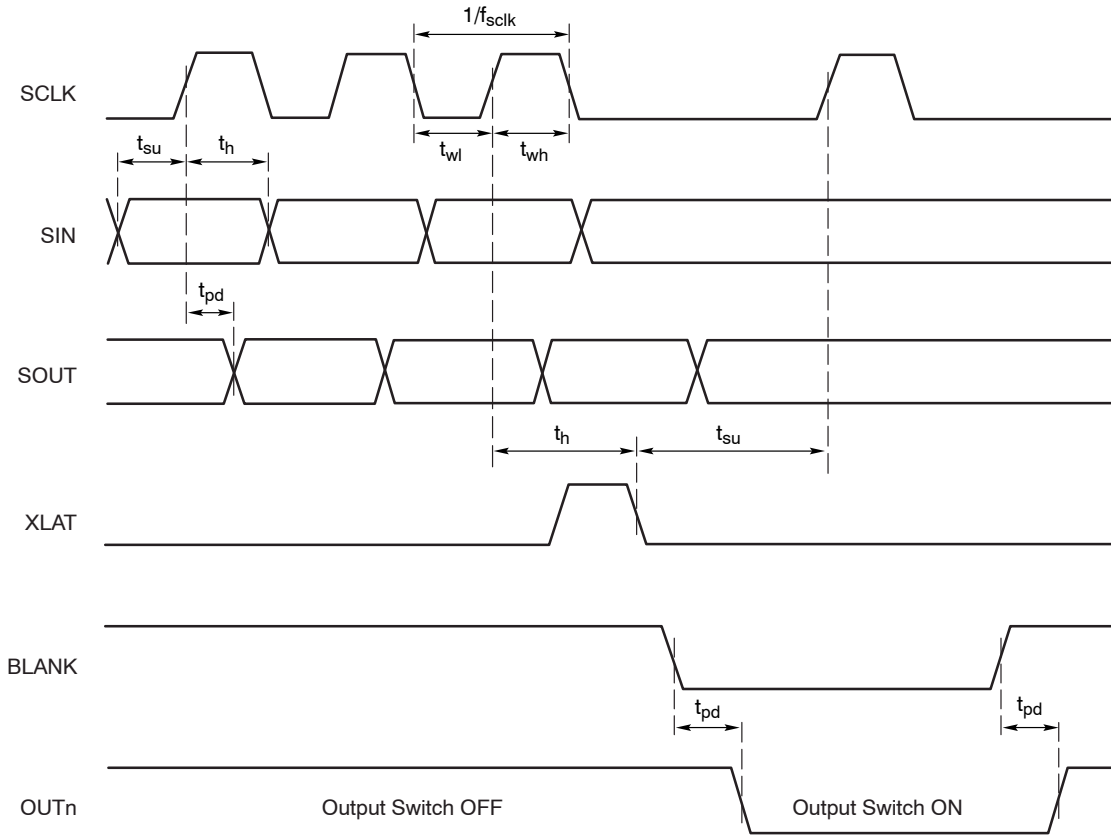


Figure 13. Timing Diagram

Application Information

For applications with a large number of LEDs, several CAT310 drivers can be daisy chained. The serial data output pin (SOUT) of the first driver is connected to the second driver data input pin (SIN). This sequence is repeated until the last driver is linked. All drivers are controlled by the

same clock signal. Figure 14 shows an example with three CAT310 devices driving a total of 30 LEDs in parallel. The controller transmits the serial data sequentially through the CAT310 devices. For N drivers connected in cascade, after $10 \times N$ clock pulses, the data are latched with one single XLAT transition.

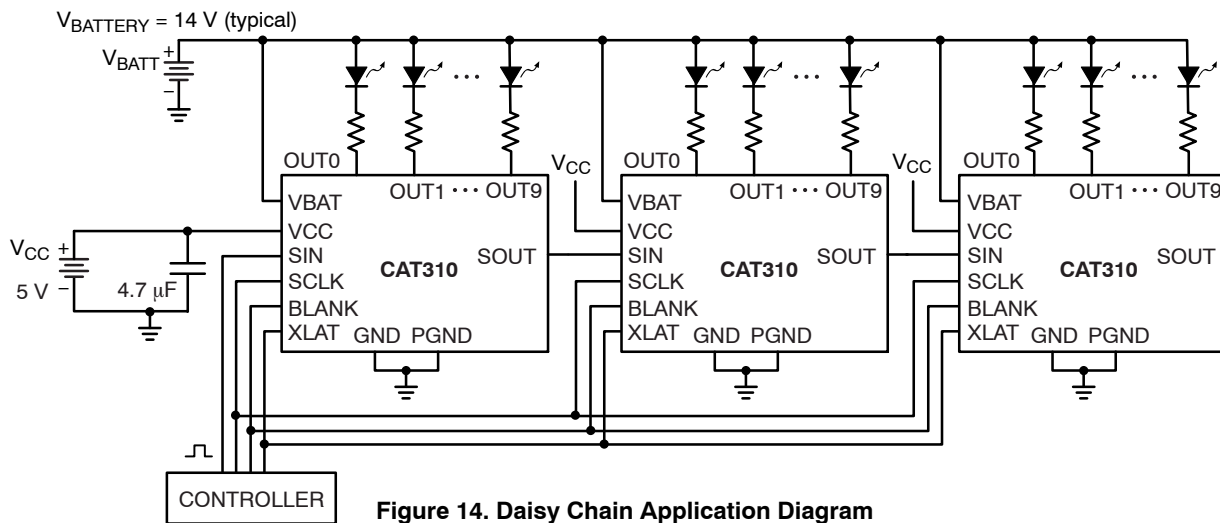
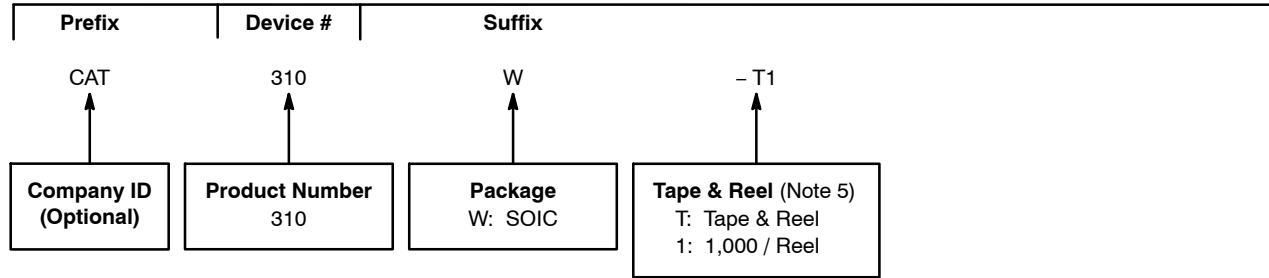


Figure 14. Daisy Chain Application Diagram

CAT310

Example of Ordering Information (Note 2)



2. The device used in the above example is a CAT310W-T1 (SOIC, Tape & Reel, 1,000 / Reel).
3. All packages are RoHS-compliant (Lead-free, Halogen-free).
4. The standard lead finish is Matte-Tin.
5. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

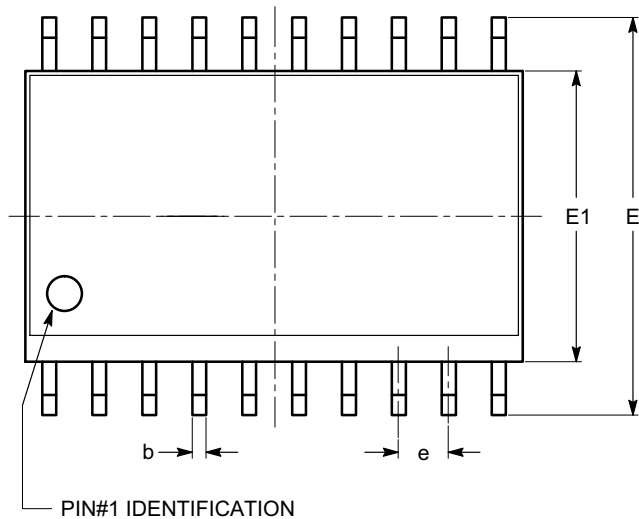
PACKAGE DIMENSIONS

ON Semiconductor®



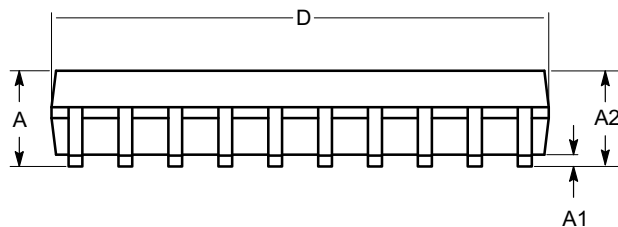
SOIC-20, 300 mils
CASE 751BJ-01
ISSUE O

DATE 19 DEC 2008

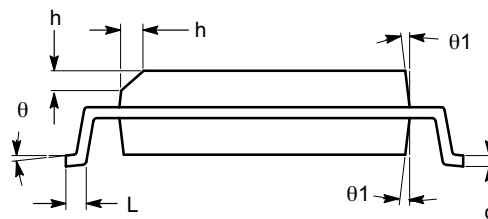


TOP VIEW

| SYMBOL | MIN | NOM | MAX |
|------------|----------|-------|-------|
| A | 2.36 | 2.49 | 2.64 |
| A1 | 0.10 | | 0.30 |
| A2 | 2.05 | | 2.55 |
| b | 0.31 | 0.41 | 0.51 |
| c | 0.20 | 0.27 | 0.33 |
| D | 12.60 | 12.80 | 13.00 |
| E | 10.01 | 10.30 | 10.64 |
| E1 | 7.40 | 7.50 | 7.60 |
| e | 1.27 BSC | | |
| h | 0.25 | | 0.75 |
| L | 0.40 | 0.81 | 1.27 |
| θ | 0° | | 8° |
| $\theta 1$ | 5° | | 15° |



SIDE VIEW



END VIEW

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-013.

| | | |
|-------------------------|--------------------------|---|
| DOCUMENT NUMBER: | 98AON34287E | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | SOIC-20, 300 MILS | PAGE 1 OF 1 |

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales