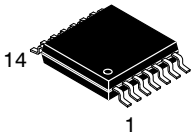
Low Voltage Quad 2-Input NAND Gate with 3.6 V Tolerant Inputs and Outputs

74ALVC00



TSSOP−14, WB
CASE 948G

Description

The ALVC00 contains four 2−input NAND gates. This product is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V.

The ALVC00 is fabricated with an advanced CMOS technology to achieve high−speed operation while maintaining low CMOS power dissipation.

Features

- 1.65 V to 3.6 V V_{CC} supply operation
- 3.6 V Tolerant Inputs and Outputs
- t_{PD}
  - 3 ns max for 3.0 V to 3.6 V V_{CC}
  - 3.5 ns max for 2.3 V to 2.7 V V_{CC}
  - 4.4 ns max for 1.65 V to 1.95 V V_{CC}
- Power−off High Impedance Inputs and Outputs
- Uses Patented Quiet Series M noise/EMI reduction circuitry
- Latch−up conforms to JEDEC JED78
- ESD Performance:
  - Human body model > 2000 V
  - Machine model > 250 V

MARKING DIAGRAM

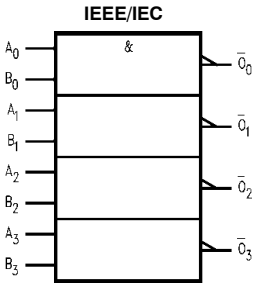
Z	= Assembly Plan Code
XY	= Date Code (Year & Week)
KK	= Lot Run Traceability Code
ALVC00	= Specific Device Code

ORDERING INFORMATION

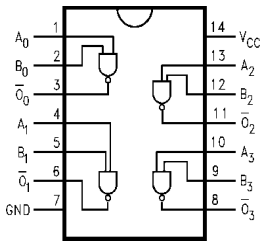
See detailed ordering and shipping information on page 4 of this data sheet.

© Semiconductor Components Industries, LLC, 2016

Logic Symbol



Connection Diagram



Pin Description

Pin Names	Description
A_n, B_n	Inputs
On	Outputs

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply Voltage	−0.5 to + 4.6	V
V_I	DC Input Voltage	−0.5 to 4.6	V
V_O	Output Voltage (Note 2)	−0.5 V to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current, V_I < 0 V	−50	mA
I_{OK}	DC Input Diode Current VO < 0 V	−50	mA
I_{OH}/I_{OL}	DC Output Source/Sink Current	±50	mA
I_{CC}	DC Ground Current per Supply Pin	±100	mA
T_{STG}	Storage Temperature	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.
2. I_O Absolute Maximum Rating must be observed, limited to 4.6 V.
3. Floating or unused control inputs must be held HIGH or LOW.

RECOMMENDED OPERATING CONDITIONS (Note 3)

Symbol	Parameter	Min.	Max.	Unit
−	Power Supply Operating	1.65	3.65	V
V_I	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Free−Air Operating Temperature	−40	+85	°C
Lit/LiV	Minimum Input Edge Rate, V_{IN} = 0.8 V to 2.0 V, V_{CC} = 3.0 V	−	5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	Min.	Max.	Unit
V_{IH}	HIGH Level Input Voltage		1.65–1.95 2.3–2.7 2.7 – 3.6	0.65 x V_{CC} 1.7 2.0	– – –	V
V_{IL}	LOW Level Input Voltage		1.65–1.95 2.3–2.7 2.7 – 3.6	– – –	0.35 x V_{CC} 0.7 0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = –100 μA	1.65–3.6	V_{CC} – 0.2	–	V
		I_{OH} = –4 mA	1.65	1.2	–	
		I_{OH} = –6 mA	2.3	2.0	–	
		I_{OH} = –12 mA	2.3 2.7 3.0	1.7 2.2 2.4	– – –	
		I_{OH} = –24 mA	3.0	2	–	
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	1.65–3.6	–	0.2	V
		I_{OL} = 4 mA	1.65	–	0.45	
		I_{OL} = 6 mA	2.3	–	0.4	
		I_{OL} = 12 mA	2.3 2.7	–	0.7 0.4	
		I_{OL} = 24 mA	3.0	–	–	
I_I	Input Leakage Current	0 ≤ V_I ≤ 3.6 V	3.6	–	r5.0	μA
I_{CC}	Quiescent Supply Current	VI = V_{CC} or GND, I_O = 0	3.6	–	10	μA
11I_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} – 0.6 V	3–3.6	–	750	μA

AC ELECTRICAL CHARACTERISTICS

		TA = –40°C to +85°C, R_L = 500 Ω								
		C_L = 50 pF				**C_L = 30 pF**				
		V_{CC} = 3.3 V ± 0.3 V		**V_{CC} = 2.7 V**		**V_{CC} = 2.5 V ± 0.2 V**		**V_{CC} = 1.8 V ± 0.15 V**		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PHL}, t_{PLH}	Propagation Delay	1.0	3.0	–	3.5	1.0	3	1.0	4.4	ns

CAPACITANCE

			T_A = ± 25°C		
Symbol	**Parameter**	**Test Conditions**	**V_{CC}**	**Typical**	**Unit**
C_{IN}	Input Capacitance	V_I = 0 V or V_{CC}	3.3	4.5	pF
C_{PD}	Power Dissipation Capacitance		3.3	23	pF
		f = 10 Mhz, C_L = 50 pF	2.5	21	
			1.8	20	

AC LOADING AND WAVEFORMS

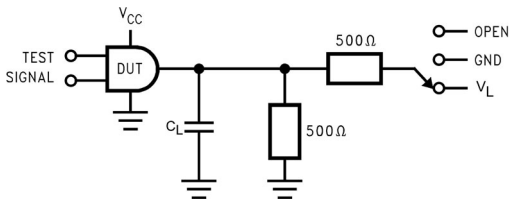


TABLE 1. Values for Figure 1

Test	Switch
t_{PLH}, t_{PHL}	Open

Figure 1. AC Test Circuit

TABLE 2. Variable Matrix

(Input Characteristics: f = 1MHz; $t_r = t_f$ = 2ns; Z_0 = 50 Ω

Symbol	V_{CC}			
	3.3 V ± 0.3 V	2.7 V	2.5 V ± 0.2 V	1.8 V ± 0.15 V
V_{mi}	1.5 V	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5 V	1.5 V	$V_{CC}/2$	$V_{CC}/2$

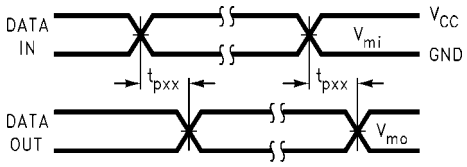


Figure 2. Waveform for Inverting and Non−inverting Functions

ORDERING INFORMATION

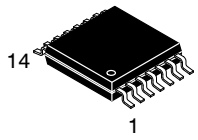
Product Number	Package	Shipping†
74ALVC00MTC	TSSOP−14 WB (Pb−Free/Halide Free)	2500 / Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

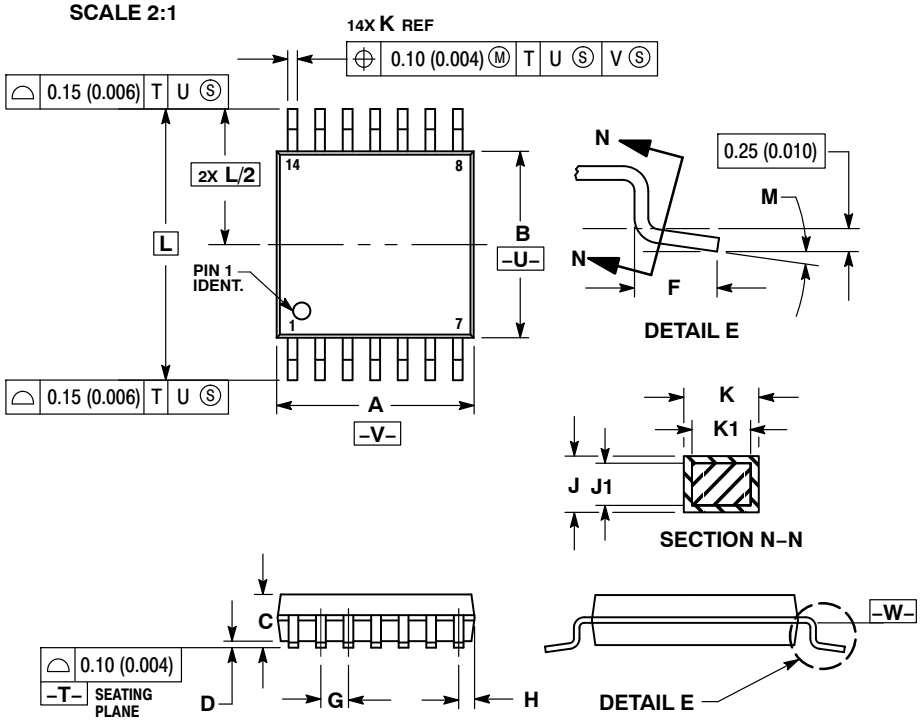
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016



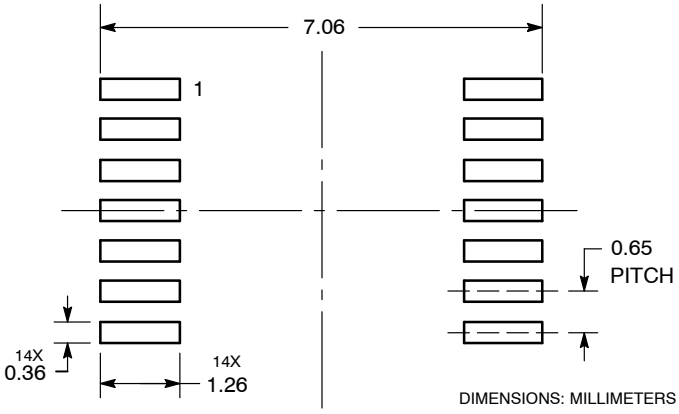
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

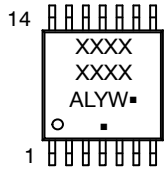
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASH70246A**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales