ON Semiconductor

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16-bit Microcontroller 512K-byte Flash ROM / 24K-byte RAM

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Features

- 16-channel 12-bit resolution AD converter
- Iinfrared remote controller receiver circuit
- CRC operating circuit
- Internal Reset Function

Performance

- 83.3 ns (12.0 MHz) $V_{DD} = 3.0 \text{ to } 3.6 \text{ V}$ Ta = -40°C to +85°C
- 100 ns (10.0 MHz) $V_{DD} = 2.7$ to 3.6 V Ta = -40°C to +85°C

Function Descriptions

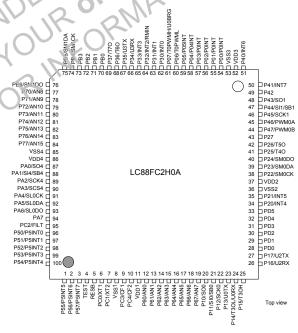
- Xstromy16 CPU
- 4G-byte address space
- General-purpose registers : 16 bits × 16 registers
- Ports
 - I/O Ports 86
- Power supply pins 8 (VSS1 to VSS4, VDD1 to VDD4)
- Timer
 - 16-bit timers \times 8
- Base timer serving as a time-of-day clock
- Serial interfaces
- Synchronous SIO interfaces × 3 (with automatic transmission capability)
- Single master I²C/synchronous SIO interface × 2
- Slave I²C/synchronous SIO interface
- Asynchronous SIO (UART) interfaces × 3
- Multifrequency 12-bit PWM modules
- 16-channel 12-bit resolution AD converter
- Watchdog timer
- Infrared remote controller receiver circuit
- CRC operating circuit
- Real time clock
- System clock frequency divider
- CF oscillator circuit, Crystal oscillator circuit, RC oscillator circuit
- 61-source 14-vector interrupt feature
- On-chip debugger function

Application

• Home audio, Car audio, White goods



TQFP100 1 9x14 / TQFP100



Pin Assignment (Top view)

ORDERING INFORMATION

See detailed ordering and shipping information on page 48 of this data sheet.

^{*} This product is licensed from Silicon Storage Technology, Inc. (USA)

Function Details

- Xstromy16 CPU
 - 4G-byte address space
 - General-purpose registers : 16 bits × 16 registers

■ Flash ROM

- Programming voltage level: 2.7 to 3.6 V.
- Block-erasable in 2K byte units.
- Data written in 2-byte units.
- 524288 × 8 bits

RAM

- 24576 × 8 bits
- Minimum instruction cycle time (tCYC)
 - 83.3 ns (12 MHz), $V_{DD} = 3.0 \text{ to } 3.6 \text{ V}$
 - 100 ns (10 MHz), $V_{DD} = 2.7$ to 3.6 V

■ Ports

• Normal withstand voltage I/O ports

• Oscillation/normal with stand voltage I/O ports

Normal withstand voltage I/O ports

Ports whose I/O direction can be designated in 1 bit units: 86 (P0n P1n, P2n, P3n, P4n, P5n, P6n, P7n, PAr, PB0 to PE6 PC2 PD0 to PD5)

Oscillation/normal with stand voltage I/O ports: 4 (PC0, PC1, PC3, PC4)

TEST pins

Power 7: • Reset pins • TEST pins

• Power pins 8 (VSS1 to 4,

Timers

- Timer 0: 16-bit timer that supports PWM/toggle outputs
 - <1> 5-bit prescaler
 - <2> 8-bit PWM \times 2. 8-bit timer + 8-bit PWM mode selectable
 - <3> Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator.
- Timer 1: 16-bit timer with capture registers
 - <1>5-bit prescaler
 - <2> May be divided into 2 channels of 8-bit timer
 - > Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator
 - Timer 2: 16-bit timer with capture registers
 - <1>4-bit prescaler
 - <2> May be divided into 2 channels of 8 bit timer
 - <3> Clock source selectable from system clock, OSC0, OSC1, and external events
- Timer 3 . 16-bit timer that shpports PWM/toggle outputs
 - <1> 8-bit prescaler
 - <2> 8-bit timer × 2 ch or 8-bit timer + 8-bit PWM mode selectable
 - <3> Clock source selectable from system clock, OSC0, OSC1, and external events
- Timer 4: 16-bit timer that supports toggle outputs
 - <1> Clock source selectable from system clock and prescaler 0
- Timer 5 : 16-bit timer that supports toggle output
 - <1> Clock source selectable from system clock and prescaler 0
- Timer 6: 16-bit timer that supports toggle outputs
 - <1> Clock source selectable from system clock and prescaler 1
- Timer 7: 16-bit timer that supports toggle output
 - <1> Clock source selectable from system clock and prescaler 1
- * Prescaler 0 and 1 are consisted of 4bits and can choose their clock source from OSC0 or OSC1.

• Base timer

- <1> Clock may be selected from OSC0 (32.768 kHz crystal oscillator) and frequency-divided output of system clock.
- <2> Interrupts can be generated in 7 timing schemes.

■ Real time clock

- <1> Calender with Jan. 1, 2000 to Dec.31, 2799 including automatic leapyear calculation function.
- <2> Consisted of Indipendent second-minuit-hour-day-month-yeare-century counters.

■ Serial interfaces

- SIO0 : 8-bit synchronous SIO
 - <1> LSB first/MSB first mode selectable
 - <2> Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
 - <3> Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
 - <4> Continuous/automatic data transmission (9- to 32768-bit units specifiable)
 - <5> Interval function (intervals specifiable in 0 to 64tSCK units)
 - <6> Wakeup function
- SIO1 : 8-bit synchronous SIO
 - <1> LSB first/MSB first mode selectable
 - <2> Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
 - <3> Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
 - <4> Continuous/automatic data transmission (9- to 32768-bit units specifiable)
 - <5> Interval function (intervals specifiable in 0 to 64tSCK units)
 - <6> Wakeup function
- SIO4 : 8-bit synchronous SIO
- NEW DESIGN MINDESIGN ATION <1> LSB first/MSB first mode selectable
 <2> Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
 - <3> Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
 - JEFOR ME <4> Continuous/automatic data transmission (9- to 32768-bit units specifiable)
 - <5> Interval function (intervals specifiable in 0 to 64tSCK units)
 - <6> Wakeup function
- SMIIC0 : Single master I²C/8-bit synchronous SIO
 - Mode 0 : Single-master mode communication
 - Mode 1: Synchronous 8-bit serial I/O (MSB first)
- SMIIC1 : Single master I²C/8-bit synchronous SIO
 - Mode 0 Single-master mode communication
 - Mode 1: Synchronous 8-bit seriel I/O (MSB first)
 - SLIIC Slave I²C/8-bit synchronous SIO
 - Mode $0: I^2C$ slave mode communication
 - Mode 1: Synchronous 8-bit seriai I/O (MSB first)
 - Note: usable only with the external clock source

• UART0

<1> Data length : 8 bits (LSB first)

<2> Start bits : 1 bit <3> Stop bits : 1 bit

<4> Parity bits : None/even parity/odd parity

<5> Transfer rate : 4/8 cycle

<6> Baudrate source clock: P07 input signal used as a 1 cycle signal (T0PWMH can be used as a clock source) or

FOR NEW DESIGN
ONSORMATION
ORWATION

Timer4 cycle.

<7> Full duplex communication

Note: The "cycle" refers to one period of the baudrate clock source.

• UART2

<1> Data length : 8 bits (LSB first)

<2> Start bits : 1 bit <3> Stop bits : 1/2 bit

<4> Parity bits : None/even parity/odd parity

<5> Transfer rate : 8 to 4096 cycle

<6> Baudrate source clock : System clock/OSC0/OSC1/P26 input signal

<7> Wakeup function

<8> Full duplex communication

Note: The "cycle" refers to one period of the baudrate clock source

• UART3

<1> Data length : 8 bits (LSB first)

<2> Start bits : 1 bit <3> Stop bits : 1/2 bit

<4> Parity bits : None/even parity/odd parity

<5> Transfer rate : 8 to 4096 cycle

<6> Baudrate source clock System clock/OSCO/OSCO/P36 input signal

<7> Wakeup function

<8> Full duplex communication

Note The "cycle" refers to one period of the baudrate clock source.

■ AD converter

- 1> 12/8 bits resolution selectable
- Analog input: 16 channels
- 3> Comparator mode

■ PWM

- FWM6: Multifrequency 12-bit PWM × 2 channels (PWM0A and PWM0B)
 - <1> 2-channel pairs controlled independently of one another
 - <2> Clock source selectable from system clock or OSC1
 - <3> 8-bit prescaler : TPWMR0= (prescaler value + 1) × clock period
 - <4> 8-bit fundamental wave PWM generator circuit + 4-bit additional pulse generator circuit
 - <5> Fundamental wave PWM mode

Fundamental wave period : 16 TPWMR0 to 256 TPWMR0

High pulse width : 0 to (Fundamental wave period - TPWMR0)

<6> Fundamental wave + additional pulse mode

Fundamental wave period : 16 TPWMR0 to 256 TPWMR0 Overall period : Fundamental wave period \times 16

High pulse width : 0 to (Fundamental wave period - TPWMR0)

■ CRC operating circuit

■ Watchdog timer

- <1> Driven by the base timer + internal watchdog timer dedicated counter
- <2> Interrupt or reset mode selectable

■ Infrared Remote Controller Receiver Circuit

- 1) Noise rejection function (noise filter time constant: Approx. 120 µs when the 32.768 kHz crystal oscillator is selected as the reference clock source)
- 2) Supports data encording systems such as PPM (Pulse Position Modulation) and Manchester encording
- 3) X'tal HOLD mode release function

■ Internal Reset Function

- Power-on reset (POR) function
 - 1) POR reset is generated only at power-on time.
 - 2) The POR release level can be selected through option configuration.
- Low-voltage detection reset (LVD) function
 - 1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
 - 2) The use/disuse of the LVD function and the low voltage threshold level can be selected by option configuration.

■ Interrupts (peripheral function))

- Any interrupt requests of the level equal to or lower than the current interrupt are not accepted <2> When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Interrupt Module
1	08000Н	Watchdog timer (1)
2	08004H	Base timer (2)
3	08008H	Timer () (2)
4	0800CH	INT0 (1)
5	08014H	INT1 (1)
6	08018H	INT2 (1) / timer 1 (2) / UART2 (4)
7	0801CH	INT3 (1) / timer 2 (4) / SMIIC6 (1) / SLIIC1 (1)
8	08020H	INT4 (1) / timer 3 (2) / Inibred remote control receiver (4)
9	08024H	INT5 (1) / timer 4 (1) / SiO1 (2)
10	0802Сн	PWM0 (1) / SMhC1 (1)
11	08030Н	ADC (1) / timer 5 (1) / SIO4 (2)
12	08C34H	IN 16 (1) / timer 6 (1) / UART 3 (4)
13	08038H	INT7 (1) / SIO0 (2) / SIO0(2)
14	0803CH	Port 0 (3) / Port 5 (8) / RTC (1) / CRC (1)

- 3 priority levels selectable
- Of interrupts of the same level, the one with the smallest vector address takes precedence.
- A number enclosed in parentheses denotes the number of sources.

■ Subroutine stack : RAM area

- Subroutine calls that automatically save PSW, interrupt vector calls : 6 bytes
- Subroutine calls that do not automatically save PSW: 4 bytes

■ Multiplication/division instructions

- 16 bits × 16 bits (4 tCYC execution time)
- 16 bits ÷ 16 bits (18 to 19 tCYC execution time)
- 32 bits ÷ 16 bits (18 to 19 tCYC execution time)

Oscillator circuits

- RC oscillator circuit (internal): For system clock
- CF oscillator circuit (built-in Rf circuit): For system clock(OSC1)
- Crystal oscillator circuit (built-in Rf circuit): For low-speed system clock (OSC0)
- SLRC oscillator circuit (internal): For system clock (In the case of exception processing)
- VCO oscillator circuit : For timer3,4,5,6,7 clock

■ System clock divider function

- Can run on low current.
- 1/1 to 1/128 of the system clock frequency can be set.

■ Standby function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
 - <1> Oscillation is not stopped automatically.
 - <2> Released by a system reset or occurrence of an interrupt.
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
 - <1>OSC1, RC, and OSC0 oscillations automatically stop.
 - <2> There are six ways of releasing the HOLD mode:
- (1) Setting the reset pin to the low level
 (2) Setting at least one of the INT0, INT1, INT2, INT4, INT5, INT6, and INT7 pins to the specified level
 (3) Having an interrupt source established at port 0
 (4) Having an interrupt source established at port 5
 (5) Having an interrupt source stablished at port 5

 - (5) Having an interrupt established at SIO0, SIO1 or SIO4
 - (6) Having an interrupt established at UART2 or UART3
- HOLDX mode: Suspends instruction execution and the operation of the peripheral circuits except those which run on
 - <1>OSC1 and RC oscillations automatically stop.
 - <2> OSC0 maintains the state that is established when the HOLDY mode is entered.
 - <3> There are nine ways of releasing the HOLDX mode.
 - (1) Setting the reset pin to the low level
 - (2) Setting at least one of the INT0, INT1, INT2, INT4, INT5, INT6, and INT7 p ins to the specified level
 - (3) Having an interrupt source established at port 3
 - (4) Having an interrupt source established at port 5
 - (5) Having an interrupt source established at the base timer circuit
 - (6) Paving an incrrupt established at SIO0, SIO1 or SIO4
 - (7) Having an interrupt established at UART2 or UATR3
 - (8) Having an interrupt established at Infared renote control receiver.
 - (9) Having an interrupt source established at the real time clock circuit

■ On-chip debugger function

- Supports software debuggirg with the IC mounted on the target board.
- Supports source line debugging and tracing functions, and breakpoint setting and real time display.
- Single-wire communication

■ Package form

• TQFP100 (14 × 14): Pb-Free and Halogen Free type

■ Development tools

• On-chip debugger: EOCUIF1 or EOCUIF2 + LC88FC2H0A

■ Programming board

Package	Programming Board
TQFP100 (14 × 14)	W88F52TQ

■ Flash ROM Programmer

Mak	er	Model	Supported Version	Device
Flash Support Single		AF9709C		
Group	programmer			
Company	Gang	AF9723/AF9723B(Main body)		
(FSG)	programmer	(Include Ando Electric Co.,Ltd.		
		models		
		AF9833(Unit)		
		(Include Ando Electric Co.,Ltd.		
		Models)		
Flash Support	On-board	AF9101/AF9103(Main budy)	(Note 2)	LC88FC2H0A
Group	Single /	(FSG models)		
Company	Gang	SIB88 Type A		
(FSG)	programmer	(Interface driver)		
+		(ON Semiconductor model)		
ON				
Semiconductor				1,5
(Note 1)				
	Single /	SKK Type C	Application Version	LC83FC2H0A
ON	Gang	(SanyoFWS)	After 1.08	
Semiconductor	programmer		Chip Data Version	
			After 2.46	
	On-board	FWS-X16DI Type 2	Application Version	LC88FC2H0A
	Single		After 1.08	10/2
	programmer		Chip Data Version	1
			After 2 45	17,

For information about AF-Series:

Flash Support Group Company (TOA ELECTRONICS, Inc.)

TEL: +81-53-459-1050 E-mail: sales@j-fsg.co.jp

Note1 : On-board-programmer from FSG (AF9101/AF9103) and serial interface driver from our company (SIB86-TypeA) together can give a PC-less, standalone on-board-programming capabilities.

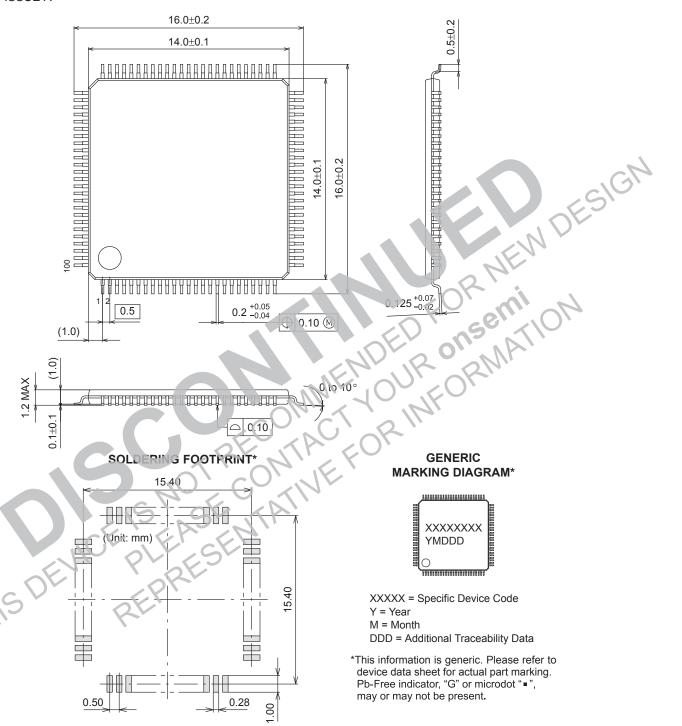
Note2: It needs a special programming devices and applications depending on the use of programming environment. Please ask FSG or our company for the information.

Package Dimensions

unit: mm

TQFP100 14x14 / TQFP100

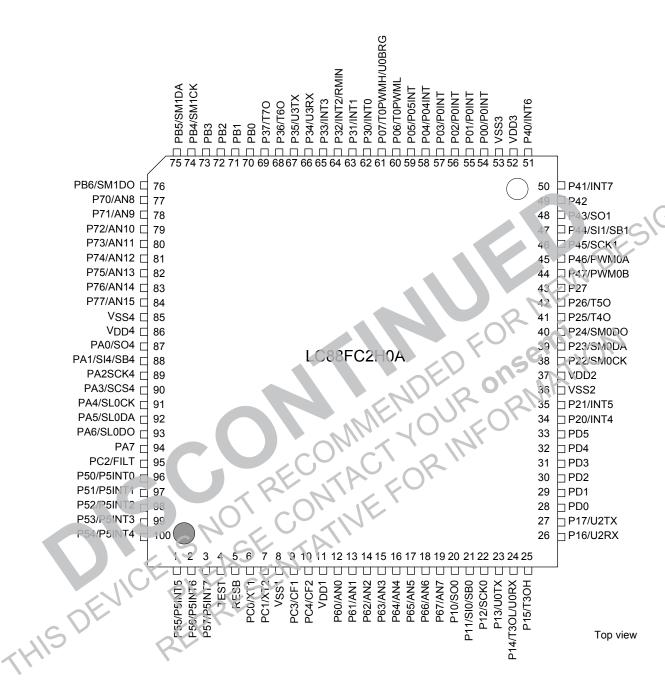
CASE 932AY ISSUE A



NOTE: The measurements are not to guarantee but for reference only.

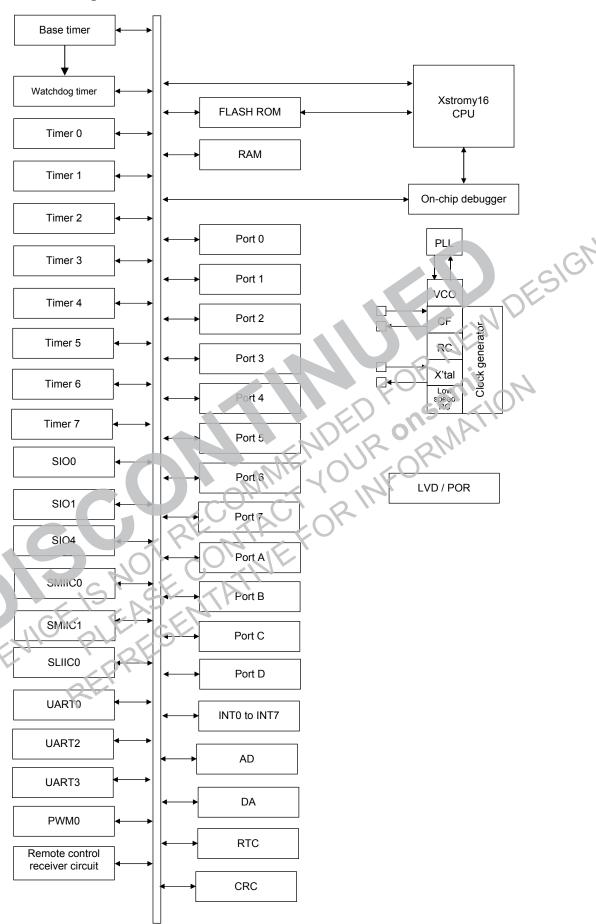
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Pinout



TQFP100 (14×14) (Pb-Free and Halogen free type)

System Block Diagram



Pin Description

Pin Descri	puon	
Pin Name	I/O	Description
VSS1, VSS2,	1	– power sources
VSS3, VSS4		
VDD1, VDD2,	_	+ power sources
VDD3, VDD4		
Port 0	I/O	• 8-bit I/O port
P00 to P07		• I/O specifiable in 1-bit units
100 to 107		Pull-up resistors can be turned on and off in 1 bit units
		• HOLD release input (P00 to P03, P04, P05)
		• Port 0 interrupt input (P00 to P03, P04, P05)
		• Pin functions
		P06 : Timer 0L output
		P07 : Timer 0L output/UART0 clock input
Port 1	I/O	• 8-bit I/O port
P10 to P17		• I/O specifiable in 1-bit units
110 10 117		• Pull-up resistors can be turned on and off in 1 bit units
		• Pin functions
		P10 : SIO0 data output
		P11 : SIO0 data input/pulse input/output
		P12 : SIO0 clock input/output
		P13 : UART0 transmit
		P14 : Timer 3L output/UART0 receive
		P15 : Timer 3H output
		P16: UART2 receive
		P17 : UART2 transmit
Port 2	I/O	• 8-bit I/O port
P20 to P27		• I/O specifiable in 1-bit units
120 to 127		• Pull-up resistors can be turned on and off in 1 bit units
		• Pin functions
		P20: INT4 input/HOLD release input/timer 3 event input/
		timer 2L capture input/timer 2H capture input
		P21: INT5 input/HOLU release input/timer 3 event input/
		timer 2L capture input/timer 2H capture input
		P22. SMIICO clock input/output
		P23 : SMIIC 0 bus input/output/data input
		P24 . SMIIC0 data output (used in 3-wire SIO mode)
		P25 : Timer 4 output
		P26 · Timer 5 output
.,	GY	Interrupt acknowledge type
		INT4, INT5: H level, L level, H edge, L edge, both edges

Continued on next page.

Continued from preceding page

I/O	Description
I/O	
	• 8-bit I/O port
	• I/O specifiable in 1-bit units
	• Pull-up resistors can be turned on and off in 1 bit units
	• Pin functions
	P30 : INT0 input/HOLD release/timer 2L capture input
	P31: INT1 input/HOLD release/timer 2H capture input
	P32 : INT2 input/HOLD release/timer 2 event input/timer 2L capture input/ Infrared Remote Controller Receiver input
	P33 : INT3 input/HOLD release/timer 2 event input/timer 2H capture input
	P34: UART3 receive
	P35 : UART3 transmit
	P36 : Timer 6 output
	P37 : Timer 7 output
	Interrupt acknowledge type
	INT0 to INT3 : H level, L level, H edge, L edge, both edges
I/O	• 8-bit I/O port
	• I/O specifiable in 1-bit units
	• Pull-up resistors can be turned on and off in 1 bit units
	• Pin functions
	Prin runctions P40: INT6 input/HOLD release input P41: INT7 input/HOLD release input P43: SIO1 data output P44: SIO1 data input/bus input/output
	P41: INT7 input/HOLD release input
	P43 : SIO1 data output P44 : SIO1 data input/bus input/output
	P45 : SIO1 clock input/output
	P46 : PWM0A output
	P47 : PWM0Boutput
	Interrupt acknowledge type
	INT6, INT7: H level, L level, H edge, L edge, both edges
I/O	• 8-bit I/O port
	• I/O specifiable in 1-bit units
	Pull-up resistors can be turned on and off in 1 bit units
	• HOLD release input
	Port 0 interrupt input
1/0.	8-bit I/O port
	• 1/O specifiable in 1-bit units
	Pull-up resistors can be turred on and off in 1 bit units
	• Pin functions
	ANO (P60) to AN7 (P67): AD converter input port
1/0	• 8-bit I/O port
CX	• I/O specifiable in 1-bit units
O'	• Full up resistors can be turned on and off in 1 bit units
~	• Pin functions
	AN8 (P70) to AN15 (P77) : AD converter input port
	I/O

Pin Name	1/0	ceding page. Description
		· · · · · · · · · · · · · · · · · · ·
Port A	I/O	• 8-bit I/O port
PA0 to PA7		• I/O specifiable in 1-bit units
		• Pull-up resistors can be turned on and off in 1 bit units
		Multiplexed pin functions
		PA0 : SIO4 data output
		PA1 : SIO4 data input/pulse input/output
		PA2 : SIO4 clock input/output
		PA3 : SIO4 chip select input PA4 : SLIIC0 clock input
		PA5 : SLIICO bus input/output/data input
		PA6 : SLIIC0 data output (used in 3-wire SIO mode)
Port B	I/o	• 7-bit I/O port
PB0 to PB6		• I/O specifiable in 1-bit units
PB0 10 PB0		•Pull-up resistors can be turned on and off in 1 bit units
		• Multiplexed pin functions
		PB4: SMIIC1 clock input/output
		PB5 : SMIIC1 bus input/output/data input
		PB6 : SMIIC1 data output (used in 3-wire SIO mode)
Port C	I/O	• 5-bit I/O port
PC0 to PC4		• I/O specifiable in 1-bit units
		• Pull-up resistors can be turned on and off in 1 bit units(PC2)
		• Pin functions
		PC0: 32.768 kHz crystal oscillator input
		PC1: 32.768 kHz crystal ospilla or output PC2: FILT of VCO
		PC3 : Ceramic oscillator input
		I/O specifiable in 1-bit units Pull-up resistors can be turned on and off in 1 bit units(PC2) Pin functions PC0: 32.768 kHz crystal oscillator input PC1: 32.768 kHz crystal oscillator output PC2: FILT of VCO PC3: Ceramic oscillator input PC4: Ceramic oscillator output/VCO cutput
Port D	I/O	• 6-bit I/O port
	1,0	• I/O specifiable in 1-bit units
PD0 to PD5		• Pull-up resistors can be turned on and off in 1 bit units
TEST	I/O	TEST pin
		• Used to communicate with on-chip debugger.
		Connects an external 100 kΩ pull-do vn resistor.
RESB	I/O	
		15 CV XX
		12 12 11
		CE CENT
		DL CSV
	1	
$\sim V$		
5	<	2 K.
5		Reset pin

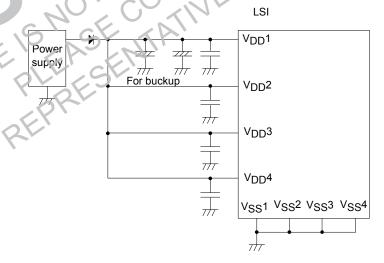
Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor. Data can be read into any input port even if it is in the output mode.

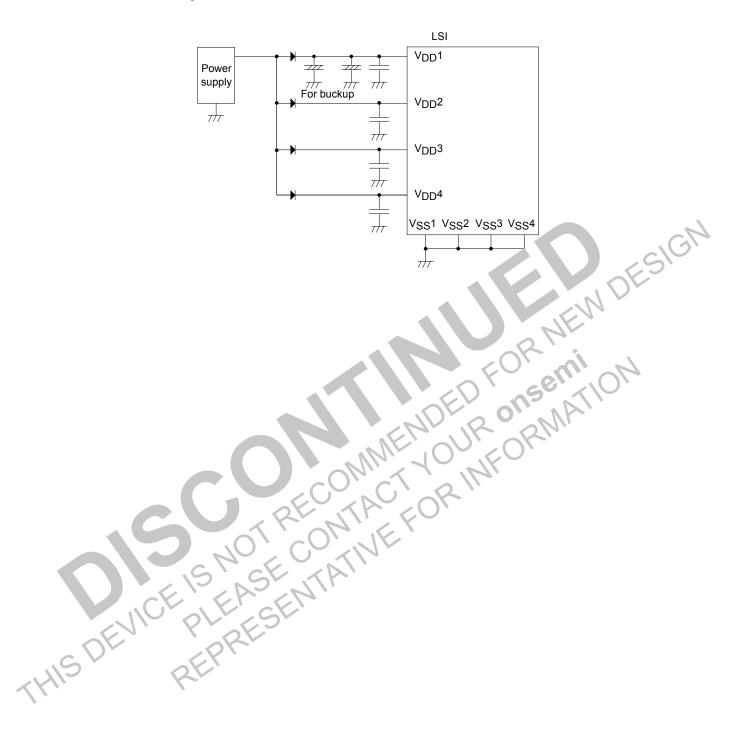
Port Name	Option Selected in Units of	Output Type	Pull-up Resistor
P00 to P07	1 bit	CMOS	Programmable
P10 to P17		Able to program special	
P20 to P27		functions'output type from CMOS	
P30 to P37		output or Nch-opendrain	
P40 to P47			
P50 to P57			
P60 to P67			
P70 to P77			
PA0 to PA7			
PB0 to PB6			
P60 to P67		CMOS	
P70 to p77			
PD0 to PD5			
PC2			
PC0	_	N-channel open drain	None
		(32.768 kHz crystal oscillator input)	No.
PC1	_	Nch-open drain	None
		(32.768k kHz crystal oscillator output)	O. W. 2
PC3	_	CMOS	None-
		(ceranic oscillator input)	7/2
PC4	-	CMOS	None
		(ceramic oscillator output)	2111.

^{*} Make the following connection to minimize the noise input to the VDD1 pin and prolong the backup time. Be sure to electrically short the VSS1, VSS3, VSS3 and VSS4 pins

Example 1: When data is being backed up in the HOLD mode, the H level signals to the output ports are fed by the backup capacitors.



Example 2 : When data is being backed up in the HOLD mode, the H level output at any ports is not sustained and is unpredictable.



■ Absolute Maximum Ratings at Ta = 25°C, V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0 V

	Parameter	Symbol	Applicable Pin	SS1 = VSS2 = VSS3 = Conditions	*331 0		Specific	cation	
	rarameter	Symbol	/Remarks		V _{DD} [V]	min	typ	max	unit
Max volt	ximum supply	VDD max	V _{DD} 1, V _{DD} 2, V _{DD} 3, V _{DD} 4	$V_{DD}1 = V_{DD}2 = V_{DD}3 = V_{DD}4$		-0.3		+4.6	
	at voltage	VI (1)	RESB			-0.3		V _{DD} +0.3	
Inpi	ut/output voltage	VIO (1)	Ports 0, 1, 2 Ports 3, 4,5 Ports 6, 7 Ports A, B, C, D			-0.3		V _{DD} +0.3	V
High level output current	Peak output current	IOPH (1)	Ports 0, 1, 2, 3 P40 to P45 Ports 7, A, D PB2 to PB6	CMOS output selected Per applicable pin		-7.5			
tput cu		IOPH (2)	P46, P47 PB0, PB1	Per applicable pin		-12.5			
rrent		IOPH (3)	Port 5, 6 PC0 to PC4	Per applicable pin		-4.5			,5
	Average output current (Note 1-1)	IOMH (1)	Ports 0, 1, 2, 3 P40 to P45 Ports 5, 6, 7, A PB2 to PB6 Ports D	CMOS output selected Per applicable pin		-5	NE	NO	
		IOMH (2)	P46, P47 PB0, PB1	Per applicable pin		-10	e m	10.	7
		IOMH (3)	Port 5, 6 PC0 to PC4	Per applicable pin	DEP	3	ANA.		
	Total output current	ΣΙΟΑΗ (1)	Pprts 5 PC0 to PC4	Total of currents at applicable pins	OUK	-10	Sla.		
		ΣΙΟΑΗ (2)	Port 6	Total of currents at applicable pins	IN	-10			mA
		ΣΙΟΑΗ (3)	Port 5, 6 PC0 to PC4	Total of currens at applicable pins	DR.	-20			
	16	ΣΙΟΑΗ (4)	Ports 1 D1 P 20 to P 21	total of currents at applicable page		-20			
		ΣΙΟΑΗ (5)	1 22 to P2/	Total of currents at applicable pins		-20			
		ΣΙΟΑΗ (6)	Ports 1, 2, D	Total of currents at applicable pins		-40			
	EVI	ΣΙΟΑΉ (7)	Ports 4	Total of currents at applicable pins		-20			
5	Or	ΣΙΟΑΗ (8)	Ports 0, 3	Total of currents at applicable pins		-20			
		ΣΙΟΛΗ (9)	Ports 0, 3, 4	Total of currents at applicable pins		-40			
		ΣΙΟΑΗ (10)	Ports B, 7	Total of currents at applicable pins		-20			
		ΣΙΟΑΗ (11)	Ports A	Total of currents at applicable pins		-20			
		ΣΙΟΑΗ (12)	Ports 7, A, B	Total of currents at applicable pins		-40	of 100 ma		

Note 1-1: Average output current refers to the average of output currents measured for a period of 100 ms.

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Applicable Pin	Conditions	Г		Specific	eation	
T urumeter	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Peak output current	IOPL (1)	Ports 0, 1, 3, 4 Ports 7, D	Per applicable pin					
el outpu		P20, P21, P24 to P27 PA0 to PA4, PA6, PA7 PB0 to PB4, PB6,					15	
Low level output current	IOPL (2)	P22, P23 PA4, PA5	Per applicable pin				20	
	IOPL (3)	PB4, PB5 Ports 5, 6 PC0 to PC4	Per applicable pin				7.5	
Average outp current (Note 1-1)	ut IOML (1)	PC0 to PC4 Ports 0, 1, 3, 4 Ports 7, D P20, P21, P24 to P27	Per applicable pin				12.5	
		PA0 to PA4, PA6, PA7 PB0 to PB4, PB6, PB7						6
	IOML (2)	P22, P23 PA4, PA5 PB4, PB5	Per applicable pin			NE	15	
	IOML (3)	Ports 5, 6 PC0 to PC4	Per applicable pin		OP		5	
Total output current	ΣIOAL (1)	Ports 5 PC0 to PC2	Total of currents at applicable pins	05	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	S	lo	mA
	ΣIOAL (2)	Port 6 PC3 to PC4	Total of currents at applicable pins	DYP	0,	MA	10	
	ΣIOAL (3)	Port 5, 6 PC0 to PC4	Total of currents at applicable plns	00,	ÇO'\		20	
	ΣIOAL (4)	Ports 1, D P20, P21	Total of currents at applicable pins	RIF			35	
	ΣΙΟΑΙ (5)	P22 to P27	Total of currents at applicable pins) ·			35	
	ΣΙΟΑL (6)	Ports 1, 2, D	Total of currents at applicable pins				70	
	ΣΙΟΑL (7) ΣΙΟΑL (8)	Port 4 Port 0, 3	Total of currents at applicable pins Total of currents at				35	
DEVI	ΣΙΟΑL (8)	Port 0, 3	applicable pins Total of currents at				35	
SOF	ΣΙΟΑΙ (10)	Port 7, B	applicable pins Total of currents at				70	
	ΣΙΟΑL (11)	Port A	applicable pins Total of currents at				35	
	ΣΙΟΑL (12)	Port 7, A, B	applicable pins Total of currents at				70	
Allowable power	Pd max	TQFP100	applicable pins $Ta = -40 \text{ to } +85^{\circ}\text{C}$,,,	
dissipation			Package with thermal resistance bord (Note 1-2)				460	mW
Operating ambient temperature	Topr		(1.000 1 2)		-40		+85	
Storage ambient temperature	Tstg				-55		+125	°C

Note 1-1 : Average output current refers to the average of output currents measured for a period of 100 ms. Note 1-2 : SEMI standards thermal resistance board (size : $76.1 \times 114.3 \times 1.6$ tmm, glass epoxy) is used.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

■ Allowable Operating Conditions at Ta = -40 to +85°C, V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0 V

<u> </u>	poracing	Conditions at ra	= -40 to +65°C, VSS1 = VS	<u> </u>	- v55 - -	0 V		
Parameter	Symbol	Applicable Pin/Remarks	Conditions			Specific	ation	
Parameter	Symbol	Applicable Pill/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Operating supply	V _{DD} (1)	VDD1=VDD2=VDD3	0.081 μs ≤ tCYC ≤ 66 μs		3.0		3.6	
voltage (Note 2-1)			0.098 μs ≤ tCYC ≤ 66 μs		2.7		3.6	
Memory sustaining supply voltage	VHD	VDD1=VDD2=VDD3	RAM and register contents sustained in HOLD mode		2.0		3.6	
High level input voltage	VIH (1)	Ports 0, 1, 2, 3, 4 Port 5, A, B		2.7 to 3.6	0.3V _{DD} +0.7		v _{DD}	
	VIH (2)	Ports 6, 7, D,PC2		2.7 to 3.6	0.3V _{DD} +0.7		V _{DD}	
	VIH (3)	RESB PC0, PC1, PC3, PC4		2.7 to 3.6	0.75V _{DD}		V _{DD}	
	VIH (4)	P22, P23, PA4, PA5, PB4, PB5 I2C side		2.7 to 3.6	0.7VDD		VDD	V
Low level input voltage	VIL (1)	When ports 1, 2, 3, 4, 5, A and port B, PnFSAn=0		2.7 to 3.6	VSS		$0.2 { m V}_{ m DD}$	
	VIL (2)	Ports 0, 6, 7, D, PC2 When ports 1, 2, 3, 4, 5, A and port B, PnFSAn=1		2.7 to 3.6	Vss	N/S	0.2V _{DD}	
	VIL (3)	CF1, RESB PC0, PC1,PC3, PC4		2.7 to 3.6	Ves	S.Z	0.25V _{DD}	
	VIL (4)	P22, P23, PA4, PA5, PB4, PB5 I2C side	I ENI	2.7 to 3.c	V _S S	W	0.3V _{DD}	
Instruction cycle time	tCYC		MALL	3 0 to 3.6	0.031		66	
(Note 2-2)			$\sim 0^{1/2}$	2.7 to 3.6	0.098		66	μs
External system clock frequency	FEXCF (1)	CF1	• CF2 pin open. • System clock frequency th vision ratic = 1/1	3.0 to 3.6	0.1		12	
	0	40 ° C	• External system clock PUT 150 ±5%	2.7 to 3.6	0.1		10	MHz
		P. ASVN	CF2 pin open • System clock frequency	3.0 to 3.6	0.2		24	
	U's	L'GE	division ratio = 1/2	2.7 to 3.6	0.2		20	

Note 2-1 . Pelationship between tCYC and oscillation frequency is 1/FmCF when frequency division ratio is 1/1 and 2/FmCF when the ratio is 1/2.

Continued on next page.

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D .	0 1 1	Applicable Pin	C Fr		Specification				
Parameter	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit	
Oscillation frequency range (Note 2-3)	FmCF (1)	PC3 (CF1), PC4 (CF2)	12 MHz ceramic oscillator mode See Fig. 1.	3.0 to 3.6		12			
(2.000 2.0)	FmCF (2)	PC3(CF1), PC4(CF2)	10 MHz ceramic oscillator mode See Fig. 1.	2.7 to 3.6		10		MHz	
	FmRC		Internal RC oscillation	2.7 to 3.6	0.5	1.0	2.0		
	FmSLRC		Internal low-speed RC oscillation	2.7 to 3.6	18	30	45		
	FsX'tal	XT1, XT2	32.768 kHz crystal oscillator mode See Fig. 2.	2.7 to 3.6		32.768		kHz	
	FmVCO(1)		VCO oscillator When setting FRQSEL = 0 See Fig. 9.	2.7 to 3.6	12		28	15	
	FmVCO(2)		VCO oscillator When setting FRQSEL = 1 See Fig. 9.	2.7 to 3.6	38	NE	70	MHz	
	FmVCO(5)		VCO oscillator	2.7 to 3.6	OR	Note 2-3		7	

Note 2-2: See Tables 1 and 2 for oscillator constant values

Note 2-3: VCO oscillation frequency = Ceramic oscillator frequency > Setting point of SELREF

...ges is not implied. Extended expo Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended

■ Electrical Characteristics at Ta = -40 to +85°C, V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0 V

Parameter	Symbol	Applicable Pin	Conditions		Specification				
1 drameter	Symbol	/Remarks		V _{DD} [V]	min	typ	max	unit	
High level input current	IIH (1)	Ports 0, 1, 2 Ports 3, 4, 5 Ports 6, 7 Ports A, B,C, D RESB	Output disabled Pull-up resistor off VIN = VDD (including output Tr. off leakage current)	2.7 to 3.6			1		
Low level input current	IIL (1)	Ports 0, 1, 2 Ports 3, 4, 5 Ports 6, 7 Ports A, B, C, D RESB	Output disabled Pull-up resistor off VIN = VSS (including output Tr. off leakage current)	2.7 to 3.6	-1			μА	
High level output voltage	VOH (1)	Ports 0, 1, 2, 3 Ports 5, 6	IOH = -0.4 mA	3.0 to 3.6	V _{DD} -0.4				
·	VOH (2)	Ports A, D, PC2 P40 to P45 PB2 to PB6	IOH = -0.2 mA	2.7 to 3.6	V _{DD} -0.4			C	
	VOH (3)	P46, P47	IOH = -1.6 mA	3.0 to 3.6	VDD-0.4				
	VOH (4)	PB0, PB1	IOH = -1.0 mA	2.7 to 3.6	V _{DD} -0.4		N		
	VOH (5)	PC0, PC1,	IOH = -1.0 mA	3.0 to 3.6	V _{DD} -0.4	JE	7 "		
	VOH (6)	PC3, PC4,	IOH = -0.4 mA	2.7 to 3.6	V _{DD} −0.4	19.			
Low level output voltage	VOL (1)	Ports 0, 1, 3, 4 Ports 5, 6, 7, D PC2	IOL = 1.6 mA	3.0 to 3.6	0/e	ewi	0.4	v	
	VOL (2)	P20 to P21, P24 to P27 PA0 to PA3 PA6 to PA7 PB0 to PB3, PB6	IOL = 1.0 mA	2.7 to 3.6	FOR	Mir	0.4		
	VOL (3)		IOL = 3.0 mA	3.0 to 3.6			0.4		
	VOL (4)	PA4, PA5, PB4, PB5	IOL = 1.3 mA	2.7 to 3.6			0.4		
	VOL (5)	PC0, PC1,	IOL = 1.0 mA	3.0 to 3.6			0.4		
	VOL (6)	PC3 PC4,	1OL = 0.4 mA	2.7 to 3.6			0.4		
Pull-up resistor	Rpu (1)	Ports 0, 1, 2, 3 Forts 4, 5, 6, 7	$VOH = 0.9V_{DD}$	3.0 to 3.6	15	35	80		
11/0	Rpu (2)	Ports A, B, D, PC2		2.7 to 3.6	15	35	100	kΩ	
Hysteresis voltage	VHYS	RESP When ports 1, 2, 3, 4, A, B PnFSAn=1		2.7 to 3.6		0.1VDD		V	
Pin capacitance	СР	All pins	Pins other than that under test VIN = VSS f = 1 MHz Ta = 25°C	2.7 to 3.6		10		pF	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

■ Serial I/O Characteristics at $Ta = -40 \text{ to } +85^{\circ}\text{C}$, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0 \text{ V}$

1-1. Serial I/O Characteristics (Wakeup Function Disabled) (Note 4-1-1)

Parameter Symbol Applicable Conditions VIDIO VIDIO	1-1	<u>. ১</u>	eriai i/O Ch	aracteristic	cs (wakeu	p Function Disabled)	(Note 4-1-1)	<u> </u>			-
Period SCK (1) SCKD (P12) SCE Fig. 6.		р	'arameter	Symbol		Conditions		<u> </u>	Specif	ication	
Low level ISCKH (1)		r		59111001	Pin/Remarks		V _{DD} [V]	min	typ	max	unit
High level pulse width tSCKH (1) tSCKH (2) tSCKH (2) pulse width tSCKH (2) pulse width tSCKH (2) pulse width tSCKH (2) pulse width tSCKH (2) tSCKH (Ser	Inp	Period	tSCK (1)	SCK0 (P12)	• See Fig. 6.		4		<u> </u>	-
High level pulse width tSCKH (1) tSCKH (2) tSCKH (2) pulse width tSCKH (2) pulse width tSCKH (2) pulse width tSCKH (2) pulse width tSCKH (2) tSCKH (ial c	ut cl	Low level	tSCKL (1)							
High level pulse width tSCKHA (1) tSCKHA (1) tSCKHA (1) tSCKHA (1) tSCKHA (1) tSCKHBSY (1a) tSCKHBSY (1b) tSCKHBSY (1b) tSCKHBSY (1b) tSCKHBSY (1b) tSCKHBSY (1b) tSCKHBSY (1b) tSCKH (2) tSCK	lock	ock						2			
See Fig. 6. 15CKHBSY (1a) 15CKHBSY (1b) 15CKH (2) 15CKHBSY (2a) 15CKHBSY (2b) 15CKHBSY (-	tSCKH (1)				2	<u> </u>	_	
Period ISCKHBSY (1a) ISCKH (2a) ISCKH (2b) ISCK			pulse width	tSCKHA (1)		Automatic communication		Γ <u></u>	<u> </u>]
							2.7 to 3.6	6			
Communication Communicatio				+CONTIDON				 	 		tCYC
See Fig. 6. SCK (2) SCK0 (P12) SCCK0 (P12) S								23			
Period ISCK (2) SCK0 (P12) SCK0 (P12) SCK0 (P12) SCK0 (P12) SCK0 (P12) SCK1 (2) Pulse width High level pulse width SCKHA (2) SCHA (2) SCHA (2) SCHA (2) SCHA (2) SCHA (2) SCHA ((1a)					<u> </u>	<u></u>	
See Fig. 6.				tSCKHBSY		Mode other than automatic					
Period ISCK (2) SCK0 (P12) CMOS output selected See Fig. 6.				(1b)				4			
See Fig. 6. 4 1/2			Dariod	tCCV (2)	SCKU (B12)						, c)
High level pulse width High level pulse wi		Jutp	1 01100	WCK (2)	SCNU (P12)	_	_ 1	4			
High level pulse width High level pulse wi		ut cl	Low level	tSCKL (2)							
High level pulse width tSCKH (2) tSCKHA (2) tSCKHBSY (2a) tSCKHBSY (2a) tSCKHBSY (2b) tSCHBSY (2b) tSCHB		ock		(2)					1/2	111	
Pulse width ISCKHA (2)				tSCKH (2)]				4		tSCK
CYC SCKHBSY (2a) CYC SCKHBSY (2a) CYC CMOS o mut selected 2.7 to 3.6 6 2.3 to 3.6 6 2.3 to 3.6 6 2.3 to 3.6 6 2.4 to 3.6 6 2.4 to 3.6 6 2.5 to 3.6 7 to 3.6			-					12	1/2	1-	
CMOS or put selected 2.7 to 3.6 6 ISCKHBSY (2a)				tSCKHA (2)				O,		7	
Second S							27 to 3.6	6	6,,	YO,	
Can Can								202	I.N		
Comparison of the comparison				tSCKHBSY			1.0	V	Mr.	=	1
See Fig. 6 See Fig. 6 See Fig. 6						mode		CK		23	tCYC
State Sta							D, C		1	23	
Communication mode 4				tSCKHDON			112		 		
See Fig. 6 See Fig. 6 O.03							6,	4			
SB0 (P11) rising edge of SIOCLK 0.03 0.03 0.03					(2)	• See Fig. 6) `				
Output delay time tdD0 (1) SO0 (P10), SB0 (P11) SO0 (P10) SO0 (P10), SB0 (P11) Output delay time tdD0 (2)	Ser	Dat	ta setup time					0.03	-		-
Output delay time tdD0 (1) SO0 (P10), SB0 (P11) SO0 (P10) SO0 (P10), SB0 (P11) Output delay time tdD0 (2)	ial iı				SB0 (P11)			0.03	<u> </u>		
Output delay time tdD0 (1) SO0 (P10), SB0 (P11) SB0 (P11) SB0 (P11) Time tdD0 (2)	nput	Dat	ta hold time	thDI(1)	CE.	See Pig. 0.	2.7 to 3.6				
Sep (P+1) ItCYC	1			P	5	1/1,		0.03			
Sep (P+1) ItCYC	Š		Output delay	tdD0 (1)	SO0 (P10)	• (Note 4-1-2)		 	 		
Output clock tdDO (2) • (Note 4-1-2) 2.7 to 3.6 1tCYC +0.05	erial	put				` ′		l ,	1		
Output clock tdDO (2) • (Note 4-1-2) 2.7 to 3.6 1tCYC +0.05	outı	cloc	K"	, ~	KV '			l ,			
utput clock ltCYC +0.05	tug	1	7	CY'				l ,		+0.05	μs
utput clock ltCYC +0.05	1			RV				<u> </u>	<u> </u>		
		Out		tdDO(2)		• (Note 4-1-2)	2.7 to 3.6	l ,			
		but (l ,		1+CVC	
		clock						ļ j			
		~						ļ ,		+0.05	
Note A.1.1: Those execifications are theoretical values. Add margin depending on its use								<u> </u>	<u> </u>		

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

1-2. SIO0 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-2-1)

	1-4.	J	iou Seriai i	npul/Outpu	il Gilaraci	eristics (wakeup run	Cuon Ena	Dieu) (N	ote 4-2-	1)					
		p	arameter	Symbol	Applicable	Conditions			Specif	ication					
				•	Pin/Remarks		V _{DD} [V]	min	typ	max	unit				
	Seria	Input	Period	tSCK (3)	SCK0 (P12)	• See Fig. 6.		2							
	Serial clock	Input clock	Low level pulse width	tSCKL (3)				1							
	k		High level	tSCKH (3)	-		2.7 to 3.6	1			tCYC				
			pulse width	tSCKHBSY				1			-				
				(3)				2							
	Seria	Dat	a setup time	tsDI (2)	SI0 (P11),	• Specified with respect to rising edge of SIOCLK		0.03							
	al inpu	Data setup time Data hold time		Data hold time		Data hold time		thDI (2)	SB0 (P11)	• See Fig. 6.	2.7 to 3.6				-
	ut	Data hold time						0.03							
	Se	In	Output delay	tdD0 (3)	SO0 (P10),	• (Note 4-2-2)					μs				
	Serial output	Input clock	time		SB0 (P11)					1tCYC	S				
	utput	ock					2.7 to 3.6			+0.05					
	No	to	1 2 1 : These o	nacifications	ro theoretical	values. Add margin depend	inc on ito us			W					
			4-2-2 : Specifie		to the falling	edge of SIOCLK. Specified			time an	output cha	ange				
			20go	and open aran	oatpatoa	5. 555 / Ig. 6.		OK							
									SU.		7				
							ED	ans							
						N) R	ons	Mr						
						ME	$O_{O_{i}}$:0h	•						
						OMIL'S Y	U ₁								
						ECUTACY	R"								
					R	C MILL EC)`								
			1		0)	-0/1/1/E									
				SN											
					V2,	7/1									
		V	1/0		SE										
			En.	7											
	C)		EVICE	CPI											
141				RV											

2-1. SIO1 Serial Input/Output Characteristics (Wakeup Function Disabled) (Note 4-3-1)

	т	Parameter	Countrie 1	Applicable	Conditions			Specif	ication	
	r	rarameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Seri	Inpu	Period	tSCK (4)	SCK1 (P45)	• See Fig. 6.		4			
Serial clock	Input clock	Low level pulse width	tSCKL (4)				2			
^		High level	tSCKH (4)				2			
		pulse width	tSCKHA (4)		• Automatic communication mode • See Fig. 6.	2.7 to 3.6	6			
			tSCKHBSY (4a)		Automatic communication modeSee Fig. 6.		23			tCYC
			tSCKHBSY (4b)		 Mode other than automatic communication mode See Fig. 6. 		4			
	Output clock	Period	tSCK (5)	SCK1 (P45)	• CMOS output selected • See Fig. 6.		4			,5
	t clock	Low level pulse width	tSCKL (5)					1/2	ND	tSCK
		High level pulse width	tSCKH (5)					1/2		iser
			tSCKHA (5)		 Automatic communication mode CMOS output selected See Fig. 6. 	27 to 36	6	ew	101	<u> </u>
			tSCKHBSY (5a)		• Automatic communication mode CMOS output selected • See Fig. 5.	OUR	4	W	23	tCYC
			tSCKHBSY (5b)		Mode other than automatic communication mode See Fig. 6.	R	4			
Serial in	Da	ta setup time	tsDI (3)	SI1 (P44), SB1 (P44)	• Specified with respect to rising edge of SIOCLK		0.03			
input	Da	ta hold time	thD1 (3)	SE	• See Fig. 6.	2.7 to 3.6	0.03			
Serial output	input clock	Output delay	tdDo (4)	SO1 (F43), SB1 (P44)	• (Note 4-3-2)				1tCYC +0.05	μѕ
	Output clock		tdDO (5)		• (Note 4-3-2)	2.7 to 3.6			1tCYC +0.05	

Note 4-3-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-3-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

2-2. SIO1 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-4-1)

Z-Z .	Sion Seriai	iiiput/Outp	at Onaract	oriotioo (Trantoup i ai				'/	
	Parameter	Symbol	Applicable	Conditions			Specif	fication	
	T		Pin/Remarks		V _{DD} [V]	min	typ	max	unit
Seria	Period	tSCK (6)	SCK1 (P45)	• See Fig. 6.		2			
Serial clock	Low level	tSCKL (6)				1			
× ^	pulse width High level	tSCKH (6)	_		2.7 to 3.6	1			tCYC
	pulse width	tSCKHBSY				1			
		(6)				2			
Serii.	ata setup time	tsDI (4)	SI1 (P44),	• Specified with respect to		0.03			
Serial input	ata hold time	thDI (4)	SB1 (P44)	rising edge of SIOCLK • See Fig. 6.	2.7 to 3.6				
=						0.03			
Se Ji	Output delay	tdD0 (6)	SO1 (P43),	• (Note 4-4-2)					μs
Input clock Serial output	time		SB1 (P44)					ltCYC	(C)
Serial output					2.7 to 3.6			+0.05	
								M_{λ}	
Note Note		specifications a ed with respect n the open drai	to the falling	edge of SIOCLK. Specified	s the interva	up to the	1	•	ange
Note	4-4-2 : Specifie	ed with respect	to the falling on output mode	edge of SIOCLK. Specified as e. See Fig. 6.	s the interva	up to the	1	•	ange

3-1. SIO4 Serial Input/Output Characteristics (Wakeup Function Disabled) (Note 4-5-1)

			0 1 1	Applicable	C. Tr			Specif	ication	
		Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Seri	Inp	Period	tSCK (7)	SCK4 (PA2)	• See Fig. 6.		4			
Serial clock	Input clock	Low level	tSCKL (7)				2			
ock	ck	pulse width	~ ~~~~ /=\	-						
		High level pulse width	tSCKH (7)				2			
		puise width	tSCKHA (7)		Automatic communication		_			
					mode • See Fig. 6.	2.7 to 3.6	6			
			tSCKHBSY	-	Automatic communication					tCYC
			(7a)		mode		23			
					• See Fig. 6.					
			tSCKHBSY		Mode other than automatic					
			(7b)		communication mode		4			
	_	D : 1	(CCIV (O)	CCV (DAO)	• See Fig. 6.					
	Output clock	Period	tSCK (8)	SCK4 (PA2)	CMOS output selectedSee Fig. 6.		4		<i>"</i>	
	ut cl	Low level	tSCKL (8)	-	Sec Fig. 0.					
	ock	pulse width	ISCRE (0)			4		1/2	N	
		High level	tSCKH (8)					31.2	-	tSCK
		pulse width						145		
			tSCKHA (8)		Automatic communication		OL			
					mode		6			
					• CMOS output selected	2 7 to 3 6	1,09			
			tSCKHBSY		• See Fig. 6. • Automatic communication) \	0,	- 4P		
			(8a)		mode	11/2	2	M_{i}		tCYC
			(0.11)		CMOS output selected	001	4		23	1010
					• See Fig 6.	$U_{I_{I}}$				
			tSCKHBSY		• Mode other than automatic	211				
			(8b)		communication mode		4			
	_			ari Turi	• See Fig. 6.					
Serial 11	Da	ta setup time	tsDI (5)	SI4 (PA1), SE4 (PA1)	• Specified with respect to rising edge of SIOCLK		0.03			
ll in	Da	ta hold time	thDI (5)	354 (FA1)	• See Fig. 6	2.7 to 3.6				
E .	Du	an hold time		SV		2.7 10 3.0	0.03			
			6	1	7.		0.03			
Sei	Jut	Output delay	tdD0 (7)	SO4 (FA0),	• (Note 4-5-2)					
Serial outpu	mput clock	ume	1	SB14(PA1)					1tCYC	
utt	ock		201						+0.05	μs
			0K,							
*			tdDO (8)	-	• (Note 4-5-2)	2.7 to 3.6				1
	Output clock		(0)		(11010 + 3-2)					
	ıt cle								1tCYC	
	эck								+0.05	

Note 4-5-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-5-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

3-2. SIO4 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-6-1)

	<u>ა-z</u>	5-2. SIO4 Seriai		mpul/Outpi	ut Charact	eristics (wakeup run	Cuon Ena	blea) (N	ote 4-6-	1)			
Prince P		т		Symbol	Applicable	Conditions			Specif	ication			
Low level pulse width ESCKL (9) ESCKH (9) ESCK		Г	arameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit		
Figh level pulse width ISCKH(9) ISCKH(Seri	Inpu	Period	tSCK (9)	SCK4 (P45)	• See Fig. 6.		2					
Figh level pulse width ISCKH(9) ISCKH(al clc	ıt clo	Low level	tSCKL (9)				1					
Security pulse width SCKHBSY (9) SI4 (P44), Specified with respect to rising edge of SIOCLK See Fig. 6. SOME PAGE SIMPLE See Fig. 6. Some Page SIOCLK See Fig. 6. SIMPLE	čk	ck	*	(CONTI (O)	-		2.7 to 3.6	1			tCYC		
Serial output delay time thDI (6) SI4 (P44), SB4 (P44) • See Fig. 6. 2.7 to 3.6 Output delay time thDI (6) SB4(P44) • (Note 4-6-2) Note 4-6-1: These specifications are theoretical values. Add margin depending in its use Note 4-6-2: Specified with respect to the falling edge of SIOCLK. Specified at the interval up to the time an output change begins in the open drain output mode. See Fig. 6.					=		2.7 60 3.0	1					
Data hold time thDI (6) SB4 (P44) rising edge of SIOCLK • See Fig. 6. 2.7 to 3.6 0.03 Output delay time Output delay time Note 4-6-1: These specifications are theoretical values. Add margin depending on its use Note 4-6-2: Specified with respect to the falling edge of SIOCLK. Specified at the interval up to the time an output change begins in the open drain output mode. See Fig. 8			1					2					
Serial Output delay time Unitime Vido (9) SO4 (P43), SB4(P44) (Note 4-6-2) SB4(P44) (SB4(P44)) (SB	Seria	Data setup time		Data setup time		tsDI (6)				0.03			
Note 4-6-1 : These specifications are theoretical values. Add margin depending on its use. Note 4-6-2 : Specified with respect to the falling edge of SIOCLK. Specified as the interval op to the time an output change begins in the open drain output mode. See Fig. 6	al Inn	Data hold time		thDI (6)	SB4 (P44)		2.7 to 3.6						
Output delay time SO4 (P43), SB4(P44) Interest Specifications are theoretical values. Add margin depending on its use state 4-6-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.								0.03					
Note 4-6-1: These specifications are theoretical values. Add margin depending on its use. Note 4-6-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 8.	2	Ir	Output delay	tdD0 (9)	SO4 (P43)	• (Note 4-6-2)					μs		
Note 4-6-1: These specifications are theoretical values. Add margin depending on its use Note 4-6-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.		put c								1+CVC	.C)		
Note 4-6-1: These specifications are theoretical values. Add margin depending on its use Note 4-6-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 3.		lock					2.7 to 3.6						
Note 4-6-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.	-									NY	1		
S DEVICE PLEAFSEN. REPRESEN.				G	O R	COMMITY CONTACTO CONTACTO CONTACTO	U_{n}	KO'					
A Property of the second secon	C		EVIC	PLE	ESE								
	•			Kr									

4-1. SMIICO Simple SIO Mode Input/Output Characteristics

	P	arameter	Symbol	Applicable	Conditions			Specif	ication	ı
				Pin/Remarks		V _{DD} [V]	min	typ	max	uni
Serial clock	Input clock	Period	tSCK (10)	SM0CK (P22)	See Fig. 6.		4			
l clo	cloc	Low level	tSCKL (10)	SWICER (122)	Sec 1 ig. 0.		_			
×	k	pulse width				2.7 to 3.6	2			tCY
		High level pulse width	tSCKH (10)				2			101
	Outp	Period	tSCK (11)	SM0CK (P22)	CMOS output selected		4			
	Output clock	Low level	tSCKL (11)	SWOCK (122)	• See Fig. 6.	2.7 to 3.6		1/2		
	k	pulse width High level	tSCKH (11)							tSC
S	Dat	pulse width ta setup time	tsDI (7)	SM0DA (P23),	Specified with respect to			1/2		
Serial input				SWODA (123),	rising edge of SIOCLK	2.7 to 3.6	0.03			
tμdτ	Dat	ta hold time	thDI (7)		• See Fig. 6.		0.03			
Serial output	Out	tput delay time	tdD0 (10)	SM0DO (P24), SM0DA (P23)	• Specified with respect to falling edge of SIOCLK				N	μ
dino					Specified as interval up	2.7 to 3.6		N	1tCYC	
~					to time when output state	2.7103.0	-02		+0.05	
=										46.
	e 4-7	7-1 : These spe	ecifications ar	e theoretical val	to time when output state starts changing. • See Fig. 6. ues. Add margin depending	g on its use	ous	MA	TIO	

4-2. SMIIC0 I²C Mode Input/Output Characteristics

	Р	arameter		Symbol	Applicable	Conditions			Specif	ication	1
		T		Symoor	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Clock	Input clock	Period		tSCL	SM0CK (P22)	• See Fig. 8.		5			
	lock	Low level	h	tSCLL			2.7 to 3.6	2.5			
		High level		tSCLH				2			Tfilt
	Outp	pulse widt Period	n	tSCLx	SM0CK (P22)	Specified as interval up to		10			
	Output clock	Low level	h	tSCLLx	SWIOCK (F22)	time when output state starts changing.	2.7 to 3.6		1/2		
		High level		tSCLHx		onung.ng.			1/2		tSCL
piı	ns inp	X and SM0D out spike ssion time		tsp	SM0CK (P22) SM0DA (P23)	• See Fig. 8.	2.7 to 3.6		(1	Tfilt
			Input	tBUF	SM0CK (P22) SM0DA (P23)	• See Fig. 8.		2.5		NC	Tfilt
	twee	ease time n start and	Output	tBUFx	SM0CK (P22) SM0DA (P23)	Standard clock mode Specified as interval up to time when output state starts changing If igh-speed clock mode Specified as interval up to time when output state starts changing.	2.7.00 3.6	5.5	SW	110	µsec
			Inpu	tHD;STA	SMOCK (P22) SMODA (P23)	• hen SMHC register control bir, L'CS HDS = 0 • See Fig. 8.	RIN	2.0			TCL
		estart on hold	put		JOTE	• When SMIIC register control bit 12CSHDS = 1 • See Fig. 8.	27. 26	2.5			Tfilt
tin	ne	on hod	0	tHD;STAx	SM0CK (P22) SM0DA (P23)	 Specified as interval up to time when output state starts changing. 	2.7 to 3.6	4.1			
) •	Output	REP		High-speed clock mode Specified as interval up to time when output state starts changing.		1.0			μsec
			Input	tSU;STA	SM0CK (P22) SM0DA (P23)	• See Fig. 8.		1.0			Tfilt
	start tup ti	condition me		tSU;STAx	SM0CK (P22) SM0DA (P23)	Standard clock mode Specified as interval up to time when output state starts changing.	2.7 to 3.6	5.5			
			Output			High-speed clock mode Specified as interval up to time when output state starts changing.		1.6			μsec

Parameter		Cl1	Applicable	Conditions			Specifica	ation	
Parameter		Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
	Input	tSU;STO	SM0CK (P22) SM0DA (P23)	• See Fig. 8.		1.0			Tfilt
Stop condition setup time	Ou	tSU;STOx	SM0CK (P22) SM0DA (P23)	• Standard clock mode • Specified as interval up to time when output state starts changing.	2.7 to 3.6	4.9			
	Output			High-speed clock mode Specified as interval up to time when output state starts changing.		1.1			μsec
	Input	tHD;DAT	SM0CK (P22) SM0DA (P23)	• See Fig. 8.		0			
Data hold time	Output	tHD;DATx	SM0CK (P22) SM0DA (P23)	• Specified as interval up to time when output state starts changing.	2.7 to 3.6	1		1.5	Tfilt
	Input	tSU;DAT	SM0CK (P22) SM0DA (P23)	• See Fig. 8.		l	ZE	2	
Data setup time	Output	tSU;DATx	SM0CK (P22) SM0DA (P23)	Specified as interval up to time when output state starts changing	2.7 to 3.6	itSCL- 1.5Tfilt	emi	101	Tfilt
	Input	tF	SM0CK (P22) SM0DA (P23)	• See Fig. 8.	2.7 to 3.6	OR	MA	300	
SM0CK and SM0DA pins fall time	Output	tF	SMOCK (P22) SMODA (P23)	• hen SMIIC register control bits PSLW = 1, P5V = 1	3	20+0.1Cb		250	ns
	put		TR	* SM0CF, SM0DA por output FAST mode • Cb ≤ 400 pF	3.0 to 3.6			100	

Note 4-8-1 These specifications are incorretical values. And margin depending on its use.

Note 4-8-2: The value of Triit is determined by the values of the register SMICOBRG, bits 7 and 6 (BRP1, BRP0) and the system clock frequency

BRP1	BRP0	Tfilt
	0	tCYC×1
0	1	tCYC×2
1	0	tCYC×3
1	1	tCYC×4

Set bits (BPR1, BPR0) so that the value of Tfilt falls between the following range :

250 $ns \ge Tfilt > 140 ns$

THIS DEV

Note 4-8-3 : Cb represents the total loads (in pF) connected to the bus pins. Cb \leq 400 pF

Note 4-8-4: The standard clock mode refers to a mode that is entered by configuring SMIC0BRG as follows:

250 ns \geq Tfilt > 140 ns BRDQ (bit5) = 1

SCL frequency setting \leq 100 kHz

The high-speed clock mode refers to a mode that is entered by configuring SMIC0BRG as follows :

 $250~ns \geq Tfilt > 140~ns$

BRDQ (bit5) = 0

SCL frequency setting \leq 400 kHz

5-1. SMIIC1 Simple SIO Mode Input/Output Characteristics

	P	Parameter	Symbol	Applicable	Conditions			Specif	fication	1
		T		Pin/Remarks		V _{DD} [V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK (12)	SM0CK (PB4)	See Fig. 6.		4			
clock	clock	Low level pulse width	tSCKL (12)			2.7 to 3.6	2			
		High level pulse width	tSCKH (12)				2			tCY
	Out	Period Period	tSCK (13)	CMOCK (PDA)	. 0.400		4			
	Output clock	Low level	tSCKL (13)	SM0CK (PB4)	• CMOS output selected • See Fig. 6.	2.7 to 3.6		1/2		
	ck	pulse width High level	tSCKH (13)			2.7 10 3.0				tSC
So	Dat	pulse width ta setup time	tsDI (8)	SM0DA (PB5)	Specified with respect to			1/2		
Serial input		ta hold time	thDI (8)	-	rising edge of SIOCLK • See Fig. 6.	2.7 to 3.6	0.03			. (
					-		0.03			
Serial	Ou	tput delay time	tdD0 (12)	SM0DO (PB6), SM0DA (PB5)	• Specified with respect to falling edge of SIOCLK				M,	μ
					Specified as interval up	2.7 to 3.6		171	1tCYC	
Serial output					to time when output state	2.7 10 3.0			+0.05	
	ote ·	4-9-1 : These s	pecifications	are theoretical v	to time when out ut state starts changing. • See Fig. 6. *alues. Add margin dependence.	ling on its us	se.	SON	+0.05	1

5-2. SMIIC1 I²C Mode Input/Output Characteristics

	Р	arameter		Symbol	Applicable	Conditions			Specif	ication	I
				Symoon	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Clock	Input clock	Period		tSCL	SM1CK (PB4)	• See Fig. 8.		5			
	lock	Low level pulse widtl	h	tSCLL			2.7 to 3.6	2.5			
		High level		tSCLH				2			Tfilt
	Outp	pulse width Period	<u>n</u>	tSCLx	SM1CK (PB4)	Specified as interval up to		10			
	Output clock	Low level pulse widtl	h	tSCLLx	. 5.111 (1.2.1)	time when output state starts changing.	2.7 to 3.6		1/2		
		High level pulse widtl		tSCLHx					1/2		tSCI
pir	ns inp	K and SM0D out spike ssion time		tsp	SM1CK (PB4) SM1DA (PB5)	• See Fig. 8.	2.7 to 3.6		(1	Tfilt
			Input	tBUF	SM1CK (PB4) SM1DA (PB5)	• See Fig. 8.		2.5		NI	Tfilt
	twee	ease time n start and	Output	tBUFx	SM1CK (PB4) SM1DA (PB5)	Standard clock mode Specified as interval up to time when output state starts changing If igh-speed clock mode Specified as interval up to time when output state starts changing.	2.7 to 3.6	5.3	SWE	TYO	μsec
			Input	tHD;STA	SM1CK (PE4) SM1DA (PB5)	• When SMIIC register control bit, LYCS HDS = 0 • See Fig. 8. • When SMIIC register control bit	RIN	2.0			Tfili
co: tin	ne	start on hold	Output	thD;\$TAx	SM1CK (PB4) SM1DA (PE5)	time when output state starts changing.	2.7 to 3.6	4.1			μsec
) `		ut	RE!		High-speed clock mode Specified as interval up to time when output state starts changing.		1.0			
			Input	tSU;STA	SM1CK (PB4) SM1DA (PB5)	• See Fig. 8.		1.0			Tfilt
	estart tup ti	condition me	Ou	tSU;STAx	SM1CK (PB4) SM1DA (PB5)	Standard clock mode Specified as interval up to time when output state starts changing.	2.7 to 3.6	5.5			
			Output			High-speed clock mode Specified as interval up to time when output state starts changing.		1.6			μsec

Parameter		Symbol	Applicable	Conditions			Specifica	fication		
Parameter		Pin/Remarks Conditions VDD [V]		min	typ	max	unit			
	Input	tSU;STO	SM1CK (PB4) SM1DA (PB5)	• See Fig. 8.		1.0			Tfilt	
Stop condition setup time	Ou	tSU;STOx	SM1CK (PB4) SM1DA (PB5)	Standard clock mode Specified as interval up to time when output state starts changing.	2.7 to 3.6	4.9				
	Output			High-speed clock mode Specified as interval up to time when output state starts changing.		1.1			μsec	
	Input	tHD;DAT	SM1CK (PB4) SM1DA (PB5)	• See Fig. 8.		0				
Data hold time	Output	tHD;DATx	SM1CK (PB4) SM1DA (PB5)	• Specified as interval up to time when output state starts changing.	2.7 to 3.6	1		1.5	Tfilt	
	Input	tSU;DAT	SM1CK (PB4) SM1DA (PB5)	• See Fig. 8.		1		NC		
Data setup time	Output	tSU;DATx	SM1CK (PB4) SM1DA (PB5)	Specified as interval up to time when output state starts changing.	2.7 to 3.6	1tSCI 1.5T filt	wi		Tfilt	
	Input	tF	SM1CK (PB4) SM1DA (PB5)	• See (1g. 8.	2.7 to 3.6	ons	NA	300		
SM0CK and SM0DA pins fall time	Output	tF	SM1CK (PB4) SM1DA (PB5)	When SMIIC register control bits PSLW = 1, PHV = 1	03	20+0.1Cb		250	ns	
	out		P	• SM0CK, SM0DA port output FAST node • Ch ≤ 400 pF	3 to 3.6			100		

Note 4-10-1: These spoifications are theoretical values. Add mar in depending on its use.

Note 4-10-2: The value of Tfilt is determined by the values of the register SMIC1BRG, bits 7 and 6 (BRP1, BRPO) and the system clock frequency

BRPI	BRP0	Tfilt
0.6	0	tCYC×1
	1	tCYC×2
1	0	tCYC×3
1	1	tCYC×4

THIS DEVIC Set bits (BPR1, BPR0) so that the value of Tfilt falls between the following range:

250 ns \geq Tfilt > 140 ns

Note 4-10-3 : Cb represents the total loads (in pF) connected to the bus pins. Cb \leq 400 pF

Note 4-10-4: The standard clock mode refers to a mode that is entered by configuring SMIC0BRG as follows:

250 ns ≥ Tfilt > 140 ns

BRDQ (bit5) = 1

SCL frequency setting \leq 100 kHz

The high-speed clock mode refers to a mode that is entered by configuring SMIC1BRG as follows:

250 $ns \ge Tfilt > 140 ns$

BRDQ (bit5) = 0

SCL frequency setting \leq 400 kHz

6-1. SLIIC0 Simple SIO Mode Input/Output Characteristics

D		Parameter Symbol		Applicable Conditions				Specification				
	Parameter		Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit		
Serial	Input clock	Period	tSCK (13)	SL0CK (PA4)	See Fig. 6.		4					
clock	clock	Low level pulse width	tSCKL (13)			2.7 to 3.6	2			tCYC		
		High level pulse width	tSCKH (13)				2					
Serial	Data setup time		tsDI (9)	SL0DA (PA5)	rising edge of SIOCLK	0.7.	0.03					
input	Data hold t	ta hold time	thDI (9)		• See Fig. 6.	2.7 to 3.6	0.03					
Serial output	Ou	tput delay time	tdD0 (13)	SL0DO (PA6), SL0DA (PA5)	 Specified with respect to falling edge of SIOCLK Specified as interval up to time when output state starts changing. See Fig. 6. 	2.7 to 3.6		C	1tCYC +0.05	μs		

Note 4-11-1: These specifications are theoretical values. Add margin depending on its use.

6-2. SLIIC1 I²C Mode Input/Output Characteristics

	Do	rameter		Symbol	Applicable Conditions			Specification					
	rai	iameter		Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit		
Clock	Input	Period		tSCL	SL0CK (PA4)	• See Fig. 8.		5					
IOCN	lock	Low level pulse width	1	tSCLL			2.7 to 3.6	2.5			Tfilt		
		High level pulse width	ı	tSCLH				2					
oins i	inpu	and SL0DA at spike ion time		tsp	SL0CK (PA4) SL0DA (PA5)	• See Fig. 8.	2.7 to 3.6			1	Tfilt		
		ase time start and	Input	tBUF	SL0CK (PA4) SL0DA (PA5)	• See Fig. 8.	2.7 to 3.6	2.5			Tfilt		
Start/restart			Input	tHD;STA	SL0CK (PA4) SL0DA (PA5)	• When SMIIC register control bit, I2CSHDS = 0 • See Fig. 8. • When SMIIC register	2.7 to 3.6	2.0		N C	Tfilt		
		ıt	tSU;STA	SL0CK (PA4)	control bit I2CSHDS = 1 • See Fig. 8.		2.5	NE		1			
Resta setup		ondition ne	Input	150,51A	SL0DA (PA5)	See Fig. 8	2.7 to 3.6	1.0	36,	UO.	Tfilt		
Stop		dition	Input	tsu;sto	SLOCK (PA4) SLODA (PA5)	See Fig. 8.	2.7 to 3.6	1.0	5/1/1		Tfilt		
Data	holo	d time	Input Output	tHD:DATx	SLOCK (PA4) SLODA (PA5) SLOCK (PA4) SLODA (PA5)	• See Fig. 2. • Specified as interval up to time when output state starts changing.	2.7 to 3.6	0		1.5	Tfilt		
ò	0		ıt Input	tSU;DAT	SL0CK (PA4) SL0DA (PA5)	• See Fig. 8.		1					
Data	setu	up time	Output	tSU;DATx	SL0CK (PA4) SL0DA (PA5)	Specified as interval up to time when output state starts changing.	2.7 to 3.6	1tSCL- 1.5Tfilt			Tfil		

7. UARTO Operating Conditions at Ta = -40 to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0$ V

Parameter	0 1 1	Applicable	Conditions —		Specification					
	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit		
Transfer rate	UBR0	U0RX (P13), U0TX (P14), U0BRG (P07)		2.7 to 3.6	4		8	tBGCYC		

Note 4-9: tBGCYC denotes one cycle of the baudrate clock source.

8. UART2 Operating Conditions at Ta = -40 to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0$ V

Parameter	0 1 1	Applicable	G IV	Conditions		Specification			
	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit	
Transfer rate	UBR2	U2RX (P16), U2TX (P17),		2.7 to 3.6	8		4096	tBGCYC	

Note 4-10: tBGCYC denotes one cycle of the baudrate clock source.

9. UART3 Operating Conditions at Ta = -40 to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0$ V

Parameter	Symbol	Applicable Pin/Remarks	Conditions			Specif		
		Pili/Remarks		$V_{\rm DD}[V]$	min	typ	max	unit
Transfer rate	UBR3	U3RX (P34),						
		U3TX (P35)		20.05	\mathbb{C}		1000	avia l
				2.7 to 3.6	8	6/1	4096	BGCYC
				CV		5 1		

Note 4-10: tBGCYC denotes one cycle of the baudrate clock source.

■ Pulse Input Conditions at Ta = -4.0 to +85°C, VSS1 = VSS2 = VSS3 = VSS4 = 0 V

Parameter	Symbol	Applicable	Conditions	11/1		Specification		
Parameter		Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
High/low level	τPIH (1)	INTO (P30)	• Interrupt source flag can be sel.					
pulse width	tPIL (1)	INT1 (P31),	• Event inputs for timers 2 and 3					
		IN Γ2 (P32),	are enabled.					
	7	1ЛТЗ (РЗЗ),	5 4 4		_			~~~
	15	INT4 (F20),	X D \	2.7 to 3.6	2			tCYC
		IN 15 (P21),	7//					
		1NT6 (P40),						
	0	INT7 (P41)						
OF	tPIL (2)	RESB	Resetting is enabled.	2.7 to 3.6	10			μs

■ AD Converter Characteristics at Ta = -40 to +85°C, V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0 V

1. 12-bit AD Conversion Mode

		Applicable Pin				Specif	ication	
Parameter	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Resolution	NAD	AN0 (P60)		2.7 to 3.6		12		bit
Absolute accuracy	ETAD	to AN7 (P67), AN8 (P70)	(Note 6-1)	2.7 to 3.6			±16	LSB
Conversion time	TCAD12		Conversion time calculated	3.0 to 3.6	64		115	
		, , ,		2.7 to 3.6	128		230	μs
Analog input voltage range	VAIN			2.7 to 3.6	V_{SS}		v_{DD}	V
Analog port	IAINH		$VAIN = V_{DD}$	2.7 to 3.6			1	
input current	IAINL		VAIN = V _{SS}	2.7 to 3.6	-1			μA

⁻ Conversion time calculation formula : TCAD12 = $\left(\frac{52}{\mathrm{AD}\,division\,ratio}$ +2) × tCYC

2. 8-bit AD Conversion Mode

<u> </u>								
		Applicable Pin				Specif	ication	
Parameter	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Resolution	NAD	AN0 (P60)		2.7 to 3.6		8		bit
Absolute accuracy	ETAD	to AN7 (P67), AN8 (P70)	(Note 6-1)	2.7 to 3.6	10		±1.5	LSB
Conversion time	TCAD8	to AN15 (P77)	Conversion time calculated	3.0 to 3.6	39	20	71	7
		, i		2.7 to 3.6	79		140	μs
Analog input	VAIN	,		2.7 to 3.6	VSS	11.	$v_{ m DD}$	V
voltage range				2.7 10 3.0	2 55	J/J	DD	•
Analog port	IAINH		$VAIN = V_{DD}$	2.7 to 3.6			1	
input current	IAINL		VAIN = V _{SS}	2.7 to 3.6	1-1			μΑ

⁻ Conversion time calculation formula: TCAD8 = $(\frac{52}{\text{AD arvision (att.)}} + 2) \times \text{tCYC}$

Note 6-1. The quantization error (±1/2LSB) is excluded from the absolute accuracy.

Note 6-2: The conversion time refers to the interval from the time a conversion starting instruction is issued the time the compice digital value against the analog input value is loaded in the result register.

The conversion time is twice the normal value when one of the following conditions occurs:

- The first AD conversion is executed in the 12-bit AD conversion mode after a system reset.

The first AD conversion is executed after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode.

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■ Consumption Current Characteristics at Ta = -40 to +85°C, V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0 V

_	typ : 3.3 V								
	_		Applicable	~ "			Specifi	ication	
	Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	Тур	max	unit
N	ormal mode	IDDOP (1)	VDD1	• FmCF = 12 MHz ceramic oscillator					
	onsumption	(-)	=VDD2	mode					
	ırrent		=VDD3	• FmX'tal = 32.768 kHz crystal					
(1)	Note 7-1)		=VDD4	oscillation mode	3.0 to 3.6		5.5	13.0	
				• System clock set to 12 MHz					
				• Internal RC oscillation stopped					
		*****		• 1/1 frequency division mode					
		IDDOP (2)		• FmCF = 10 MHz ceramic oscillator					
				mode • FmX'tal = 32.768 kHz crystal oscillator					
				mode	2.7 to 3.6		5.0	12.0	mA
				System clock set to 10 MHz	2.7 10 3.0		3.0	12.0	
				• Internal RC oscillation stopped					
				• 1/1 frequency division mode					15
		IDDOP (3)		• FmCF = 0 Hz (oscillation stopped)					
				• FmX'tal = 32.768 kHz crystal oscillator				N	
				mode	2.7 to 3.6		0.75	1.8	
				System clock set to internal RC oscillation			Bin		
				• 1/1 frequency division mode		OK			
		IDDOP (4)		• FmCF = 0 Hz (oscillation stopped)					
		12201 (1)		• FmX'tal = 32.768 kHz crystal oscillator	$^{\prime}$ O_{\cdot}	109		$\langle 1 \rangle$	
				mode	27.06	0,,	A.A.	120	
				System clock set to 32.768 kHz	2.7 to 3.6	0	30	120	μΑ
				• Internal RC oscillation stopped	\mathcal{O} .	\cdot O _Z			
				• 1/1 frequency division mode					
			7	RECONTACTOR	111-		Contin	ued on ne	ext page.
				SEC TRU OF					
				RINIFO					
				100/18					
			NO	10 11/1					
		10	; c	SENTATIV					
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	I	1			I	nucu noi	ii picccui	ing page.
		Applicable				Specif	ication	
Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT (1)	VDD1 =VDD2 =VDD3 =VDD4	HALT mode FmCF =12 MHz ceramic oscillator mode FmX'tal = 32.768 kHz crystal oscillation mode System clock set to 12 MHz Internal RC oscillation stopped 1/1 frequency division mode	3.0 to 3.6		1.7	3.5	
	IDDHALT (2)		HALT mode FmCF = 10 MHz ceramic oscillator mode FmX'tal = 32.768 kHz crystal oscillator mode System clock set to 10 MHz Internal RC oscillation stopped 1/1 frequency division mode	2.7 to 3.6		1.5	3.2	mA
	IDDHALT (3)		HALT mode FmCF = 0 Hz (oscillation stopped) FmX'tal = 32.768 kHz crystal oscillator, mode System clock set to internal RC oscillation 1/1 frequency division mode	2.7 to 3 o	on:	NE Pari	0.8	1
	IDDHALT (4)		HALT mode FmCr = 0 Hz (oscillation stopped) Fm Ctal = 32.768 kHz crystal oscillator mode System c ock set to 32.768 kHz Internal RC oscillation stopped 1/1 frequency division mode	2.7 to 3.6	OP	8.5	65	μА
SDE	NCE P	EAR	SENTATIVE			Contin	ued on no	ext page.

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		Applicable				Specif	ication	
Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
HOLD mode consumption current	IDDHOLD (1)	VDD1	HOLD mode • CF1 = V _{DD} or open (external clock mode)	2.7 to 3.6		0.2	45	
	IDDHOLD (2)		HOLD mode • CF1 = V _{DD} or open (external clock mode) • LVD option selected	2.7 to 3.6		1.2	48	
HOLDX mode consumption current	IDDHOLD (3)		HOLDX mode • CF1=V _{DD} or open (external clock mode) • FmX'tal = 32.768 kHz crystal oscillator mode	2.7 to 3.6		4.6	60	μА
	IDDHOLD (4)		HOLDX mode • CF1 = V _{DD} or open (external clock mode) • FmX'tal = 32.768 kHz crystal oscillator mode • LVD option selected	2.7 to 3.6		5.6	63	ES

Note 7-1: The consumption current value includes none of the currents that flow into the output transistor and internal pull-up resistors.

■ F-ROM Programming Characteristics at Ta - +10 to +55°C, V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0 V

	<u>, , , , , , , , , , , , , , , , , , , </u>		<u> </u>		00		
		Applicable			Sp	cification	
Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	mir typ	max	unit
Onboard	IDDFW (1)	VDD1	Microcontroller erase current	7	(0)		
programming current			current is excluded.	2.7 to 3 6		10	mA
Onboard	tFW (1)		• 2K byte crase operation				
programming			Kr MII FO	2.7 to 3.6		25	ms
time	tFW (2)		• 2-byte programming operation				
		No.	7.0-414	2.7 to 3.6		45	μS
THIS DEV	CEP	PRE	SENTA				

■ Power-on Reset (POR) Characteristics at Ta = +40 to +85°C, V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0 V

						Specif	ication	
Parameter	Symbol	Pin/Remarks	Conditions	Option selected voltage	min	typ	max	unit
Por release	PORRL		• Select from option.	2.57V	2.47	2.57	2.72	
voltage			(Note 8-1)	2.87V	2.77	2.87	3.02	
Detction voltage unknown state	POUKS		• See Fig10. (Note 8-2)			0.7	0.95	V
Power supply rise time	PORIS		• Power supply rise time from 0 V to 1.6 V.				100	mS

Note8-1: The POR release level can be selected out of 2 levels only when the LVD reset function is disabled.

Note8-2: POR is in an unknown state before transistors start operation.

■ Low Voltage Detection Reset (LVD) Characteristics

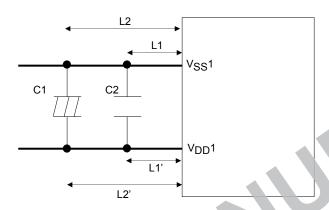
at Ta = +40 to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0 V$

Parameter Symbol Pin/Remarks Conditions Option selected voltage LVD reset LVDET • Select from option. (Note 9-2) • See Fig. 11. LVD hysteresis width
voltage (Note 9-2) LVD hysteresis width Detection voltage unknown state Low voltage detection minimum width (Replay (Note 9-2) • See Fig. 11. (Note 9-2) • See Fig. 11. (Note 9-2) • See Fig. 11. (Note 9-3) • See Fig. 11 (Note 9-3) • See Fig. 12.
width Detection voltage unknown state Low voltage detection minimum width (Replay Control of the position o
voltage unknown state Low voltage detection minimum width (Replay (Note 9-3) • LVDET-0.5 V • See Fig. 12.
detection minimum width (Replay
sensitivity) Note9-1: LVD reset voltage specification values do not include hysteresis voltage.

■ Power Pin Treatment Conditions 1 (VDD1, VSS1)

Connect capacitors that meet the following conditions between the VDD1 and VSS1 pins :

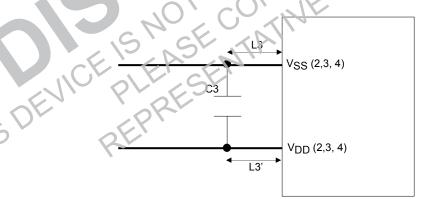
- Connect among the $V_{DD}1$ and $V_{SS}1$ pins and the capacitors C1 and C2 with the shortest possible lead wires, of the same length (L1=L1', L2=L2') wherever possible.
- Connect a large-capacity capacitor C1 and a small-capacity capacitor C2 in parallel. The capacitance of C2 should be approximately $0.1~\mu F$ or larger.
- The V_{DD}1 and V_{SS}1 traces must be thicker than the other traces.



■ Power Pin Treatment Conditions 2 (VDD(2, 3, 4), VSS(2, 3, 4))

Connect capacitors that meet the following condition between the VDD(2, 3, 4) and VSS(2, 3, 4) pins:

- Connect among the VDD(2, 3, 4) and VSS(2, 3, 4) pins and the capacitor C3 with the shortest possible lead wires, of the same length (1.3=L3') wherever possible.
- The capacitance of C3 should be approximately 0.1 μI or larger.
- The VDD(2, 3, 4) and VSS(2, 3, 4) traces must be thicker than the other traces.



■ Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a ON Semiconductor-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

■ Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Resonator

Nominal	N 1 N	9		Circuit	Constant		Operating Voltage	Oscill Stabilizat		
Frequency	Vendor Name	Resonator	C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]	Range [V]	typ [ms]	max [ms]	Remarks
12 MHz		CSTCE12M0G52-R0	(10)	(10)	OPEN	330	2.2 to 3.6	0.02	0.2	C1, C2 integrated type
10 MI	MURATA	CSTCE10M0G52-R0	(10)	(10)	OPEN	680	2.2 to 3.6	0.02	0.2	C1, C2 integrated type
10 MHz		CSTLS10M0G53-B0	(15)	(15)	OPEN	680	2.2 to 3.6	0.02	0.2	C1, C2 integrated type

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after VDD goes above the lower limit level of the operating voltage range (see Figure 4)

■ Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a ON Semiconductor-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

■ Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Resonator

Nominal			Ci	rcuit Consta	nt	Operating Voltage	Oscil _i Stabilizati		10.
Frequency	Vendor Name	or Name Resonator $C3$ $C4$ $Rf2$ $Rd2$ $[V]$ $[PF]$ $[PF$	typ [s]	.<) \\ '. \\ \	Remarks				
32.768 kHz	EPSON TOYOCOM	MC-306	10	Open	330K	2.2 to 3.6	1.0	3.0	CL=7.0pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillator circuit is executed plus the time interval that is required for the oscillation to get stabilized after the HOLD mode is released (see Figure 4).

Note: The traces to and from the components that are involved in oscillation should be kept as short as possible as the oscillation characteristics are affected by their trace pattern.

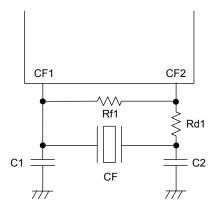


Figure 1 CF oscillator circuit

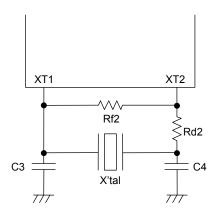
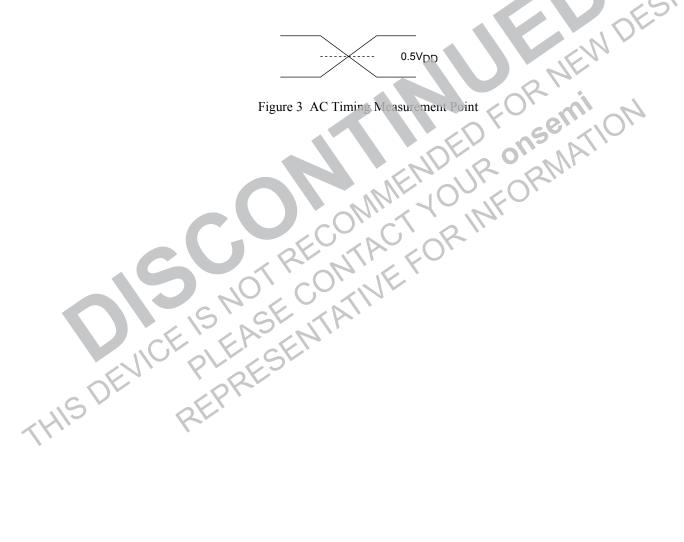
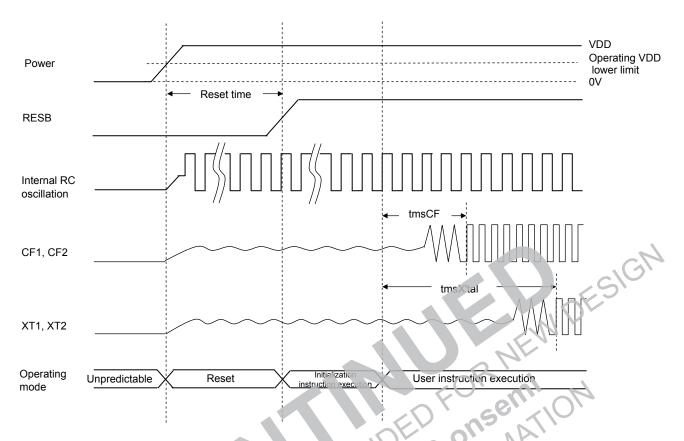
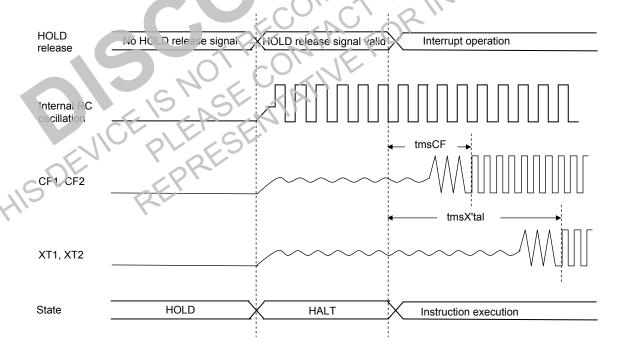


Figure 2 XT Oscillator Circuit



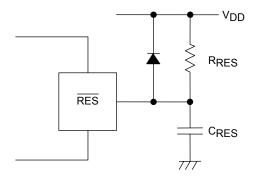


Reset Time and Oscillation Stabilization Time



HOLD Release and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Time Timing Charts

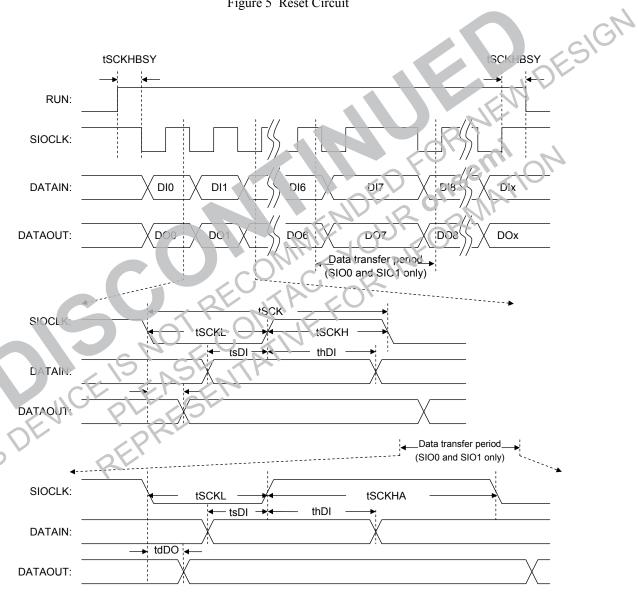


Note:

Reset signal must be present when power supply rises.

Determine the value of C_{RES} and R_{RES} so that the reset signal is present for 10 µs after the supply voltage gets stabilized.

Figure 5 Reset Circuit



^{*} Remarks: DIx and DOx denote the last bits communicated; x = 0 to 32768

Figure 6 Serial I/O Waveforms

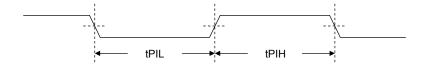
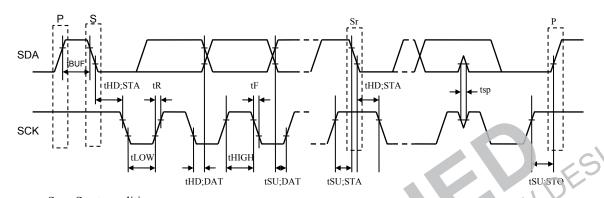


Figure 7 Pulse Input Timing Signal Waveform



S : Start conditionP : Stop conditionSir : Restart condition

Figure 8 I²C Timing

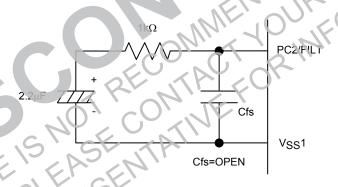


Figure 9 Recommended FILT Circuit

* Take at least 50 ms to oscillation to stabilize after PLL is started.

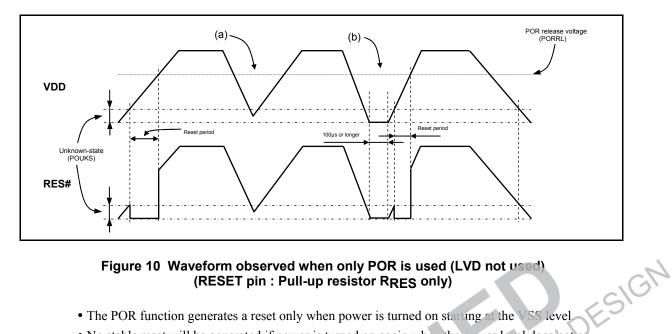


Figure 10 Waveform observed when only POR is used (LVD not used) (RESET pin : Pull-up resistor RRES only)

- The POR function generates a reset only when power is turned on starting at the VSS level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the VSS level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit.
- A reset is generated only when the power level goes down to the VSS level as shown in (b) and power is turned on again after this condition continues for 100µs or longer.

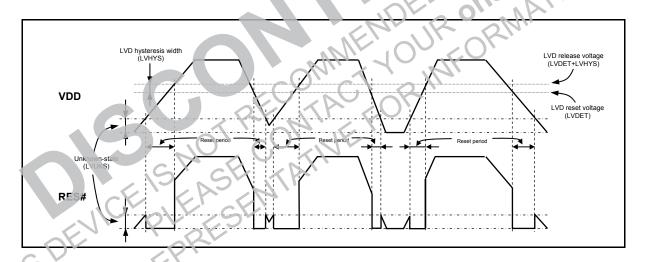


Figure 11 Waveform observed when both POR and LVD functions are used (RESET pin: Pull-up resistor RRES only)

- Resets are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.

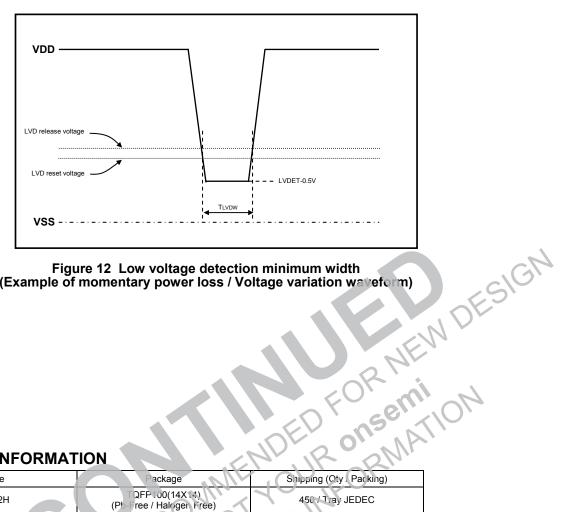


Figure 12 Low voltage detection minimum width (Example of momentary power loss / Voltage variation waveform)

Device	Package	Shipping (Oty), Packing
LC88FC2H0AVUTE-2H	TQFP100(14X14) (Ph-Free / Halogen Free)	450 / Tray JEDEC
	CONC	, OR
	1 RONIC	, FO
	70, CO, MK	
19	GE TAI	
CE	CACHI	
MO PI	15	
OF	P	
S		

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