Highly Integrated Secondary-Side Adaptive USB Type-C Charging Controller with USB-PD with SR Embedded

FAN6390MPX

The FAN6390MPX is a highly integrated, secondary−side power adaptor controller supporting USB Type−C and USB Power Delivery 2.0/3.0. It includes a fully autonomous USB PD state machine which is fully compliant with the latest USB PD 3.0 specification, minimizing design time and cost. Support for the latest Programmable Power Supply (PPS) rules allows for control of voltages from 3.3 V to 21 V and current limits from 1 A to 3 A to meet a wide range of applications and power levels.

To minimize BOM count, the FAN6390MPX includes internal synchronous rectifier control, an NMOS gate driver for VBUS load switch control, as well as Constant Voltage (CV) and Constant Current (CC) control blocks with adjustable internal references. To ensure proper operation of the adaptor, various protections are integrated into the controller including output over−voltage protection, under−voltage protection, external over−temperature protection via NTC, internal over−temperature protection, CC over voltage protection and Cable Fault Protection.

Features

- USB Type−C Rev 1.3 Compatible
- Support 60 W Output Profile
- (PDO: 5 V, 9 V, 15 V, 20 V. APDO: 9 V, 15 V, 20 V)
- Constant Voltage (CV) and Constant Current (CC) Regulation with Two Operational Amplifiers of Open−Drain Type for Dual−Loop CV/CC Control
- Charge Pump Circuit to Enhance SR Driving Voltage for High Efficiency
- Small Current Sensing Resistor (5 mΩ) for High Efficiency
- N−Channel Back to Back MOSFET Control as a Load Switch
- Built−in Output Capacitor Bleeding Function for Fast Discharging
- Precise Voltage & Current Control for Minimum Step Size via 10−bit DAC's
- 10−bit ADC for Monitoring Voltage, Current and Temperature
- Auto Re−start Protection Mode Option to Disable Load Switch for 2 seconds
- Support Protections; Output Over−Voltage Protection, Under−Voltage Protection, External Over Temperature Protection via NTC, Internal Over Temperature Protection, Cable Fault Protection, and CC Lines Over Voltage Protection

Typical Applications

- Battery Chargers for Smart Phones, Feature Phones, and Tablet PCs
- AC−DC Adapters for Portable Devices that Require CV/CC Control

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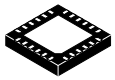
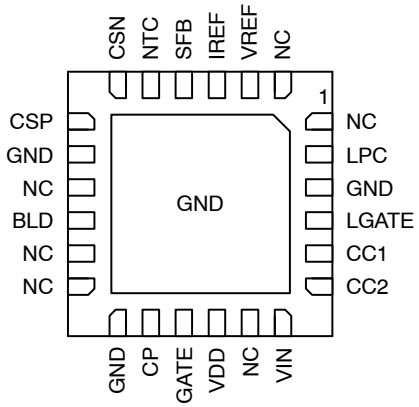


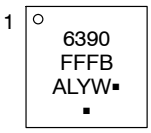
WQFN24
MLP, QUAD
CASE 510BE

PIN CONNECTIONS



(Bottom View)

MARKING DIAGRAM



6390FFFB = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

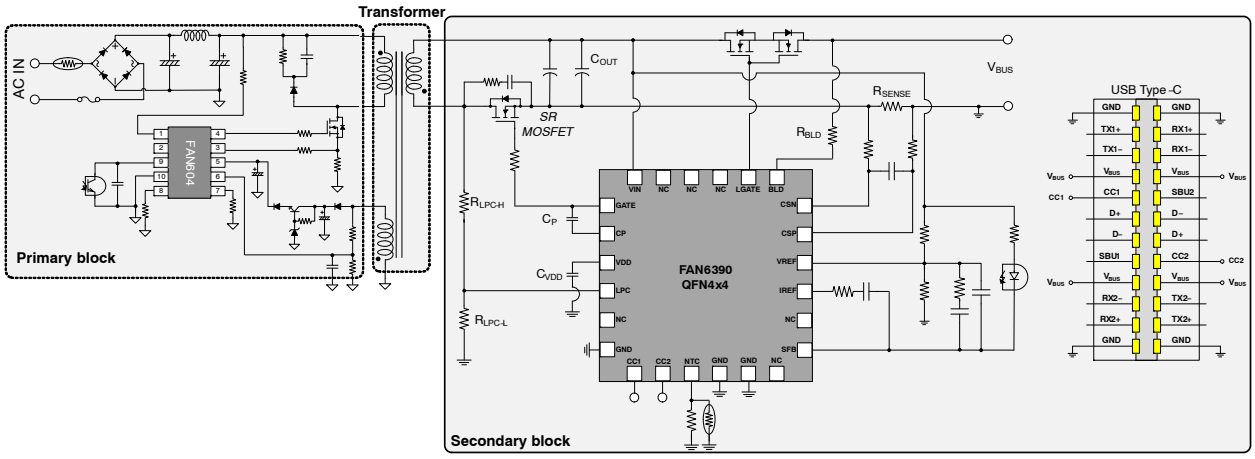


Figure 1. Application Schematic

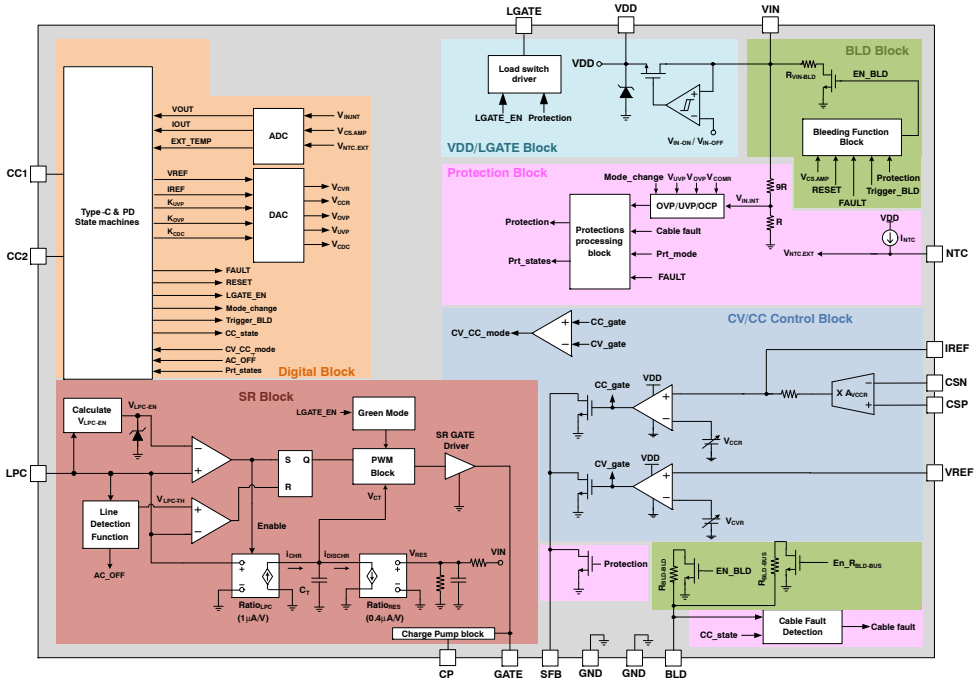


Figure 2. Block Diagram

ORDERING INFORMATION

Part Number	Operating Temperature Range	Package	Packing Method†
FAN6390MPXMPX	−40°C to +125°C	24−Lead, MLP, QUAD, JEDEC MO−220, 4 mm × 4 mm, 0.5 mm Pitch, Single DAP	Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

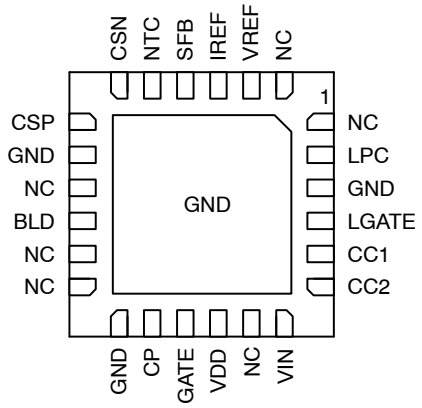


Figure 3. Pin Connections (Bottom View)

Table 1. PIN FUNCTION DESCRIPTION(MLP44)

Pin #	Pin Name	Description
1	NC	No connection
2	LPC	SR control input signal. This pin is used to detect the voltage on the secondary winding during the on time period of the primary MOSFET
3	GND	Ground
4	LGATE	Load switch gate drive signal. This pin is tied to the gate of the load switch
5	CC1	Configuration Channel 1. This pin is used to detect USB Type−C devices and communicate over USB PD when applicable.
6	CC2	Configuration Channel 2. This pin is used to detect USB Type−C devices and communicate over USB PD when applicable.
7	VIN	Output voltage (Input voltage to the FAN6390MPX). This pin is tied to the output of the adapter to monitor its output voltage and supply internal bias.
8	NC	No connection
9	VDD	Internal supply voltage. This pin is connected to an external capacitor.
10	GATE	Gate drive output. Totem−pole output to drive the external SR MOSFET.
11	CP	SR gate charge pump
12	GND	Ground
13	NC	No connection
14	NC	No connection
15	BLD	Bleeder pin. This pin is tied to VBUS after the load switch to discharge VBUS.
16	NC	No connection
17	GND	Ground
18	CSP	Current sensing amplifier positive terminal. Connect this pin directly to the positive end of the current sense resistor with a short PCB trace.
19	CSN	Current sensing amplifier negative terminal. Connect this pin directly to the negative end of the current sense resistor with a short PCB trace.
20	NTC	This pin is used for external temperature detection and protection
21	SFB	Secondary Feedback. Common output of the dual OTA open drain operation amplifiers. Typically an opto−coupler is connected to this pin to provide feedback signal to the primary side PWM controller
22	IREF	Constant Current Amplifying Signal. The voltage level on this point is the amplified current sense signal. This pin is tied to the internal CC loop amplifier's non−inverting input terminal
23	VREF	Output Voltage Sensing Voltage. This pin is used for CV regulation, and it is tied to the internal CV loop amplifier non−inverting input terminal. It is tied to the output voltage resistor divider.
24	NC	No connection

Table 2. MAXIMUM RATINGS (Notes 1, 2)

Rating	Symbol	Value	Unit
VIN Pin Input Voltage	V_{IN}	−0.3 to 26	V
SFB Pin Input Voltage	V_{SFB}	−0.3 to 26	V
BLD Pin Input Voltage	V_{BLD}	−0.3 to 26	V
LGATE Pin Input Voltage	V_{LGATE}	−0.3 to 31	V
VDD Pin Input Voltage	V_{DD}	−0.3 to 6	V
IREF Pin Input Voltage	V_{IREF}	−0.3 to 6	V
VREF Pin Input Voltage	V_{VREF}	−0.3 to 6	V
CSP Pin Input Voltage	V_{CSP}	−0.3 to 6	V
CSN Pin Input Voltage	V_{CSN}	−0.3 to 6	V
LPC pin Input Voltage	V_{LPC}	−0.3 to 6.5	V
GATE Pin Input Voltage	V_{GATE}	−0.3 to 6.5	V
NTC Pin Input Voltage	V_{NTC}	−0.3 to 6	V
CC1 Pin Input Voltage	V_{CC1}	−0.3 to 6	V
CC2 Pin Input Voltage	V_{CC2}	−0.3 to 6	V
CP Pin Input Voltage	V_{CP}	−0.3 to 6.5	V
Power Dissipation (T_A = 25°C)	P_D	0.8644	W
Operating Junction Temperature	T_J	−40 to 150	°C
Storage Temperature Range	T_{STG}	−40 to 150	°C
Lead Temperature, (Soldering, 10 Seconds)	TL	260	°C
Human Body Model, ANSI/ESDA/JEDEC JS−001−2012 (Note 3)	ESD_{HBM}	2	kV
Charged Device Model, JESD22−C101 (Note 3)	ESD_{CDM}	0.5	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All voltage values, except differential voltages, are given with respect to the GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. Meets JEDEC standards JS−001−2012 and JESD 22−C101.

Table 3. THERMAL CHARACTERISTICS (Note 4)

Rating	Symbol	Value	Unit
Thermal Characteristics, Thermal Resistance, Junction−to−Air Thermal Reference, Junction−to−Top	 $R_{\theta JA}$ $R_{\theta JT}$	 122 5	°C/W

4. T_A = 25°C unless otherwise specified.

Table 4. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Input Voltage	V_{in}		20	V
Output Current	I_{out}		5	A
Adjustable Output Voltage (Adjustable Version Only)	V_{out}		20	V
Ambient Temperature	T_A		80	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS

V_{IN} = 5 V, LPC = 1.25 V, LPC width = 2 μs at T_J = −40~125°C, F_{LPC} = 100 kHz, unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VDD SECTION						
Turn−On Valid Threshold Voltage		$V_{DD-valid}$	2.6			V
VIN Operating Voltage at 20V	V_{IN} = 20 V, I_{VDD} = 0 mA	V_{DD}	4.750	5.125	5.500	V
VDD Source Current	V_{IN} = 3.3 V, V_{DD} = 2.9 V	I_{DD}	10			mA
VIN SECTION						
Continuous Operating Voltage (Note 5)		V_{IN-OP}			22.5	V
Operating Supply Current at 5 V	V_{IN} = 5 V, V_{CS} = −25 mV, Rcs = 5 mΩ	$I_{IN-OP-5V}$			10	mA
Operating Supply Current at 20 V (Note 5)	V_{IN} = 20 V, V_{CS} = −25 mV, Rcs = 5 mΩ	$I_{IN-OP-20V}$		8		mA
Turn−On Threshold Voltage	V_{IN} Increases	V_{IN-ON}	2.9	3.2	3.4	V
Turn−Off Threshold Voltage	V_{IN} Decreases after V_{IN} = V_{IN-ON}	V_{IN-OFF}	2.805	2.875	3.005	V
Green Mode Operating Supply Current	V_{IN} = 5.2 V (default), V_{CS} = 0 mV excluding I_{P-CC1} and I_{P-CC2}	$I_{IN-Green}$			1.3	mA
VIN−UVP SECTION						
Ratio V_{IN} Under−Voltage−Protection to V_{IN}	Whole output mode, V_{CS} = 0 mV	K_{IN-UVP}	65	70	75	%
CC Mode UVP Debounce Time		$t_{D-VIN-UVP}$	45	60	75	ms
UVP Blanking Time during Mode Change from Lower Vout to Higher Vout	Whenever does mode change from lower Vout to higher Vout	$t_{BNK-UVP}$	160	200	240	ms
VIN−OVP SECTION						
Ratio V_{IN} Over−Voltage−Protection to V_{IN}	Whole output mode, V_{CS} = 0 mV	K_{IN-OVP}	116.0	121.5	127.0	%
V_{IN} Maximum Over−Voltage−Protection		$V_{IN-OVP-MAX}$	23.5	24.5	25.5	V
OVP Debounce Time		t_{D-OVP}	19	31	43	μs
OVP Blanking Time during Mode Change from Higher Vout to Lower Vout (Note 5)	Vstep ≤ 0.5 V, Vbus ≥ 13 Disabling OVP & SR Gate.	$t_{BNK-OVP}$		7		ms
OVP Blanking Time during Mode Change from Higher Vout to Lower Vout (Note 5)	Vstep ≤ 0.5 V, Vbus < 13 Disabling OVP & SR Gate.	$t_{BNK-OVP}$		19		ms
OVP Blanking Time during Mode Change from Higher Vout to Lower Vout (Note 5)	Disabling OVP & SR Gate. Vstep > 0.5 V, Vbus ≥ 13	$t_{BNK-OVP}$		56		ms
OVP Blanking Time during Mode Change from Higher Vout to Lower Vout	Disabling OVP & SR Gate. Vstep > 0.5 V, Vbus < 13	$t_{BNK-OVP}$		200		ms
CONSTANT CURRENT SENSING SECTION (100% CC)						
Current−Sense Amplifier Gain (Note 5)	R_{CS} = 5 mΩ	A_{V-CCR}		40		V/V
Current threshold on sensing resistor between CSP and CSN at $I_{OUT.CC}$ = 1.00 A	VIN = 3.3 V, 5 V, 20 V	$I_{CS-1.00A}$	0.86	1.00	1.14	A

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Guaranteed by Design

Table 5. ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 5 V, LPC = 1.25 V, LPC width = 2 μs at T_J = −40~125°C, F_{LPC} = 100 kHz, unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
CONSTANT CURRENT SENSING SECTION (100% CC)						
Current threshold on sensing resistor between CSP and CSN at $I_{OUT.CC}$ = 3.00 A	VIN = 3.3 V, 5 V, 20 V	$I_{CS-3.00A}$	2.88	3.00	3.12	A
Current threshold on sensing resistor between CSP and CSN at $\Delta I_{OUT.CC}$ = 50 mA (Note 5)	ΔI_{OTYP} = 50 mA	$I_{CS-STEP}$	48	50	52	mA
CONSTANT CURRENT SENSING SECTION (107% CC)						
Current−Sense Amplifier Gain (Note 5)	R_{CS} = 5 mΩ	A_{V-CCR}		40		V/V
Current threshold on sensing resistor between CSP and CSN at $I_{OUT.CC}$ = 3.21 A	VIN = 5 V	$I_{CS-3.00A}$	3.09	3.21	3.33	A
CONSTANT CURRENT SENSING SECTION (120% OCP)						
Current−Sense Amplifier Gain (Note 5)	R_{CS} = 5 mΩ	A_{V-CCR}		40		V/V
Current threshold on sensing resistor between CSP and CSN at $I_{OUT.CC}$ = 3.60 A	VIN = 3.3 V, 5 V, 20 V	$I_{CS-3.0A}$	3.48	3.60	3.72	A
OCP Debounce Time		$T_{OCP-Debounce}$	50	60	70	ms
OUTPUT CURRENT SENSING SECTION						
Current threshold on sensing resistor between CSP and CSN for enabling bleeding during mode change		$I_{CS-EN-BLD}$			450	mA
Debounce time for enabling bleeding during mode change		$T_{CS-EN-BLD}$			1.0	ms
CONSTANT VOLTAGE SENSING SECTION						
Reference Voltage at 3.3 V	V_{IN} = 3.3 V, V_{CS} = 0 V	$V_{CVR-3.3V}$	0.320	0.330	0.340	V
Reference Voltage at 5.0 V (Power−on reset, default)	V_{IN} = 5.0 V, V_{CS} = 0 V	$V_{CVR-5.0V}$	0.485	0.500	0.515	V
Reference Voltage at 9 V	V_{IN} = 9 V, V_{CS} = 0 V	V_{CVR-9V}	0.873	0.900	0.927	V
Reference Voltage at 15 V	V_{IN} = 15 V, V_{CS} = 0 V	$V_{CVR-15V}$	1.455	1.500	1.545	V
Reference Voltage at 20 V	V_{IN} = 20 V, V_{CS} = 0 V	$V_{CVR-20V}$	1.940	2.000	2.060	V
Reference Voltage of 20 mV step	ΔV_{IN} = 20 mV, V_{CS} = 0 V	$V_{CVR-STEP-20mV}$	1.940	2.000	2.060	mV
CABLE DROP COMPENSATION SECTION						
Cable Compensation Voltage on V_{CVR} for V_{OUT} = 150 mV/A	R_{CS} = 5 mΩ, V_{CS} = −5 mV or R_{CS} = 10 mΩ, V_{CS} = −10 mV	$V_{COMR-CDC}$	13.5	15.0	16.5	mV
FEEDBACK SECTION						
SFB Pin Maximum Sink Current		$I_{SFB-Sink-MAX}$	2			mA
BLEEDER SECTION						
VBUS Leakage Impedance (Note 5)		$R_{BLD-BUS}$	100	171	242	kΩ
VIN Pin Sink Current when Bleeding (Note 5)	Bleeding current on VIN at VIN = 20 V	$I_{VIN\ -Sink}$	300			mA
BLD Pin Sink Current when Bleeding (Note 5)	Bleeding current on BLD at VIN = 20 V	$I_{BLD\ -Sink}$	250			mA
Enable Bleeder Time (Note 5)	Disabling OVP & SR Gate. Vstep ≤ 0.5 V, Vbus ≥ 13	t_{BLD}		7		ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Guaranteed by Design

Table 5. ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 5 V, LPC = 1.25 V, LPC width = 2 μs at T_J = −40~125°C, F_{LPC} = 100 kHz, unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
BLEEDER SECTION						
Enable Bleeder Time (Note 5)	Disabling OVP & SR Gate. Vstep ≤ 0.5 V, Vbus < 13	t_{BLD}		19		ms
Enable Bleeder Time (Note 5)	Disabling OVP & SR Gate. Vstep > 0.5 V, Vbus ≥ 13	t_{BLD}		56		ms
Enable Bleeder Time	Disabling OVP & SR Gate. Vstep > 0.5 V, Vbus < 13	t_{BLD}	160	200	240	ms
OVER TEMPERATURE PROTECTION SECTION						
Current Source on NTC pin	R_{par_110} = 3.293 kΩ	I_{NTC}	55	60	65	μA
Debounce Time for Over Temperature Protection (Note 5)		$T_{NTC-Debounce}$		77.5		ms
CABLE PROTECTION SECTION						
Delay Time Enabling Pollution Detection after Rd is Detached or after Load Switch is Disabled (Note 5)		$t_{POL-EN-Delay}$	9	10	11	ms
Debounce Time for Pollution Detection (Note 5)	$V_{BLD} > V_{POL-TH}$	$t_{POL-Debounce}$	45	50	55	ms
Bleeder Enable Time for Pollution Detection (Note 5)		$t_{BLD-POL}$	9	10	11	ms
Pollution Detection Current on BLD Pin (Note 5)		$I_{POL-DET}$	350	390	450	μA
Supply Voltage of Pollution Detection Current (Note 5)		$V_{SUP-POL-DET}$	0.67	0.74	0.80	V
Pollution Detection Threshold Level (Note 5)	During t_{POL-EN} with open−circuited on BLD	V_{POL-TH}	0.50	0.60	0.65	V
Guaranteed Pollution Impedance (Note 5)		R_{POL}			2	kΩ
PROTECTION OPERATION SPECIFICATION SECTION						
Output Voltage Releasing Latch Mode (Note 5)	$V_{IN} < V_{LATCH-OFF}$, at −5°C and 85°C	$V_{LATCH-OFF}$			1.55	V
Time Duration Disabling Load Switch (Note 5)		$t_{TwoSecondAR.}$		2		s
TYPE−C SECTION						
330 μA Source Current on CC1 Pin	V_{IN} = 5 V, V_{CC1} = 0 V	$I_{P-CC1-330}$	302	330	358	μA
330 μA Source Current on CC2 Pin	V_{IN} = 5 V, V_{CC2} = 0 V	$I_{P-CC2-330}$	302	330	358	μA
Input Impedance on CC1 Pin	V_{IN} = 0 V, Sourcing 330 μA on CC1	$Z_{OPEN-CC1}$	126			kΩ
Input Impedance on CC2 Pin	V_{IN} = 0 V, Sourcing 330 μA on CC2	$Z_{OPEN-CC2}$	126			kΩ
Rd Impedance Detection Threshold on CC1 Pin	V_{IN} = 5 V, V_{CC2} = 0 V, Increasing V_{CC1}	V_{RD-CC1}	2.45	2.60	2.75	V
Rd Impedance Detection Threshold on CC2 Pin	V_{IN} = 5 V, V_{CC1} = 0 V, Increasing V_{CC2}	V_{RD-CC2}	2.45	2.60	2.75	V
UFP Attachment Debounce Time	V_{IN} = 5 V, V_{CC2} = 0 V, Increasing V_{CC1}	$t_{CCDebounce}$	100	150	200	ms
Gate High Voltage at 3.3 V	V_{IN} = 3.3 V	$V_{LGATE-3.3V}$	5.3			V
Gate High Voltage at 20 V	V_{IN} = 20 V	$V_{LGATE-20V}$	23.5			V
Gate High Voltage at $V_{IN-OVP-Max}$	$V_{IN} = V_{IN-OVP-Max}$	$V_{LGATE-OVP-Max}$			31	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Guaranteed by Design

Table 5. ELECTRICAL CHARACTERISTICS (continued)
V_{IN} = 5 V, LPC = 1.25 V, LPC width = 2 μs at T_J = −40~125°C, F_{LPC} = 100 kHz, unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
TYPE−C SECTION						
CC_1 Pin Over−Voltage Protection		$V_{CC1-OVP}$	5.5	5.75	6	V
CC_2 Pin Over−Voltage Protection		$V_{CC2-OVP}$	5.5	5.75	6	V
CC_1/CC_2 OVP Debounce Time		$t_{CC-OVP-Debounce}$			100	μs
Safe Operating Voltage at 0 V		V_{safe0V}	0.66	0.73	0.80	V
OUTPUT DRIVER SECTION						
Output Voltage Low	V_{IN} = 5 V, I_{GATE} = 100 mA	V_{OL}			0.25	V
Output Voltage High	V_{IN} = 3.3 V, C_{iss} = 4.7 nF, C_p = 4.7 nF	V_{OH}	4.0			V
VIN Threshold to Enable Charge Pump (Note 5)		V_{CP-EN}		4.2		V
Rising Time (Note 5)	V_{IN} = 5 V, C_{iss} = 4.7 nF, C_p = 4.7 nF GATE = 1 V ~ 4 V	t_R		63		ns
Falling Time (Note 5)	V_{IN} = 5 V, C_{iss} = 4.7 nF, C_p = 4.7 nF GATE = 4 V~ 1 V	t_F		63		ns
Propagation Delay to OUT High (LPC Trigger (Note 5)	V_{IN}=5 V, GATE=1 V	$t_{PD-HIGH-LPC}$		44		ns
Propagation Delay to OUT Low (LPC Trigger (Note 5)	V_{IN} = 5 V, GATE = 4 V	$t_{PD-LOW-LPC}$		30		ns
Gate Inhibit Time (Note 5)		$t_{INHIBIT}$		1.4		μs
INTERNAL RES SECTION						
Internal RES Ratio (Note 5)	V_{IN} = V_{IN-OFF} ~20 V (N = 6.5~7.5)	K_{RES}		0.110		V/V
VIN Dropping Protection Ratio with Two Cycle	LPC Width = 5 μs, V_{IN} =5 V to 3.5 V	$K_{VIN-DROP}$	60	70	80	%
Debounce time for noise immunity on VIN (Note 5)		$t_{VIN-Debounce}$	1	2	3	μs
Debounce Time for Disable SR when VIN Dropping Protection		t_{SR_OFF}	0	6.5	13	ms
LPC SECTION						
Linear Operation Range of LPC Pin Voltage (Note 5)	V_{IN_OFF} < V_{IN} ≤ 5 V	V_{LPC}	0.4		3.6	V
SR Enabled Threshold Voltage @High−Line	$V_{LPC-HIGH-H-5V}$ = $V_{LPC-TH-H-5V}$ / 0.875	$V_{LPC-HIGH-H-5V}$	0.942	1.069	1.197	V
SR Enabled Threshold Voltage @High−Line	$V_{LPC-HIGH-H-9V}$ = $V_{LPC-TH-H-9V}$ / 0.875	$V_{LPC-HIGH-H-9V}$	1.061	1.196	1.332	V
SR Enabled Threshold Voltage @High−Line	$V_{LPC-HIGH-H-15V}$ = $V_{LPC-TH-H-15V}$ / 0.875	$V_{LPC-HIGH-H-15V}$	1.245	1.433	1.541	V
SR Enabled Threshold Voltage @High−Line	$V_{LPC-HIGH-H-20V}$ = $V_{LPC-TH-H-20V}$ / 0.875	$V_{LPC-HIGH-H-20V}$	1.397	1.554	1.712	V
SR Enabled Threshold Voltage @ Low−Line	$V_{LPC-HIGH-L-5V}$ = $V_{LPC-TH-L-5V}$ / 0.875	$V_{LPC-HIGH-L-5V}$	0.442	0.496	0.550	V
SR Enabled Threshold Voltage @ Low−Line	$V_{LPC-HIGH-L-9V}$ = $V_{LPC-TH-L-9V}$ / 0.875	$V_{LPC-HIGH-L-9V}$	0.561	0.584	0.685	V
SR Enabled Threshold Voltage @ Low−Line	$V_{LPC-HIGH-L-15V}$ = $V_{LPC-TH-L-15V}$ / 0.875	$V_{LPC-HIGH-L-15V}$	0.741	0.817	0.893	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
5. Guaranteed by Design

Table 5. ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 5 V, LPC = 1.25 V, LPC width = 2 μs at T_J = −40~125°C, F_{LPC} = 100 kHz, unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
LPC SECTION						
SR Enabled Threshold Voltage @ Low−Line	$V_{LPC-HIGH-L-12V}$ = $V_{LPC-TH-L-12V}$ / 0.875	$V_{LPC-HIGH-L-20V}$	0.897	0.981	1.065	V
Low−to−High Line Threshold Voltage on LPC Pin	Spec. = (0.70 + 0.02 * V_{IN}) * 2, V_{IN} = 5 V	$V_{LINE-H-5V}$	1.46	1.60	1.74	V
High−to−Low Line Threshold Voltage on LPC Pin	Spec. = (0.65 + 0.02 * V_{IN}) * 2, V_{IN} = 5 V	$V_{LINE-L-5V}$	1.37	1.50	1.63	V
Line Change Threshold Hysteresis (Note 5)	$V_{LINE-HYS-5V}$ = $V_{LINE-H-5V}$ − $V_{LINE-L-5V}$	$V_{LINE-HYS-5V}$		0.1		V
Low−to−High Line Threshold Voltage on LPC Pin	Spec. = (0.70 + 0.02 * V_{IN}) * 2, V_{IN} = 9 V	$V_{LINE-H-9V}$	1.62	1.76	1.90	V
High−to−Low Line Threshold Voltage on LPC Pin	Spec. = (0.65 + 0.02 * V_{IN}) * 2, V_{IN} = 9 V	$V_{LINE-L-9V}$	1.53	1.66	1.79	V
Line Change Threshold Hysteresis (Note 5)	$V_{LINE-HYS-9V}$ = $V_{LINE-H-9V}$ − $V_{LINE-L-9V}$	$V_{LINE-HYS-9V}$		0.1		V
Low−to−High Line Threshold Voltage on LPC Pin	Spec. = (0.70 + 0.02 * V_{IN}) * 2, V_{IN} = 15 V	$V_{LINE-H-15V}$	1.85	2.00	2.15	V
High−to−Low Line Threshold Voltage on LPC Pin	Spec. = (0.65 + 0.02 * V_{IN}) * 2, V_{IN} = 15 V	$V_{LINE-L-15V}$	1.76	1.90	2.04	V
Line Change Threshold Hysteresis (Note 5)	$V_{LINE-HYS-15V}$ = $V_{LINE-H-15V}$ − $V_{LINE-L-15V}$	$V_{LINE-HYS-15V}$		0.1		V
Low−to−High Line Threshold Voltage on LPC Pin	Spec. = (0.70 + 0.02 * V_{IN}) * 2, V_{IN} = 20 V	$V_{LINE-H-20V}$	2.06	2.20	2.34	V
High−to−Low Line Threshold Voltage on LPC Pin	Spec. = (0.65 + 0.02 * V_{IN}) * 2, V_{IN} = 20 V	$V_{LINE-L-20V}$	1.97	2.10	2.23	V
Line Change Threshold Hysteresis (Note 5)	$V_{LINE-HYS-12V}$ = $V_{LINE-H-20V}$ − $V_{LINE-L-20V}$	$V_{LINE-HYS-20V}$		0.1		V
Higher Clamp Voltage		$V_{LPC-CLAMP-H}$	5.4	6.2	7.0	V
LPC Threshold Voltage to Disable SR Gate Switching	V_{IN} = 5 V. LPC = 3 V↑	$V_{LPC-DIS}$	V_{IN} − 0.6			V
Line Change Debounce Time from Low−Line to High−Line	Counts for LPC falling < $V_{LPC-TH-L-5V}$	$t_{LPC-LH-debounce-time}$	13	21	29	ms
Line Change Debounce from High−Line to Low−Line (Note 5)		$t_{LPC-HL-debounce}$		15		μs
INTERNAL TIMING SECTION						
Ratio between V_{LPC} & V_{RES}	V_{IN} = 5 V, F_{LPC} = 50 kHz, K_{RES} = 0.11	$Ratio_{LPC-RES}$	5.40	5.68	5.96	
Minimum LPC Time to Enable the SR Gate @ High−Line	V_{LPC} = 2.5 V	$t_{LPC-EN-H}$	210	285	360	ns
Minimum LPC Time to Enable the SR Gate @ Low−Line	V_{LPC} = 1.25 V	$t_{LPC-EN-L}$	540	705	870	ns
REVERSE CURRENT MODE SECTION						
Reverse Current Mode Entry Debounce Time	V_{IN} = 5 V, V_{LPC} = 0 V	$T_{reverse-debounce}$	270	400	530	ms
Operating Current during Reverse Current Mode	V_{IN} = 5 V, V_{LPC} = 0 V	$I_{OP.reverse}$			2.4	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Guaranteed by Design

Table 5. ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 5 V, LPC = 1.25 V, LPC width = 2 μs at T_J = −40~125°C, F_{LPC} = 100 kHz, unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
BMC TRANSMITTER NORMATIVE REQUIREMENTS						
Unit Internal	1/fBitRate	t_{UI}	3.03	3.33	3.70	μs
Rise Time	C_{VDD} = 4.7 F	$t_{Rise-TX}$	300	500	700	ns
Fall Time	C_{VDD} = 4.7 μF	$t_{Fall-TX}$	300	500	700	ns
Transmitter Output Impedance	Transmitter output impedance at Niquist frequency of USB2.0 low speed (750 kHz) while Source driving the CC line	zDriver	33		75	Ω
Transitions for Signal Detect		$n_{TransitionCount}$	3			
Time Window for Detecting Non−idle		$t_{TransitionWindow}$	12		20	μs
Rx bandwidth Limiting Filter (Digital or Analog)		$t_{RxFilter}$	100			ns
Receiver Input Impedance		zBmcRx	1			MΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Guaranteed by Design

TYPICAL CHARACTERISTICS

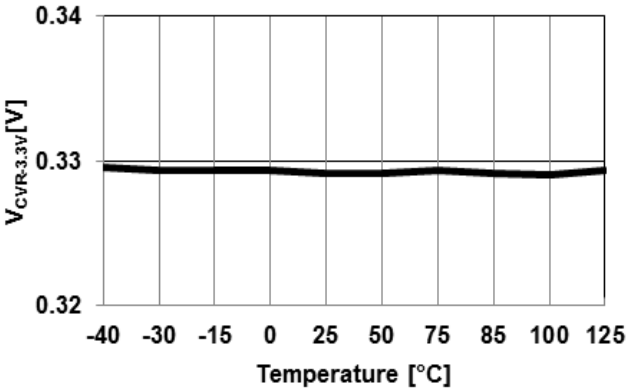


Figure 4. $V_{CVR-3.3V}$ vs. Temperature

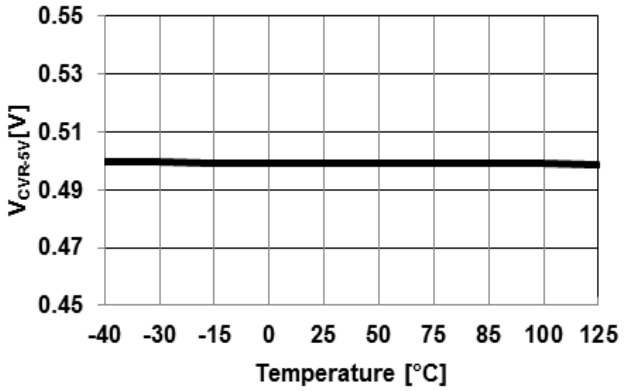


Figure 5. V_{CVR-5V} vs. Temperature

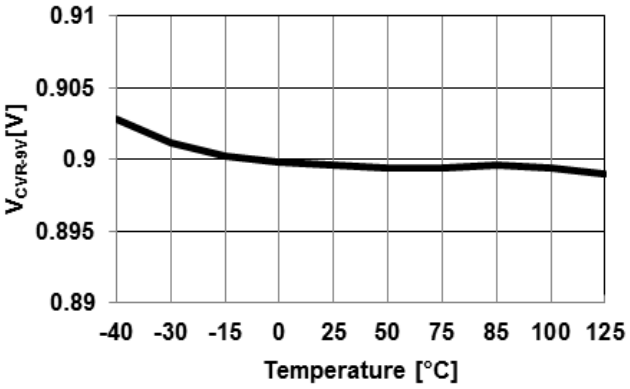


Figure 6. V_{CVR-9V} vs. Temperature

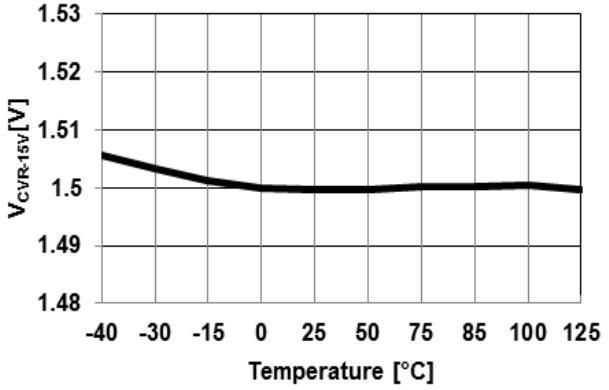


Figure 7. $V_{CVR-15V}$ vs. Temperature

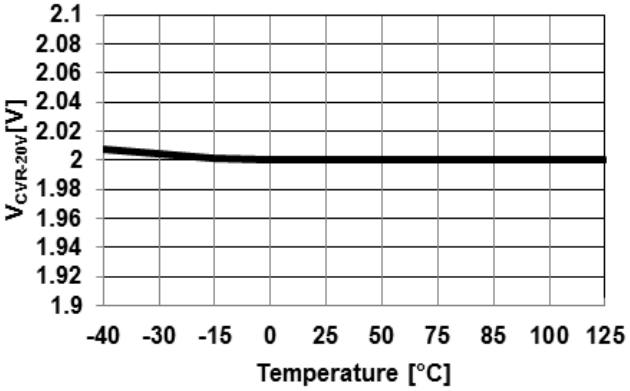


Figure 8. $V_{CVR-20V}$ vs. Temperature

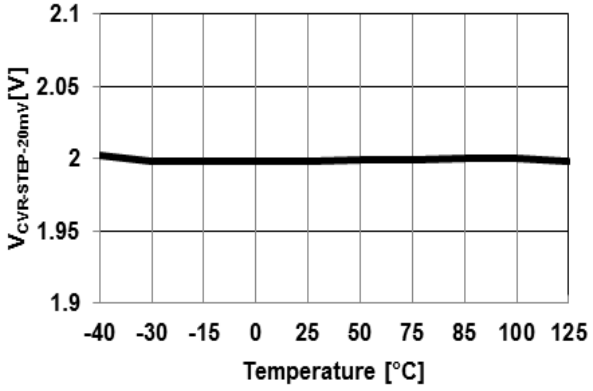


Figure 9. $V_{CVR-STEP-20mV}$ vs. Temperature

TYPICAL CHARACTERISTICS (Continued)

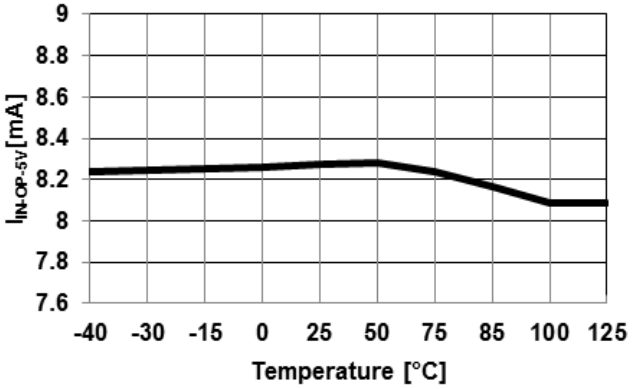


Figure 10. $I_{IN-OP-5V}$ vs. Temperature

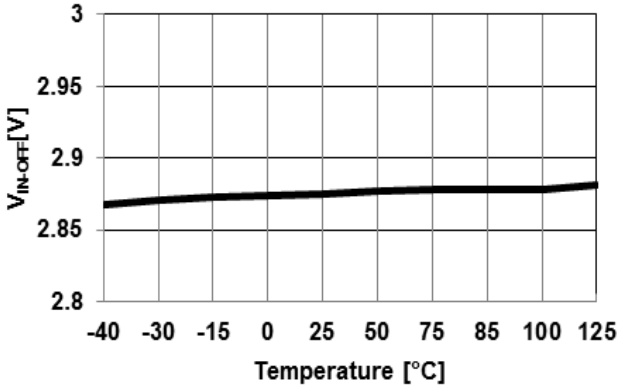


Figure 11. V_{IN-OFF} vs. Temperature

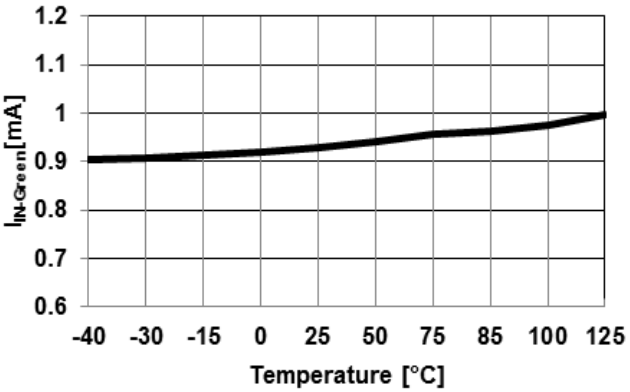


Figure 12. $I_{IN-Green}$ vs. Temperature

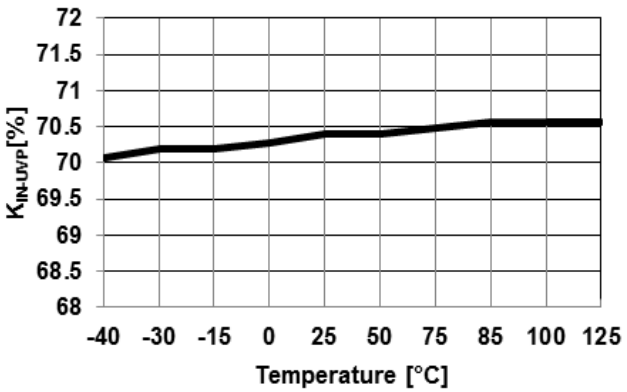


Figure 13. K_{IN-UVP} vs. Temperature

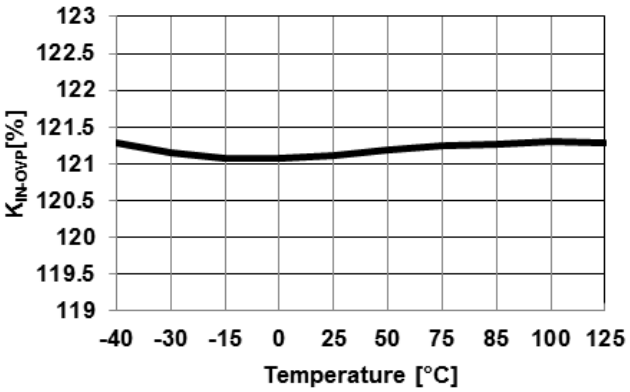


Figure 14. K_{IN-OVP} vs. Temperature

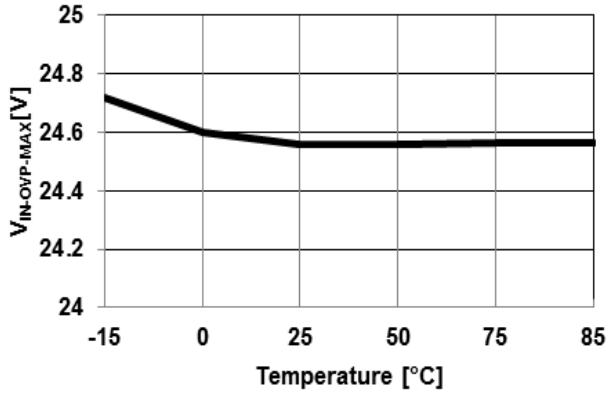


Figure 15. $V_{IN-OVP-MAX}$ vs. Temperature

TYPICAL CHARACTERISTICS (Continued)

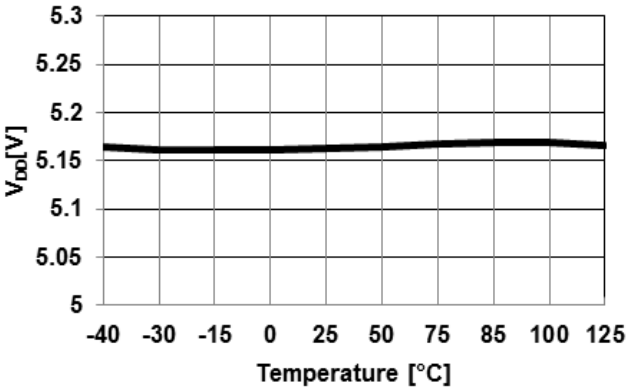


Figure 16. V_{DD} vs. Temperature

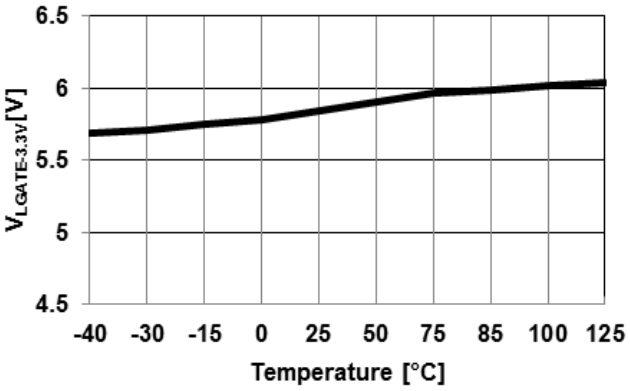


Figure 17. $V_{LGATE-3.3V}$ vs. Temperature

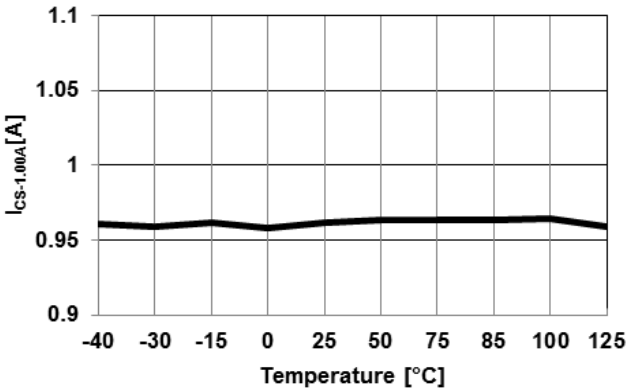


Figure 18. $I_{CS-1.00A}$ at V_{IN} = 20 V vs. Temperature

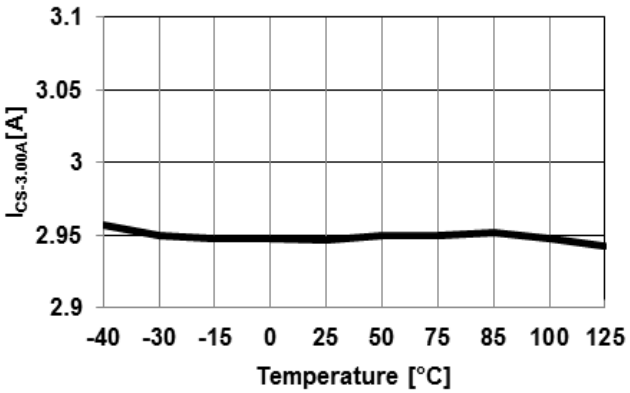


Figure 19. $I_{CS-3.00A}$ at V_{IN} = 20 V vs. Temperature

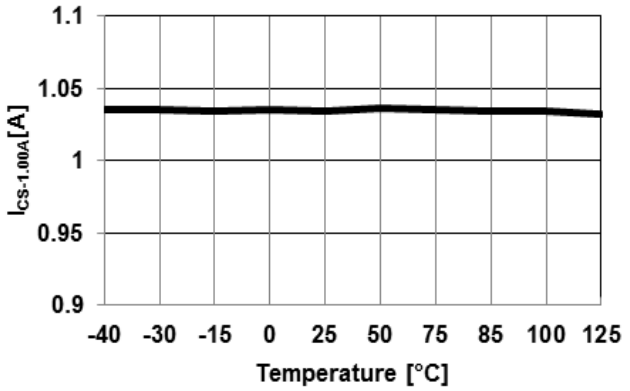


Figure 20. $I_{CS-1.00A}$ at V_{IN} = 3.3 V vs. Temperature

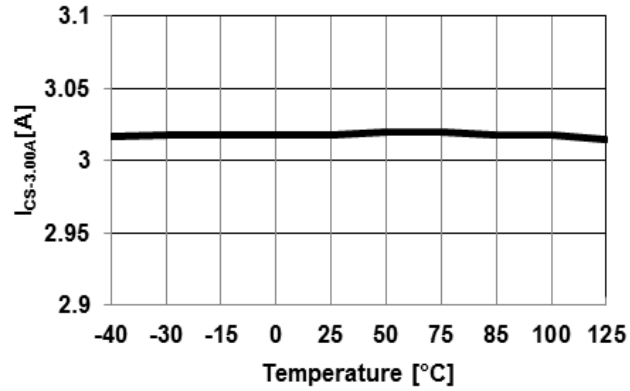


Figure 21. $I_{CS-3.00A}$ at V_{IN} = 3.3 V vs. Temperature

TYPICAL CHARACTERISTICS (Continued)

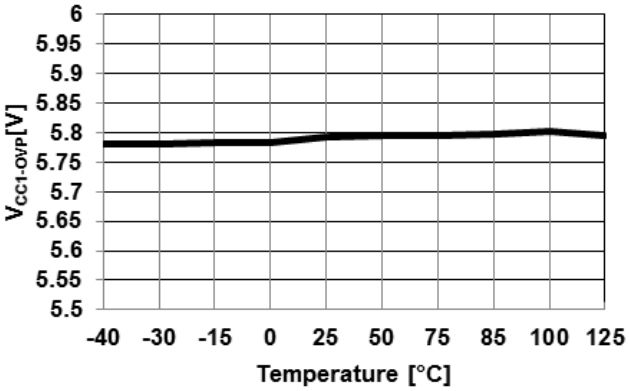


Figure 22. $V_{CC1-OVP}$ vs. Temperature

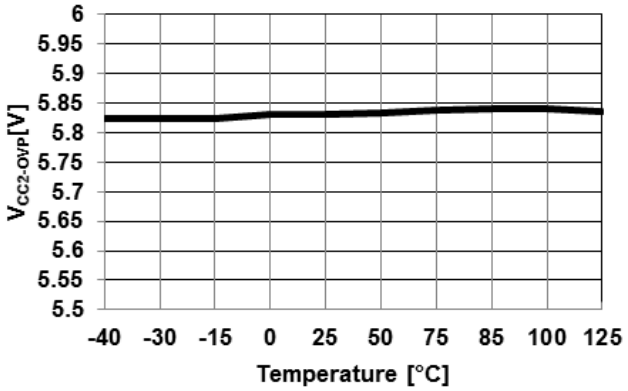


Figure 23. $V_{CC2-OVP}$ vs. Temperature

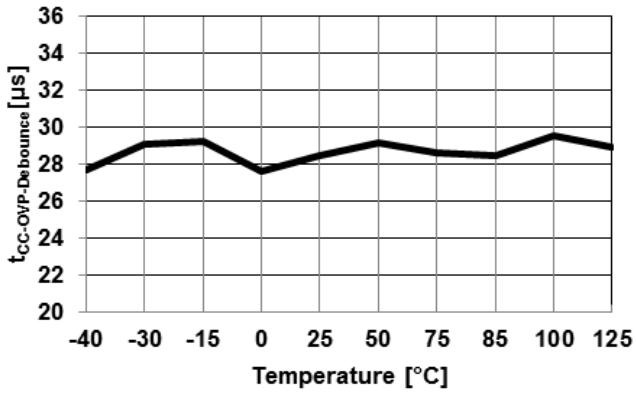


Figure 24. t_{CC-OVP}−Debounce vs. Temperature

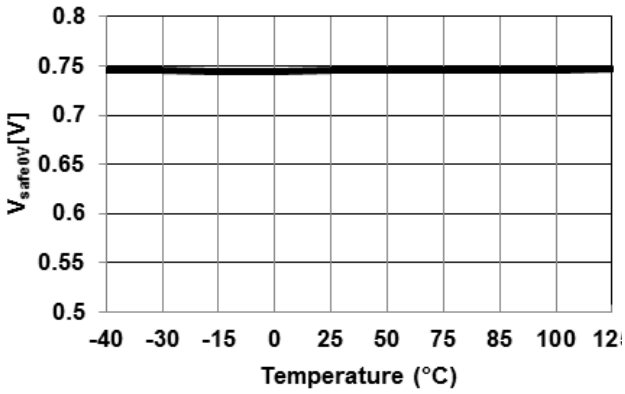


Figure 25. V_{safe0V} vs. Temperature

APPLICATIONS INFORMATION

FAN6390MPX state machine based offers several kinds of trim option to enhance design flexibility as Table 6 shows.

Table 6. SUMMARY TABLE OF ALL KINDS OF TRIM FUNCTION

Function	All Trims	FAN6390MPXMPX Trim
Cable Fault (Note 6)	0: Disabled 1: Enabled	“1” is selected. “0” is for compliance box test.
Internal RES ratio= $1/Ratio_{RRES}$	00: 0.14 (for N_P/N_S = 7.5~10) 01: 0.18 (for N_P/N_S = 9.5~13) 10: 0.11 (for N_P/N_S = 6.5~7.5) 11: 0.10 (for N_P/N_S = 5~6.5) Note: N_P and N_S are primary and secondary transformer turns	“10” is selected.
Cable Compensation for PDO	00: 150 mV/A 01: 50 mV/A 10: 100 mV/A 11: Disabled	“00” is selected. “11” is used for PD compliance box test that additional cable compensation on DFP is no need.
Current Sensing	1: 10 mΩ 0: 5 mΩ	“0” is selected. (Smaller current sensing resistor has better efficiency but could be more expensive. In order to trade off cost and efficiency for flexible design, two kinds of popular current sensing resistors are provided.)
Support PD2.0 or 3.0	0: Enable PD2.0 1: Enable PD3.0	“1” is selected. (FAN6390MPX series support only PDO power profile via PD2.0 trim and PDO plus APDO(PPS) power profile via PD3.0 trim.)
Default 5 V Adjustment	0: 5.0 V 1: 5.2 V	“0” is selected. (Two kinds of default 5 V adjustment for flexible design)
Adjustable Output Profile	8 kinds of output power profile can be selectable as list1.	“000” is selected.
Protection Modes (Note 6)	0: Auto−restart after 2sec 1: Latch protection. System re−start up	“0” is selected.
Output OVP	PDO case and PPS case 00: 120% 01: 125% 10: 130% 11: 115%	“00” is selected.
Output UVP (Note 7)	PDO case: 00: 65% 01: 60% 10: 70% 11: Disable PPS case: disable	“10” is selected.
PDO Current Mode (Note 8)	00: 5 V (107% CC), 9/15/20 V (120 % CC) 01: 5/9/15/20 V (107% CC) 10: 5/9/15/20 V (120% CC)	“00” is selected. “10” is used for PD compliance box test.
Output Power	Output power range from 15 W~60 W 000000: 15 W 000001: 16 W ... 111111: 60 W	“111111” is selected.

6. Function explanation refers to FAN6390MPX application note.
7. Based on compliance spec PPS case is current limit. Output voltage could be lower than the requested PPS voltage command during current limit. In order to operate at current limit region, FAN6390MPX series disable UVP and operates until V_{IN-OFF}.
8. Except of PDO, all APDO power profiles are 100% CC.

Table 7. UP TO 8 KINDS OF OUTPUT POWER PROFILES SELECTED BY TRIM

Power Profile Trim	Output Profile Trim		
	15 W ≤ P ≤ 27 W	**27 W < P ≤ 45 W**	**45 W < P ≤ 60 W**
000	• 5 V • 9 V • 12 V (Note 9) If PD3.0 trim activated • PPS 5 V • PPS 9 V	• 5 V • 9 V • 12 V • 15 V If PD3.0 trim activated • PPS 5 V • PPS 9 V • PPS 15 V	• 5 V • 9 V • 15 V • 20 V If PD3.0 trim activated • PPS 9 V • PPS 15 V • PPS 20 V
001	• 5 V • 5.5 V • 6.0 V • 7.0 V • 8.0 V • 9 V • 10.0 V	• 5 V • 5.5 V • 6.0 V • 7.0 V • 8.0 V • 9 V • 15 V	• 5 V • 5.5 V • 6.0 V • 7.0 V • 9 V • 15 V • 20 V
010	• 5 V • 6.0 V • 7.0 V • 8.0 V • 9 V If PD3.0 trim activated • PPS 5 V • PPS 9 V	• 5 V • 6.0 V • 7.0 V • 9 V • 15 V If PD3.0 trim activated • PPS 9 V • PPS 15 V	• 5 V • 6.0 V • 9 V • 15 V • 20 V If PD3.0 trim activated • PPS 15 V • PPS 20 V
011	• 5 V • 5.5 V • 6.0 V • 6.5 V • 7.0 V • 8.0 V • 9 V	• 5 V • 5.5 V • 6.0 V • 6.5 V • 7.0 V • 9 V • 15 V	• 5 V • 5.5 V • 6.0 V • 6.5 V • 9 V • 15 V • 20 V
100	• 5 V • 5.6 V • 9 V • 11 V	• 5 V • 5.6 V • 9 V • 11 V • 15 V	• 5 V • 5.6 V • 9 V • 11 V • 15 V • 20 V
101	• 5 V • 9 V • 14.5 V	• 5 V • 9 V • 14.5 V • 15 V	• 5 V • 9 V • 14.5 V • 15 V • 20 V
110	• 5 V • 9 V • 11 V	• 5 V • 9 V • 11 V • 15 V	• 5 V • 9 V • 11 V • 15 V • 20 V
111		• 5 V • 9 V • 15 V • 20 V	

9. 12 V can be possible to enable or disable by trim.

USB Type−C Support

The USB Type−C specification defines CC lines (CC1 and CC2) to detect the orientation and roles of a USB Port pair (Source and Sink roles). A source device will provide pull−up currents on the CC lines and the sink will provide a pull−down resistance in order to allow detection of the other when the two are attached. When there is no device attached to either the source or sink device, VBUS must not be powered and should be under 0.8 V (Max). The FAN6390MPX operates as a source−only device and provides control of an NMOS load switch to isolate VIN from VBUS to ensure that VBUS can be discharged completely when required.

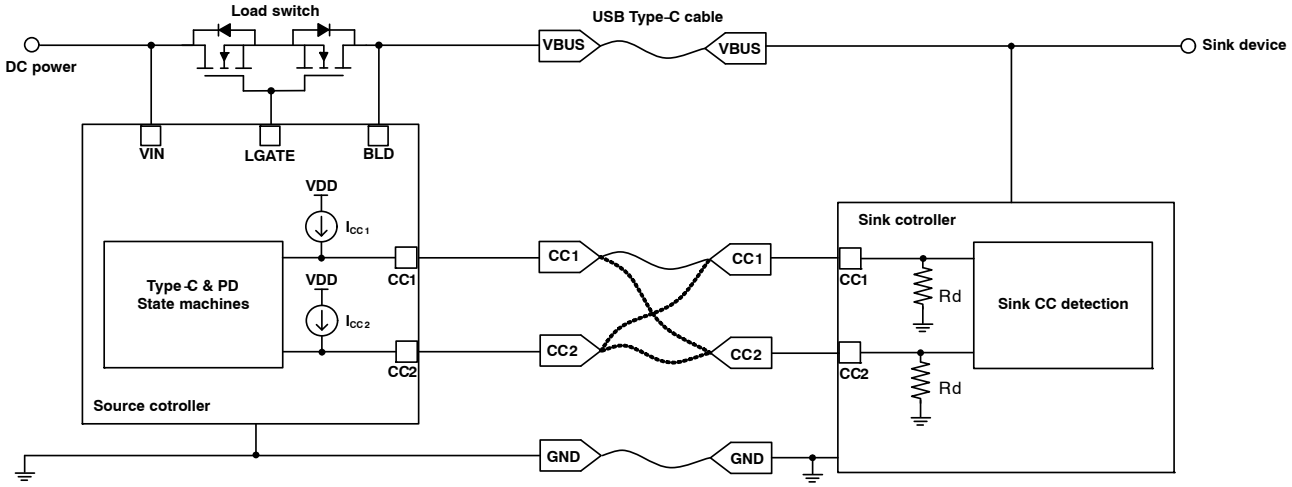


Figure 26. Source Only Device Connecting to Sink Device through Type C Cable

Figure 26 shows a USB Source connected to a USB Sink with a USB Type−C cable. Since there is only one CC signal in a standard USB Type−C cable, one of pull−ups in the USB Source (I_{p-CC1} and I_{p-CC2}) will be terminated with the Rd to ground in the USB Sink, causing a fixed voltage to be developed across the 5.1 kΩ pull−down. The FAN6390MPX monitors the CC line voltages to decide if a Sink is attached or not and the orientation of the USB Type−C cable. If the V_{Rd} voltage is within the attach threshold for $t_{CCDebounce}$ according to the thresholds defined in Table 8, the load switch will be enabled to provide vSafe5V on VBUS. The FAN6390MPX advertises support for 3 A current at the vSafe5V output voltage level.

Table 8. CC VOLTAGES ON SOURCE SIDE – 3.0 A @ 5 V

Detection	Min Voltage	Max Voltage	Threshold
Sink (vRd)	0.85 V	2.45 V	2.60 V
No Connect (vOPEN)	2.75 V		

Figure 27 shows the signal levels and timing for a typical USB Type−C attach on CC1. The Source pull−up currents are enabled on both CC1 and CC2 and the USB cable connects the Rd resistor on the CC1 signal in the Sink device which pulls down the CC1 voltage into the vRd range. Once the FAN6390MPX detects the voltage on CC1 within the vRd range for $t_{CCDebounce}$, the load switch is enabled and vSafe5V is applied on VBUS.

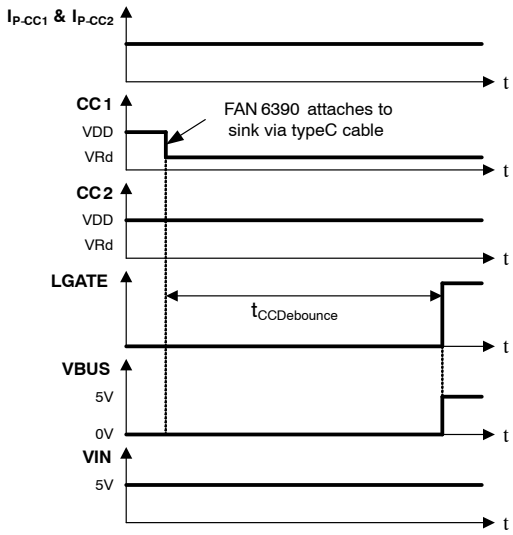


Figure 27. Attach to Sink Device via USB Type−C Cable

USB PD Support

USB Power Delivery (PD) provides a way for a Source and Sink device to negotiate output power settings, allowing for increased power delivery up to 100W. USB PD uses the CC signal that is passed through the USB cable to provide the link between a Source device and a Sink device. In order to communicate properly over the CC signal, all USB PD−capable devices include four major communication components, the Physical Layer, Protocol Layer, Policy Engine and Device Policy Manager as shown in Figure 28.

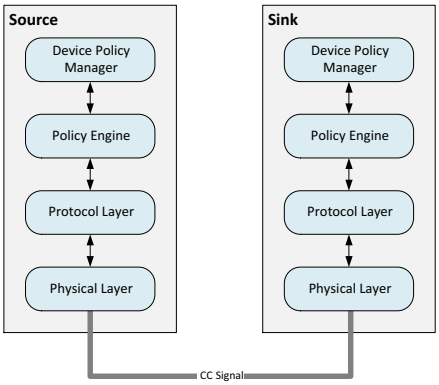


Figure 28. USB PD Communications Stack

The Physical Layer handles the transmission and reception of the bits on the CC signal. All data is first encoded using a 4b5b line code and then transmitted across the CC signal using Biphase Mark Coding (BMC). A 32−bit CRC is also used to protect the data integrity of the data payload.

The Protocol Layer defines how USB PD messages are constructed and used between a Source device and a Sink device. All USB PD messages must follow a strict packet definition and may also include timing requirements based on the type of message. The Protocol Layer is responsible for verifying the timing parameters and handling any communication errors as they arise.

The Policy Engine is responsible for executing the device Local Policy to control its power delivery behavior. The Policy Engine defines a set of message sequences that must be followed for proper operation. All power negotiations are handled by the Policy Engine.

The Device Policy Manager is responsible for overseeing the power supply and managing changes to the Local Policy, including handling of alert and fault conditions. It is also responsible for the Discover Identity messaging to determine the full capabilities of the cabling.

The FAN6390MPX implements all four components of the Source communication stack in hardware to provide a USB PD 3.0 fully−compliant solution without the need for firmware interaction. Control of the Constant Voltage and Constant Current DAC's is integrated into the Policy Engine to provide seamless power transitions between different contracts.

USB PD Power Profiles

The USB PD 3.0 specification defines Power Data Objects (PDO) and Augmented Power Data Objects (APDO) as a way for the Source device to advertise its' power capabilities. Power Data Objects are used to describe well−regulated fixed voltage supplies, poorly regulated power supplies and battery supplies that can be directly connected to VBUS. Augmented Power Data Objects are used to describe a power supply whose output voltage can be programmatically adjusted over the advertised voltage range (Programmable Power Supply or PPS). A Source can advertise a combination of PDO's and APDO's, up to a maximum of 7 total Data Objects. In order to provide a consistent experience across Source devices with the same power rating (PDP), a set of Power Rules was introduced into the USB PD 3.0 specification. The Power Rules provide a set of minimum requirements (PDO's and APDO's) that must be met for a Source device based on the advertised PDP.

The FAN6390MPX can be configured to meet a variety of different USB PD Power Profiles, depending on the application requirements. The default power profile option for the FAN6390MPX is the standard 60W option as shown in Table 9.

Table 9. FAN6390MPX DEFAULT POWER PROFILE

Data Object	Output Voltage	Max Current w/3 A Cable	Current Mode
PDO1	5 V	3.21 A	OC
PDO2	9 V	3.6 A	OCP
PDO3	15 V	3.6 A	OCP
PDO4	20 V	3.6 A	OCP
APDO1	9 V (3.3~11 V)	3 A	CC
APDO2	15 V (3.3~16 V)	3 A	CC
APDO3	20 V (3.3~21 V)	3 A	CC

Constant Voltage Control

In order to regulate adaptive output voltages, the constant voltage control (CV) is implemented. The output voltage is sensed through an external resistor divider. The sensed output voltage is connected to the VREF pin, and it is input the non−inverting input terminal of the internal operational amplifier. The inverting input terminal is connected to the internal voltage reference (V_{CVR}) which can be adjusted according to the requested output voltage. The amplifier and an internal switch operate as a shunt regulator, and the output of the shunt regulator is connected to the external opto−coupler via SFB pin. To compensate output voltage regulation, typically, two capacitors and one resistor are connected between SFB and VREF pins as Figure 29. The output voltage can be derived as calculated by the Equation 1, and the ratio of the resistor divider is 10. The reference (VCVR) for the output voltage is generated by a 10−bit DAC. The minimum resolution is 20 mV to meet PD3.0 compliance spec.

$$V_O = V_{CVR} \cdot \frac{R_{F1} + R_{F2}}{R_{F2}} \qquad \text{(eq. 1)}$$

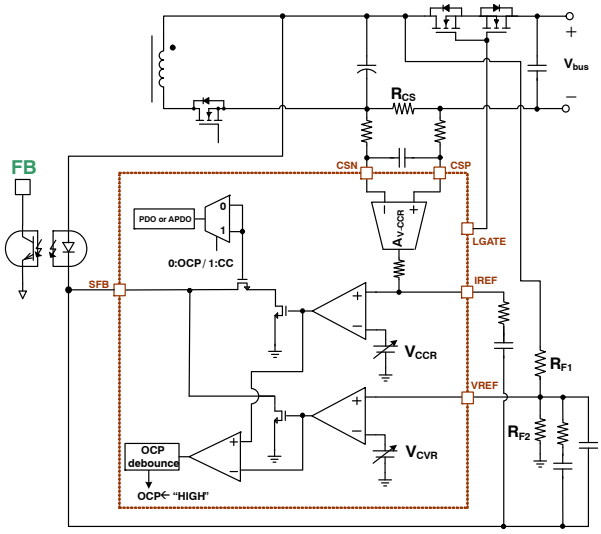


Figure 29. Voltage and Current Sensing Circuits

Constant Current Control

Constant current (CC) control is enabled during USB PD contracts. When CC mode is enabled, the supply will foldback the output voltage as the load increases in order to maintain a fixed output current as shown in Figure 30. Output current is sensed via a current−sense resistor RCS, which is connected between the CSP and CSN pins. The sensed signal is internally amplified, and this amplified voltage is connected to the non−inverting input of the internal operational amplifier. Similar to the constant voltage amplifier circuit, it also plays a role as a shunt regulator to regulate the constant output current. In order to compensate output current regulation, one capacitor and one resistor are connected between the IREF and SFB pins as shown in Figure 29. The constant output current can be calculated using Equation 2. 5mΩ is typically used for the sense resistor.

$$I_{O\_CC} = \frac{1}{A_{V-CCR}} \times \frac{V_{CCR}}{R_{CS}} \qquad \text{(eq. 2)}$$

Since the voltage across the CSP and CSN pins is small, the sensing resistor should be positioned as close as possible to the pins. An RC filter can be added to the pins to reduce the noise seen on the circuit.

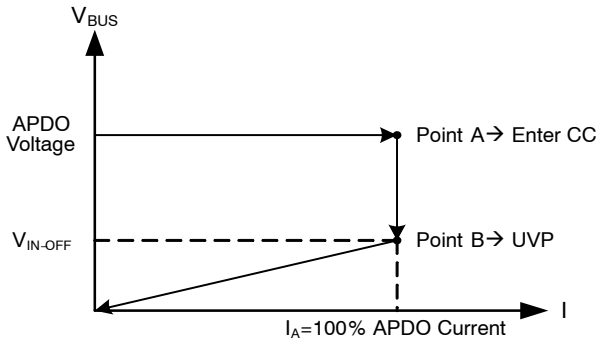


Figure 30. APDO CC Operation

Output Over−Current Protection

Over−Current Protection (OCP) is enabled during USB PD contracts. When OCP mode is enabled the supply will regulate the output voltage until the load current exceeds the OCP threshold, at which point it will cause a fault condition and disable the output voltage as shown in Figure 31. Same as Constant Current Limit Mode, the FAN6390MPX detects the output current via the current−sense resistor R_{CS}, with the difference being the output of the CC amplifier disconnected from the SFB signal. When the load current exceeds the OCP threshold for longer than t_{D-OCP}, Output Over−Current Protection is triggered and the FAN6390MPX enters Auto Restart Mode.

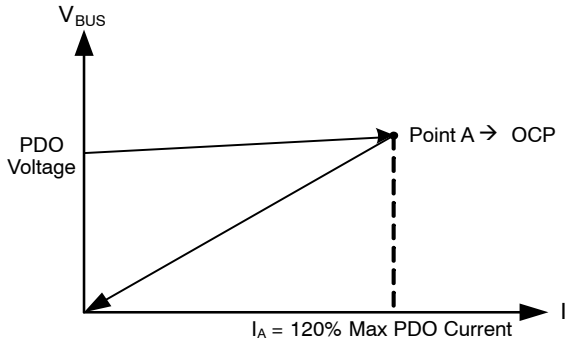


Figure 31. PDO OCP Operation Example

Green Mode Operation

The FAN6390MPX implements green mode operation in order to reduce power consumption during light−load conditions. Green Mode is enabled when there is no valid Sink attached to the Type−C port. During Green Mode operation the Synchronous Rectifier and other block are disabled, reducing the operating current to $I_{IN-Green}$. Green Mode operation is disabled when there is valid Type−C Sink device attached.

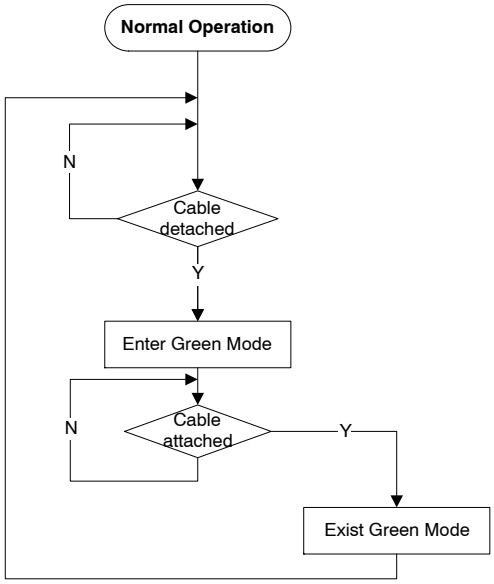


Figure 32. Green Mode Operation

Bleeder Functionality

Bleeder circuits are implemented on the VIN and BLD pins to discharge the output capacitors quickly during mode transitions and to fully discharge VBUS when required. The bleeder circuits in the FAN6390MPX are sized to meet the timing requirements in the USB PD 3.0 specification. Since the output load can discharge the load sufficiently during heavy loads, the bleeder circuits are only enabled during light load conditions ($I_{CS} < I_{CS-EN-BLD}$), The operation of the bleeder circuits is shown in Tables 10, 11 and 12.

Table 10. MODE TRANSITION BLEEDER OPERATION

Step Size	New VBUS	t_{BLD} (typ)	BLD Bleeder	VIN Bleeder	LGATE
≤0.5V	≥13V	7ms	Enabled	Disabled	Enabled
	<13V	19ms			
>0.5V	≥13V	56ms			
	<13V	224ms			

Table 11. DETACH & HARD RESET BLEEDER OPERATION

While VBUS	Final VBUS	t_{BLD} (typ)	BLD bleed	VIN bleed	LGATE
>vSafe5V	vSafe5V	224ms	Enabled	Disabled	Enabled
≤vSafe5V	vSafe0V			Enabled	Disabled

Table 12. PROTECTION MODE BLEEDER OPERATION

Condition	Final VBUS	t_{BLD} (typ)	BLD bleed	VIN bleed	LGATE
Standard Protection	vSafe0V	224ms	Enabled	Enabled	Disabled

Device Protections and Auto Restart Operation

The FAN6390MPX provides Output Over−Voltage Protection, Under−Voltage Protection, Output Over Current Protection, External Over Temperature Protection via NTC, internal Over Temperature Protection, Cable Fault Protection and CC line Over Voltage Protection. When a protection mode is triggered, the load switch is disabled and the VIN and BLD bleeder circuits are enabled to protect the Sink device. During this time, the CC pull−up currents ($I_{p-cc1-330}$ and $I_{p-cc2-330}$) are disabled to indicate to the Sink device that the Source is not ready to provide power. The functionality described is shown in Figure 33. Once the fault conditions are removed, the FAN6390MPX will re−enable the VIN bleeder circuit and begin the auto−restart timer ($t_{TwoSecondAR}$). After the auto−restart timer expires, the CC pull−up currents will be enabled to allow a Sink device to attach as shown in Figure 34.

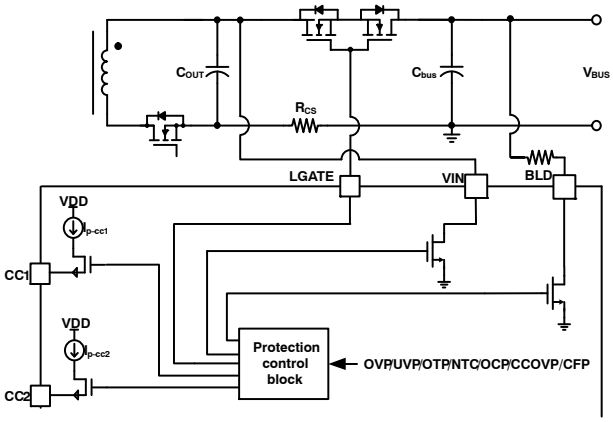


Figure 33. Protection Block Diagram

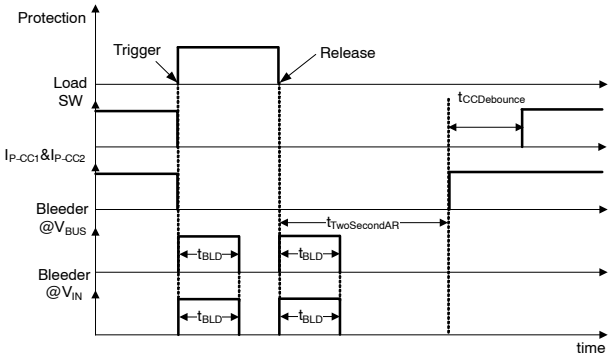


Figure 34. Auto Restart Mode Operation

Output Over−Voltage Protection

Over Voltage Protection (OVP) protects the system of any unexpected high voltage on the VBUS terminals. An OVP fault is triggered when the output voltage exceeds the OVP threshold for longer than t_{D-OVP}. Since the output voltage can change with different USB PD requests, the OVP thresholds will move with the selected contact as shown in

Table 13. In order to avoid mis−triggering an OVP condition during voltage transitions, the OVP circuitry is blanked for $t_{BLK-OVP}$. The maximum OVP threshold is limited to $V_{IN-OVP-MAX}$ regardless of the settings in the table to ensure the voltages stay within the operating range of the FAN6390MPX.

Table 13. OVER−VOLTAGE PROTECTION THRESHOLD

Protocol	PDO or APDO	OVP Threshold
PD2.0	All PDOs	K_{IN-OVP} *PDO
PD3.0	All APDOs	K_{IN-OVP} *APDO

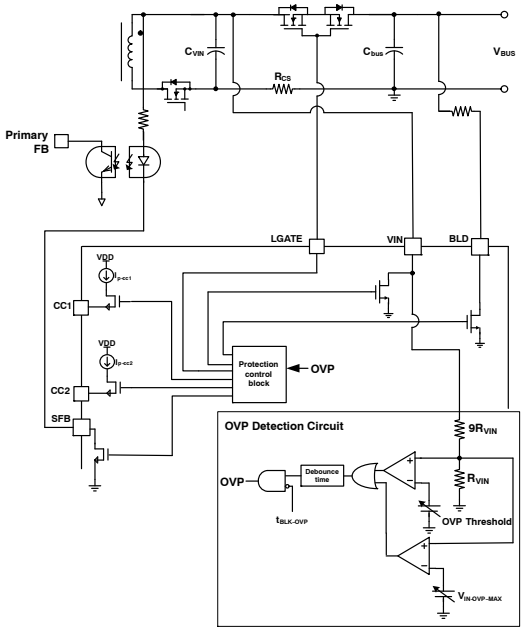


Figure 35. Output Over Voltage Sense Block

Under Voltage Lockout Protection

Under Voltage Lockout (UVLO) protects the system when the output is short−circuited with small impedance. When VIN falls below V_{IN-OFF} threshold, the FAN6390MPX will enter UVLO protection by disabling the load switch, enabling the VIN bleeder and pulling SFB low until VIN falls below $V_{LATCH-OFF}$. Figure 36 illustrates the operation during a UVLO event. The primary side controller restarts switching once VIN falls below $V_{LATCH-OFF}$, but the operation causes a restart due to the voltage being too low on the VS pin on the primary side controller.

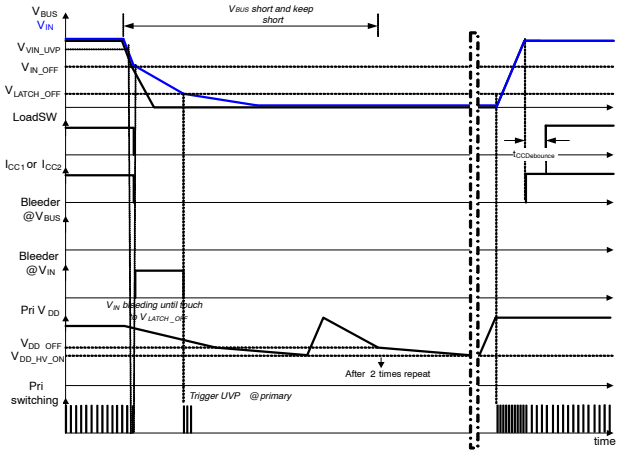


Figure 36. Under Voltage Lockout(UVLO)

External Over Temperature Protection

Higher current charging schemes require hot spot monitoring of the adapter and the Type−C connector temperature. The FAN6390MPX includes an NTC pin to measure the temperature with an external NTC resistor strategically placed on the PCB. Using only a single pin, the FAN6390MPX outputs a known current onto the NTC pin which is terminated to ground through an NTC resistor in parallel with a standard 20kW resistor as shown in Figure 37. The resulting voltage on the NTC pin is then converted to a temperature using the internal ADC and is used to report the current temperature via USB PD messaging as well as compare the temperature against an over−temperature warning and fault thresholds. When the temperature exceeds the Warning threshold, a USB PD Alert message will be sent to the Sink to indicate that the temperature is close to causing a fault as shown in Figure 38. If the temperature exceeds the Fault threshold for longer than $T_{NTC-Debounce}$, a USB PD Alert message will be sent indicating a Fault and the device will enter Auto Restart Mode. Table 14 shows the warning and protection thresholds which may vary slightly according to tolerance of R_p, R_{NTC} and I_{NTC}.

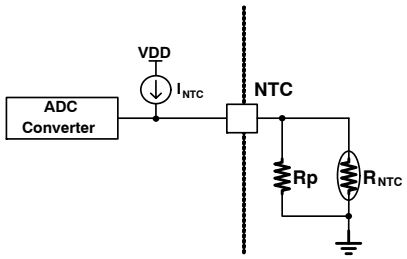


Figure 37. NTC Circuit Diagram

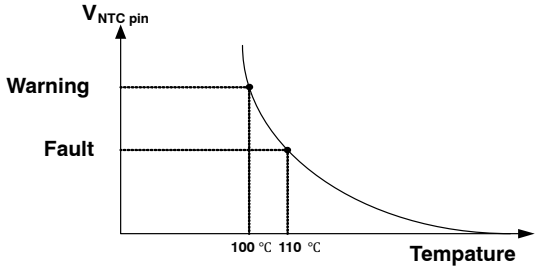


Figure 38. NTC vs. Temperature

Table 14. EXTERNAL OVER TEMPERATURE PROTECTION THRESHOLD

Message	Threshold	Setting
Warning	100°C	R_p=20k Ω@25°C R_{NTC}=100k Ω±1%@25°C ($B_{25/50}$=4300 k±1%)
Fault	110°C	

Internal Over Temperature Protection

The FAN6390MPX also implements internal over temperature protection through an internal temperature sensing circuit. Once the internal temperature exceeds the fault protection threshold of 140℃, the FAN6390MPX sends an Alert indicating an Fault and the device will enter Auto Restart Mode.

Cable Fault Protection

In order to avoid the cable line melting caused by the pollution such as low impedance across ground to BUS. FAN6390MPX implements USB BUS line impedance detection. Before $t_{CCDebounce}$ which is debonce time detecting cable attach status, load switch is not turned on and FAN6390MPX start Bus line impedance detecting. If output is low impedance under 2 kΩ, FAN6390MPX will enter Auto Restart Mode so the load switch will not turn on. No power deliver to output ensure system safety.

CC Signal Over−Voltage Protection

The USB Type−C CC pins are located physically close to VBUS on the connector and could be shorted to VBUS via conductive materials as shown in Figure 39. This not only impacts PD protocol communication, but possibly damages the CC pins because of high VBUS voltages. The FAN6390MPX attempts to protect against damaging the CC pins by implementing Over−Voltage−Protection on the CC pins. The voltage on the CC1 and CC2 pins is continuously monitored, if the voltage increases above $V_{CC1-OVP}$ or $V_{CC2-OVP}$ for longer than $V_{CC-OVP-Debounce}$, the CC Over−Voltage Protection is triggered and the device enters Auto Restart Mode.

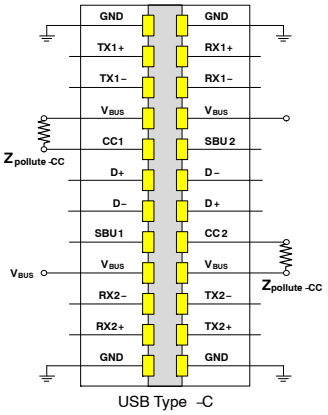


Figure 39. CC1/CC2 Short−circuited with Impedance

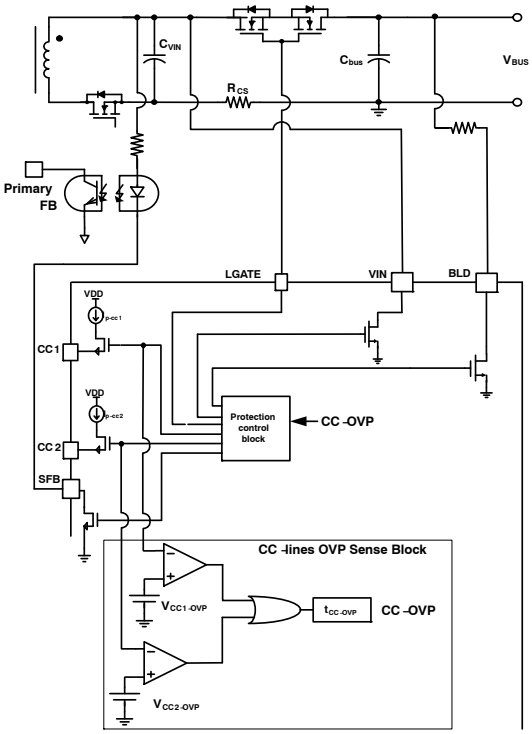


Figure 40. CC OVP Sensing Block Diagram

Charge Pump for Synchronous Rectifier (SR)

Generally, TA SR driving voltage is powered from V_{DD} derived from system V_{BUS} which drives internal circuits and SR MOSFET through GATE pin. The GATE driving voltage can't be higher than V_{BUS}. In order to achieve adapter charging high efficiency at low output voltage and high output current application, a new way to boosting GATE pin voltage for Low Side SR is as .

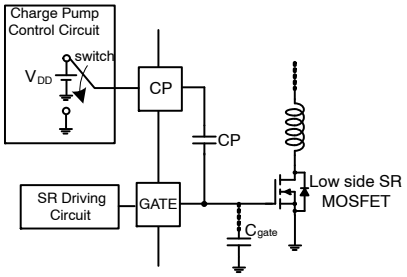


Figure 41. Charge Pump Control Circuit

While V_{IN} < 4.2 V (typ.), FAN6390MPX enable charge pump circuit to have higher driving voltage V_{OH} for efficiency. During t_{BNK} the switch in side Charge Pump Control Circuit will switch to GND in order to have CP be charged via SR Driving Circuit. After blanking time, the switch will connect to V_{DD} to boost V_{OH}. The V_{OH} will be clamped to ensure the voltage no higher than pin maximum rating to ensure driving circuit safe operation as Figure 42. Basically, proper CP capacitance is needed to achieve better system efficiency. This capacitance value should be less than 10 nF and should be adjusted depending on the MOSFET input capacitance which is needed to considered as well. The design guideline can be refer to FAN6390MPX application note.

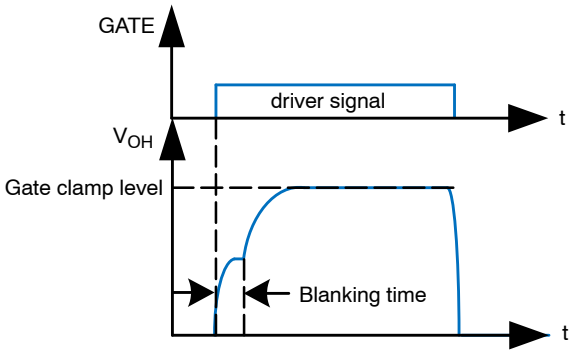


Figure 42. Timing Flow of Charge Pump

Protections Threshold Summary

Table 15 gives an overview of the available protections.

Table 15. OVERVIEW OF PROTECTIONS

Protection	PDO Threshold	APDO Threshold
Under Voltage Lockout(UVLO)	V_{IN-OFF}	
Output Over−Voltage Protection(OVP)	120% (typ.)	
Output Under−Voltage Protection(UVP)	70% (typ.)	V_{IN-OFF}
Output Over−Current Protection(OCP)	120% (typ.)	Non (Note 10)
CC Lines Over−Voltage Protection(CC−OVP)	5.75 V (typ.)	
External Over Temperature Protection	Warning:100°C (typ.) (Note 11) Fault:110°C (typ.) (Note 11)	
Internal Over Temperature Protection	Fault:140°C (typ.) (Note 11)	

10. APDO always works in CC mode
11. Based on the external components R_p = 20 kΩ @ 25°C and R_{NTC} = 100 kΩ ±1% @ 25°C ($B_{25/50}$ = 4300 k ±1%) and I_{NTC} = 60 μA (typ.)

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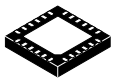
DATE 02 OCT 2013



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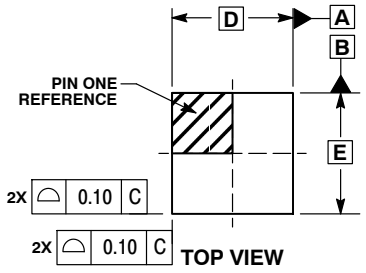
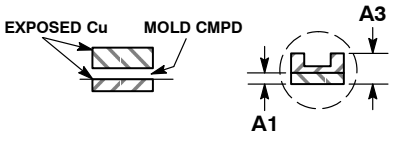
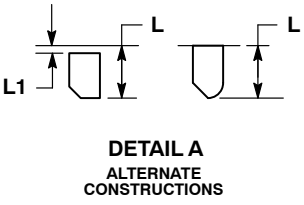
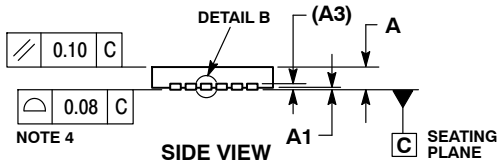
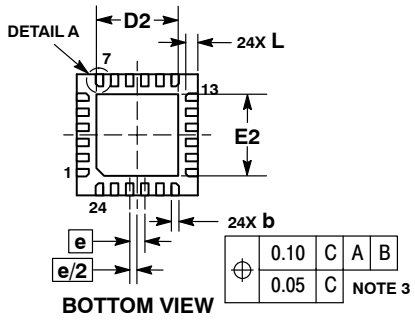






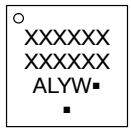




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.60	2.80
E	4.00 BSC	
E2	2.60	2.80
e	0.50 BSC	
L	0.35	0.45
L1	0.00	0.15

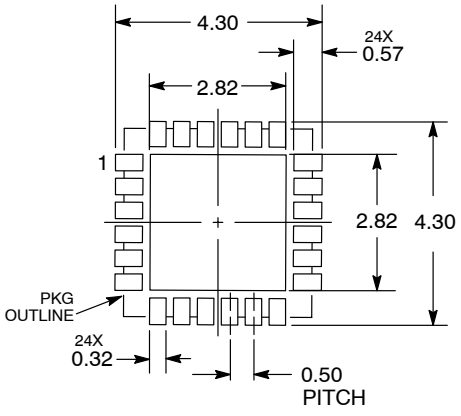
GENERIC MARKING DIAGRAM*



XXXXXX= Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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