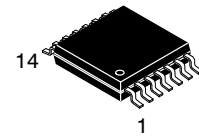


# Low Voltage Quad 2-Input NAND Gate with 3.6 V Tolerant Inputs and Outputs

## 74ALVC00



TSSOP-14, WB  
 CASE 948G

### Description

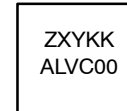
The ALVC00 contains four 2-input NAND gates. This product is designed for low voltage (1.65V to 3.6V)  $V_{CC}$  applications with I/O compatibility up to 3.6V.

The ALVC00 is fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

### Features

- 1.65 V to 3.6 V  $V_{CC}$  supply operation
- 3.6 V Tolerant Inputs and Outputs
- $t_{PD}$ 
  - ◆ 3 ns max for 3.0 V to 3.6 V  $V_{CC}$
  - ◆ 3.5 ns max for 2.3 V to 2.7 V  $V_{CC}$
  - ◆ 4.4 ns max for 1.65 V to 1.95 V  $V_{CC}$
- Power-off High Impedance Inputs and Outputs
- Uses Patented Quiet Series M noise/EMI reduction circuitry
- Latch-up conforms to JEDEC JED78
- ESD Performance:
  - ◆ Human body model > 2000 V
  - ◆ Machine model > 250 V

### MARKING DIAGRAM



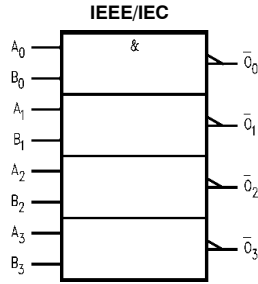
- Z = Assembly Plan Code
- XY = Date Code (Year & Week)
- KK = Lot Run Traceability Code
- ALVC00 = Specific Device Code

### ORDERING INFORMATION

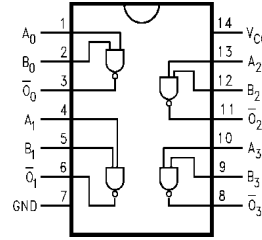
See detailed ordering and shipping information on page 4 of this data sheet.

# 74ALVC00

## Logic Symbol



## Connection Diagram



## Pin Description

Pin Names	Description
$A_n, B_n$	Inputs
On	Outputs

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
$V_{CC}$	Supply Voltage	-0.5 to +4.6	V
$V_I$	DC Input Voltage	-0.5 to 4.6	V
$V_O$	Output Voltage (Note 2)	-0.5 V to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current, $V_I < 0$ V	-50	mA
$I_{OK}$	DC Input Diode Current $V_O < 0$ V	-50	mA
$I_{OH}/I_{OL}$	DC Output Source/Sink Current	$\pm 50$	mA
$I_{CC}$	DC Ground Current per Supply Pin	$\pm 100$	mA
$T_{STG}$	Storage Temperature	-65 to +150	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.
2.  $I_O$  Absolute Maximum Rating must be observed, limited to 4.6 V.
3. Floating or unused control inputs must be held HIGH or LOW.

## RECOMMENDED OPERATING CONDITIONS (Note 3)

Symbol	Parameter	Min.	Max.	Unit
-	Power Supply Operating	1.65	3.65	V
$V_I$	Input Voltage	0	$V_{CC}$	V
$V_O$	Output Voltage	0	$V_{CC}$	V
$T_A$	Free-Air Operating Temperature	-40	+85	$^{\circ}\text{C}$
Lit/LiV	Minimum Input Edge Rate, $V_{IN} = 0.8$ V to 2.0 V, $V_{CC} = 3.0$ V	-	5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# 74ALVC00

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> (V)	Min.	Max.	Unit
V <sub>IH</sub>	HIGH Level Input Voltage		1.65–1.95 2.3–2.7 2.7–3.6	0.65 × V <sub>CC</sub> 1.7 2.0	– – –	V
V <sub>IL</sub>	LOW Level Input Voltage		1.65–1.95 2.3–2.7 2.7–3.6	– – –	0.35 × V <sub>CC</sub> 0.7 0.8	V
V <sub>OH</sub>	HIGH Level Output Voltage	I <sub>OH</sub> = –100 μA	1.65–3.6	V <sub>CC</sub> – 0.2	–	V
		I <sub>OH</sub> = –4 mA	1.65	1.2	–	
		I <sub>OH</sub> = –6 mA	2.3	2.0	–	
		I <sub>OH</sub> = –12 mA	2.3	1.7	–	
			2.7 3.0	2.2 2.4	– –	
I <sub>OH</sub> = –24 mA	3.0	2	–			
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 100 μA	1.65–3.6	–	0.2	V
		I <sub>OL</sub> = 4 mA	1.65	–	0.45	
		I <sub>OL</sub> = 6 mA	2.3	–	0.4	
		I <sub>OL</sub> = 12 mA	2.3	–	0.7	
			2.7	–	0.4	
I <sub>OL</sub> = 24 mA	3.0	–	–			
I <sub>I</sub>	Input Leakage Current	0 ≤ V <sub>I</sub> ≤ 3.6 V	3.6	–	±5.0	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6	–	10	μA
11I <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> – 0.6 V	3–3.6	–	750	μA

## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	T <sub>A</sub> = –40°C to +85°C, R <sub>L</sub> = 500 Ω								Unit
		C <sub>L</sub> = 50 pF				C <sub>L</sub> = 30 pF				
		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 1.8 V ± 0.15 V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay	1.0	3.0	–	3.5	1.0	3	1.0	4.4	ns

## CAPACITANCE

Symbol	Parameter	Test Conditions	T <sub>A</sub> = ± 25°C		Unit
			V <sub>CC</sub>	Typical	
C <sub>IN</sub>	Input Capacitance	V <sub>I</sub> = 0 V or V <sub>CC</sub>	3.3	4.5	pF
C <sub>PD</sub>	Power Dissipation Capacitance		3.3	23	
		f = 10 Mhz, C <sub>L</sub> = 50 pF	2.5	21	
1.8	20				

# 74ALVC00

## AC LOADING AND WAVEFORMS

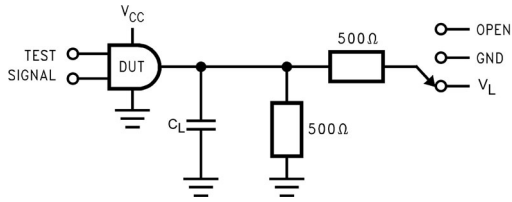


TABLE 1. Values for Figure 1

Test	Switch
$t_{PLH}, t_{PHL}$	Open

Figure 1. AC Test Circuit

TABLE 2. Variable Matrix

(Input Characteristics:  $f = 1\text{MHz}$ ;  $t_r = t_f = 2\text{ns}$ ;  $Z_0 = 50\ \Omega$ )

Symbol	$V_{CC}$			
	$3.3\text{ V} \pm 0.3\text{ V}$	$2.7\text{ V}$	$2.5\text{ V} \pm 0.2\text{ V}$	$1.8\text{ V} \pm 0.15\text{ V}$
$V_{mi}$	1.5 V	1.5 V	$V_{CC}/2$	$V_{CC}/2$
$V_{mo}$	1.5 V	1.5 V	$V_{CC}/2$	$V_{CC}/2$

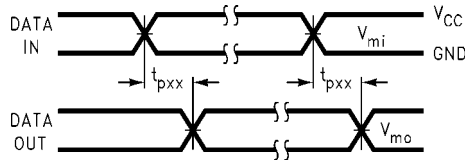


Figure 2. Waveform for Inverting and Non-inverting Functions

### ORDERING INFORMATION

Product Number	Package	Shipping <sup>†</sup>
74ALVC00MTC	TSSOP-14 WB (Pb-Free/Halide Free)	2500 / Tape and Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**TSSOP-14 WB**  
CASE 948G  
ISSUE C

DATE 17 FEB 2016

SCALE 2:1



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**GENERIC MARKING DIAGRAM\***



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



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