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VE-Trac™ Direct Quickstart Guide

This document is intended to be a guide to explain the connectivity and usage of the evaluation kit described in the table below. The evaluation kit is designed to quickly perform benchmarking or product evaluation at specific operating conditions in a lab environment. The product should only be operated and handled by qualified personnel with sufficient electrical engineering training and experience.

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APPLICATION NOTE

APPLIES TO THE FOLLOWING PARTS

NVH820S75L4SPB−EVK	750 V, 820 A module based 3−ph Evaluation kit

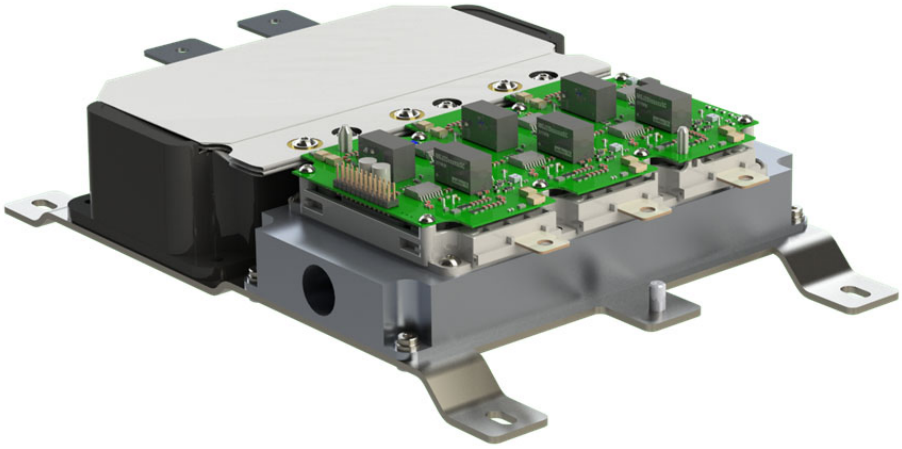

Figure 1.

INTRODUCTION

The VE−Trac Direct Evaluation Kit consists of a VE−Trac Direct power module (NVH820S75L4SPB) mounted on cooling jacket, with a 6−ch Gate driver board and a DC Link capacitor. The kit does not include a PWM controller or external current sensors. The user must user their on PWM controller to operate the system. External current sensors are needed if running closed loop for motor control. The evaluation kit allows the customers to evaluate VE−Trac Direct power module performance in their early stage of inverter development. The kit can be used as a double pulse tester to measure key switching parameters or used as a 3−ph inverter for motor control.

VE−Trac Direct evaluation kit features:

- Inverter evaluation Hardware kit for EV/HEV Traction Inverter applications (up to 150 kW)
- VE−Trac Direct NVH820S75L4SPB with 820 A, 750 V Field stop 4 IGBT/Diode chipset.
- Automotive Isolated high current and high efficiency IGBT gate driver with internal galvanic isolation, NCD57000.
- Implementation of basic protection like OTP and Desat.
- Custom Film DC Link capacitor rated up to 500 VDC, 500 μF.

TECHNICAL DETAILS

ON Semiconductor's latest generation of IGBTs and Diodes are incorporated into the VE−Trac Direct products. The 750 V products use the latest 4th Generation of FS4 IGBTs from ON Semiconductor.

Block Diagram

In this section, we describe the evaluation kit in detail, including block diagram, operating conditions, key components, On−chip current/temperature sensing and protection features.

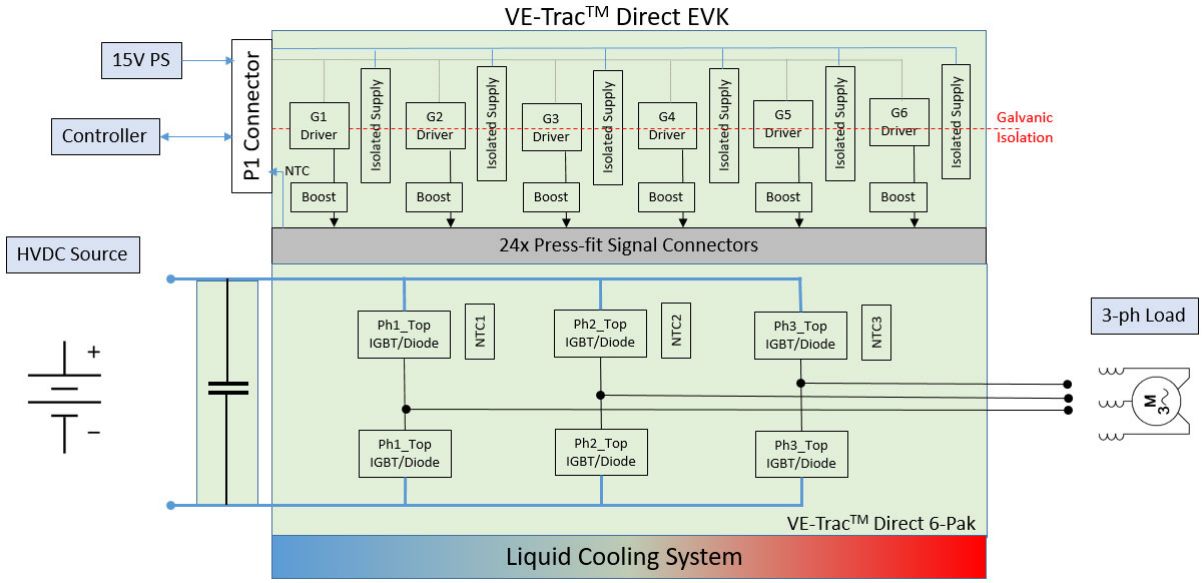

Figure 2. Simplified Block Diagram

The simplified block diagram gives a quick overview of the evaluation kit. The red dotted line shows the isolated section of the system.

Maximum Ratings

The VE−Trac Direct Evaluation kit is intended to be operated in a lab testing environment and should not be regarded as a protected system. Parts of the design have exposed high voltage and high temperatures that when accidentally contacted can result in electrical shock or severe burns. Therefore, it should only be handled by professionals with sufficient electrical engineering training and experience. Moreover, the operating conditions especially the thermal limits described below should be strictly followed for safety of the operator and the hardware.

Table 1. SUMMARY OF OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Conditions
Gate Driver Board Control Power	V_{Driv}	9 V	15 V	
DC Link Voltage	V_{BUS}	0V	500V	Limited by Capacitor
Peak Collector Phase Current (1ms)	I_{CPEAK}	−1640 A	1640 A	Limited by Tvj_Max
Maximum IGBT/FWD Junction Temperature	T_{VJ_Max}	−40°C	175°C	
Wait time after short circuit	SC	1s	–	
PCB Temperature	T_{PCB}		85°C	
Switching frequency	F_{SW}		12 kHz	
Coolant Temperature	T_c	−40°C	65°C	

Key Components

The evaluation kit is shipped in a hard plastic case with the following contents:

- Full assembled evaluation kit hardware.
- USB Drive containing all the required documentation.

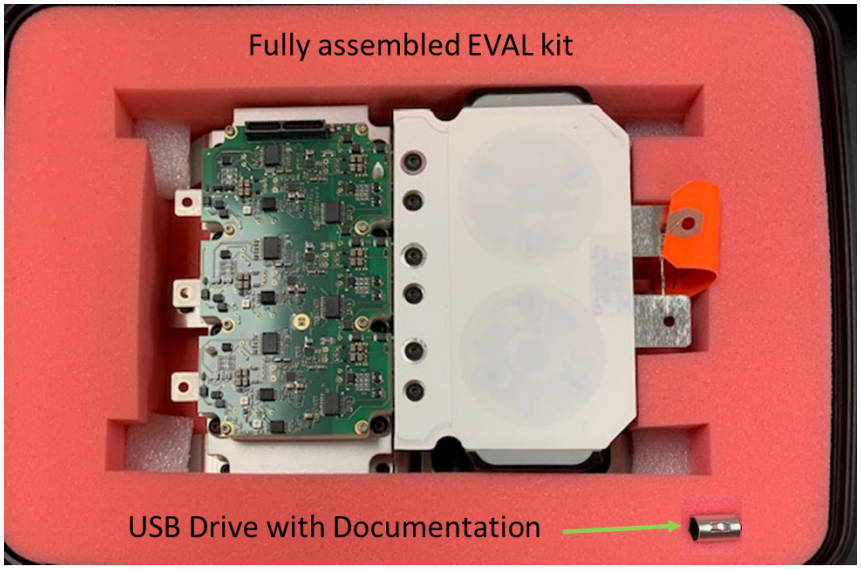

Figure 3. Shipping Contents in Case

The assembled evaluation kit assembly itself consists of the following major components.

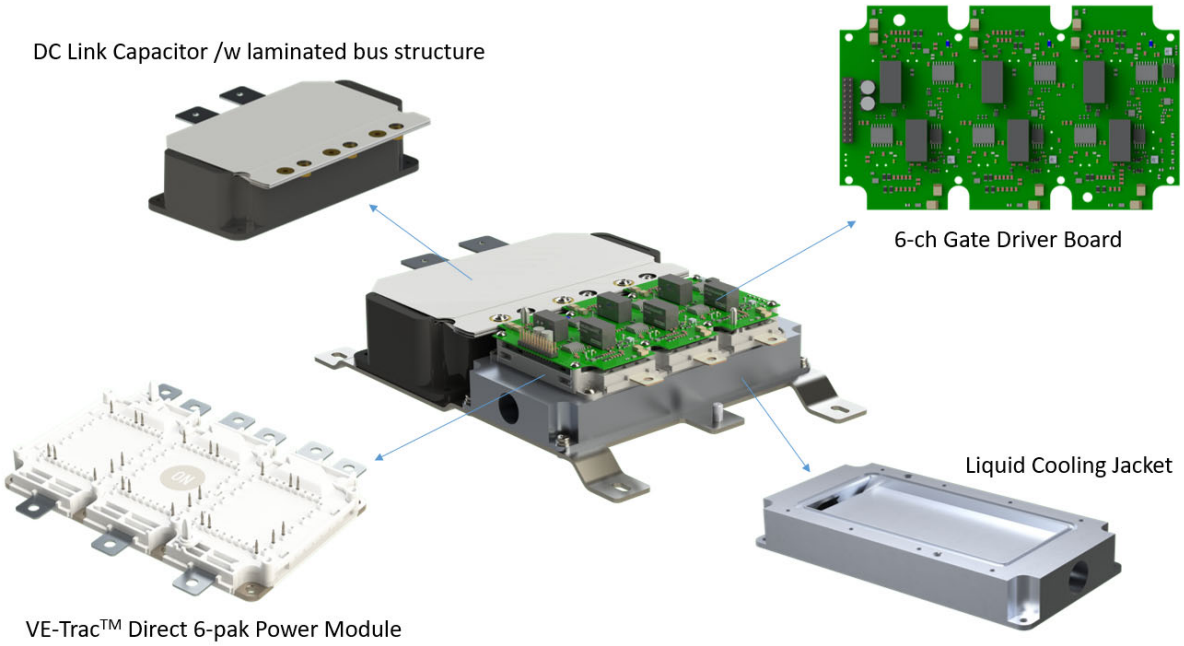

Figure 4. Major Components that Make up the Evaluation Kit

Table 2. SUPPLIERS FOR THE MAJOR COMPONENTS OF THE EVALUATION HARDWARE

Part Number	Manufacturer	Description
NVH820S75L4SPB	ON Semiconductor	Automotive VE−Trac Direct power module with FS4 750 V 820 A IGBT and Diode
NCD57000	ON Semiconductor	Automotive Isolated Gate Driver
6−Ch Gate Driver	ON Semiconductor	ON Semi design with outsourced manufacturing.
Liquid Cooling Jacket	ON Semiconductor	ON Semiconductor design with outsourced manufacturing.
700A186	SBE	DC Link Capacitor 500 V, 500 μF

Protection Features

The gate driver offers basic protection for Desat, Over Temperature and DC link over voltage. The protection trigger levels are set as below:

- Desat VCE.sat limit set to 9 V.
- Over Temperature Protection (OTP) for all phases set to 125°C
- DC Link Over Voltage Fault Threshold set to 550 VDC
- Additionally pad locations are provided for the user to implement active collector clamping if desired.

All faults are the latching type and requires a reset to clear the fault latch to start operating again. A fault reset switch is located on the driver board near the connector P1 for an operator to manually reset the faults. During a fault incident, a LED is lit to help the user identify the cause of the fault. Below is Fault Indication LED Matrix for the VE−Trac Direct evaluation kit.

Table 3. FAULT INDICATOR LEDs

Sch. Ref.	Description
D3	Ph1_BTM, Desat Fault
D12	Ph1_TOP, Desat Fault
D39	Ph2_BTM, Desat Fault
D21	Ph2_TOP, Desat Fault
D48	Ph3_BTM, Desat Fault
D30	Ph3_TOP, Desat Fault
D56	DC Link Over voltage fault
D55	NTC Fault, hottest NTC trigger

PCB AND CONNECTOR

Table 4. ELECTRICAL CONNECTIONS

Pin#	Signal	Function	Specification
CONNECTOR P1:			
1	+15V_in	Power supply	Power supply for PCB (primary side of CM choke)
2	+15V_in	Power supply	Power supply for PCB (primary side of CM choke)
3	GND_in	Ground reference	Ground return for External Power Input.
4	GND_in	Ground reference	Ground return for External Power Input
5	NC	No connection	
6	NC	No connection	
7	WL_P	Digital I/O	Differential pairs− Positive PWM input to phase 3 low side
8	WL_N	Digital I/O	Differential pairs− Negative PWM input to phase 3 low side
9	VL_P	Digital I/O	Differential pairs− Positive PWM input to phase 2 low side
10	VL_N	Digital I/O	Differential pairs− Negative PWM input to phase 2 low side
11	UL_P	Digital I/O	Differential pairs− Positive PWM input to phase 1 low side
12	UL_N	Digital I/O	Differential pairs− Negative PWM input to phase 1 low side
13	UH_P	Digital I/O	Differential pairs− Positive PWM input to phase 1 high side
14	UH_N	Digital I/O	Differential pairs− Negative PWM input to phase 1 high side
15	VH_P	Digital I/O	Differential pairs− Positive PWM input to phase 2 high side
16	VH_N	Digital I/O	Differential pairs− Negative PWM input to phase 2 high side
17	WH_P	Digital I/O	Differential pairs− Positive PWM input to phase 3 high side
18	WH_N	Digital I/O	Differential pairs− Negative PWM input to phase 3 high side
19	+15 V	Power supply reference	Power supply reference (secondary side of CM choke).
20	NTC1_temp	Analog Output	NTC temperature of Phase 1
21	GND	Ground reference	Ground reference (secondary side of CM choke).
22	NTC2_temp	Analog Output	NTC temperature of Phase 2
23	HV_read	Analog Output	Bus voltage of the capacitor.
24	NTC3_temp	Analog Output	NTC temperature of Phase 3

Table 5. PRESS−FIT CONNECTORS

Pin#	Data sheet Ref.	Function	Specification
1	C1	Analog Signal	Collector terminal of High side (phase1)
2	G1	Analog Signal	Gate terminal of High side (phase1)
3	E1	Analog Signal	Emitter terminal of High side (phase1)
4	T1	Analog Signal	NTC terminal (phase1)
5	T2	Analog Signal	NTC terminal (phase1)
6	C2	Analog Signal	Collector terminal of LOW side (phase1)
7	G2	Analog Signal	Gate terminal of LOW side (phase1)
8	E2	Analog Signal	Emitter terminal of LOW side (phase1)
9	C3	Analog Signal	Collector terminal of High side (phase2)
10	G3	Analog Signal	Gate terminal of High side (phase2)
11	E3	Analog Signal	Emitter terminal of High side (phase2)
12	T3	Analog Signal	NTC terminal (phase2)

Table 5. PRESS−FIT CONNECTORS

Pin#	Data sheet Ref.	Function	Specification
13	T4	Analog Signal	NTC terminal (phase2)
14	C4	Analog Signal	Collector terminal of LOW side (phase2)
15	G4	Analog Signal	Gate terminal of LOW side (phase2)
16	E4	Analog Signal	Emitter terminal of LOW side (phase2)
17	C5	Analog Signal	Collector terminal of High side (phase3)
18	G5	Analog Signal	Gate terminal of High side (phase3)
19	E5	Analog Signal	Emitter terminal of High side (phase3)
20	T5	Analog Signal	NTC terminal (phase3)
21	T6	Analog Signal	NTC terminal (phase3)
22	C6	Analog Signal	Collector terminal of LOW side (phase3)
23	G6	Analog Signal	Gate terminal of LOW side (phase3)
24	E6	Analog Signal	Emitter terminal of LOW side (phase3)

VE−Trac Direct Evaluation Kit Cooling System

The cooling jacket included in the evaluation kit provides a 1/2” Inch threaded hole for coolant inlet and outlet connections. In a typical lab use it’s recommended to use a 1/2” NPT – barb fitting for 1/2” ID hose as shown in the image below. The hose must selected such that it meets the planned maximum operating coolant temperature and pressure requirements of the pump. Use 50% Water/50% Ethylene Glycol as cooling fluid and make sure that cooling fluid corrosion protection is compatible with aluminum heatsink. We strongly recommend not use pure water as cooling fluid because it might damage the heatsink.

Figure 5. 1/2” NPT – 1/2” Hose Bard Fitting

EXAMPLE TESTING RESULTS

All evaluation kits have been tested to the following operating conditions using a 3−ph inductive load.

Table 6. FINAL TEST PARAMETERS

Final Test Conditions		
Bus Voltage	400	VDC
Output Current	500	Arms
Gate Resistors on/off	8/12	Ohms
Gate Voltage	+15/−8	V
PWM frequency	8	kHz
3−ph inductive load	30	uH
PF	~0.14	
MI	0.32	
Output Frequency	440	Hz
Coolant Type	EGW 50/50	
Coolant temperature	65	C
Flow rate	10	LPM

The following data is based on the operating conditions stated in the above table.

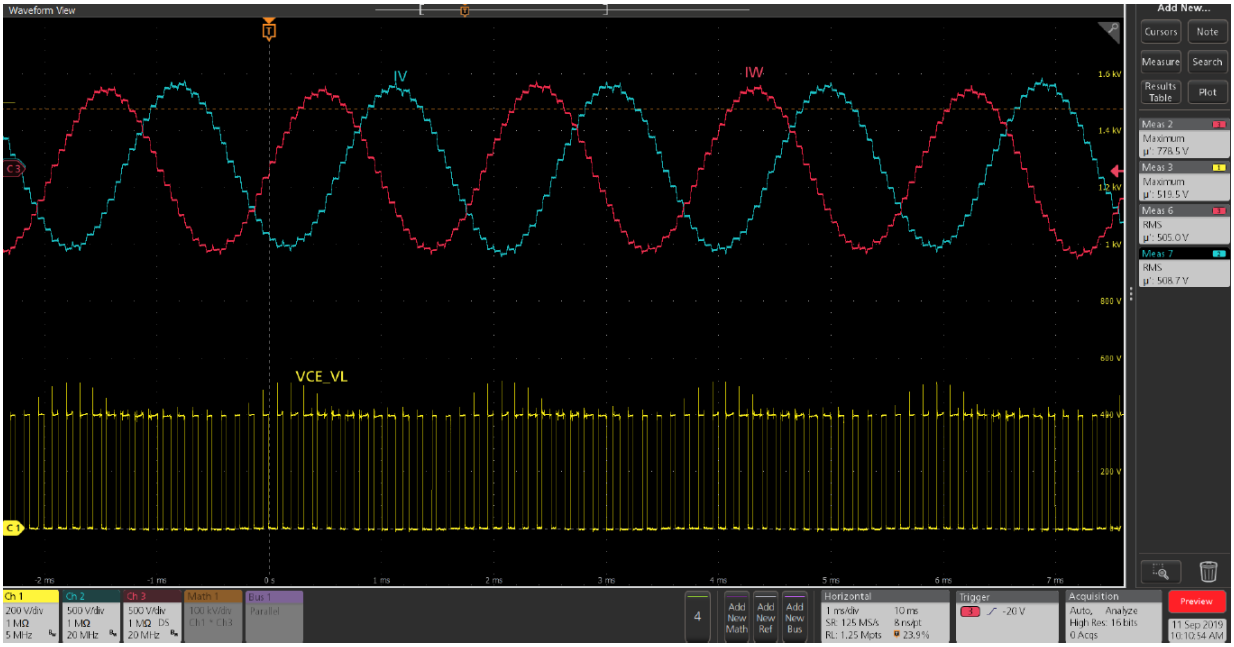

Figure 6. Output Current Waveform for the Test Conditions Stated in the Table Above

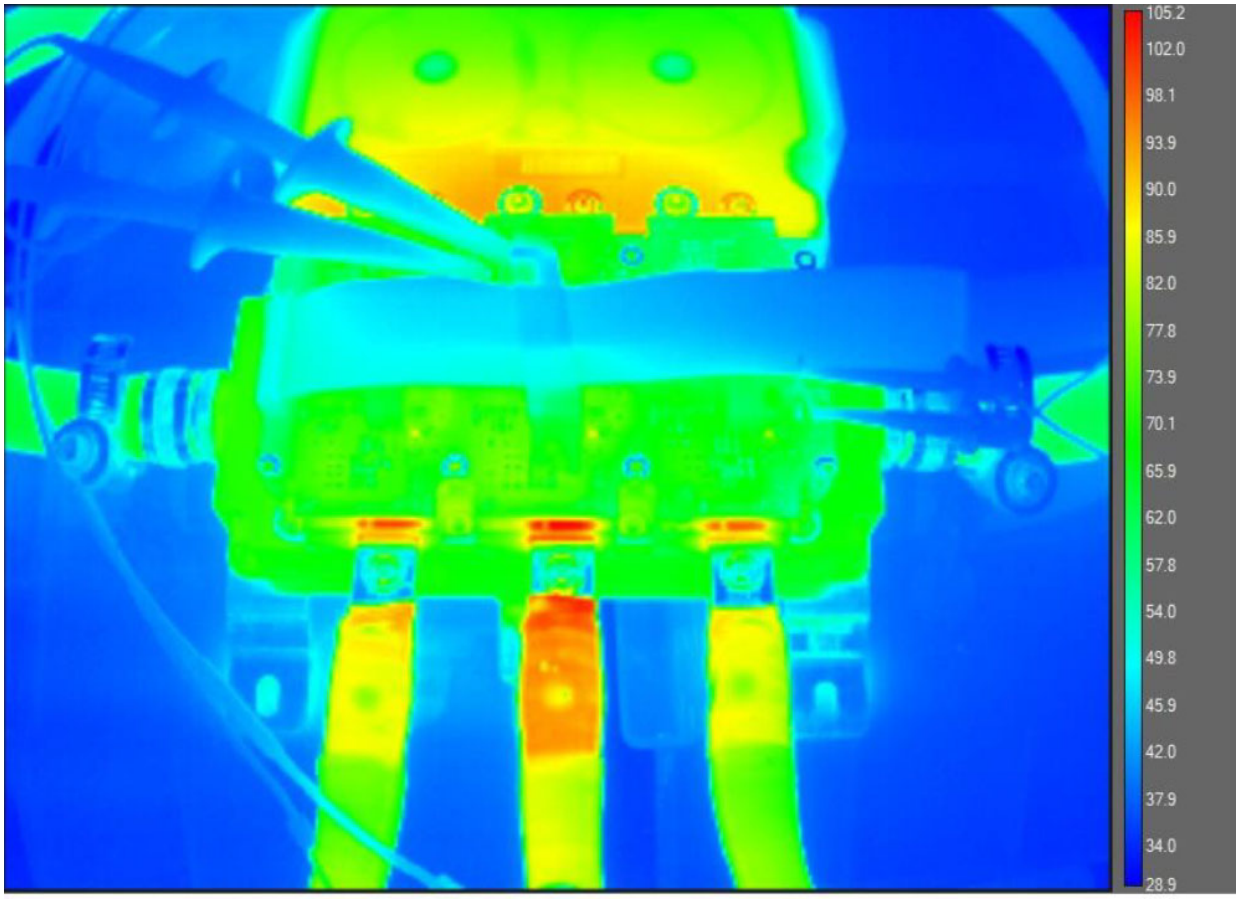

Figure 7. Thermal Image of the Evaluation Unit Under Test at the Specified Conditions Stated in the Above Table

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